

FORESEE®

LPDDR Datasheet

D-00263

FLXC2002G-C4

Version 1.1

LONGSYS ELECTRONICS RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE. Products and specifications discussed herein are for reference purposes only. All information discussed herein is provided on an "AS IS" basis, without warranties of any kind. All brand names, trademarks and registered trademarks belong to their respective owners. This document and all information discussed herein remain the sole and exclusive property of Longsys Electronics. No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or other-wise.

For updates or additional information about Longsys products, contact your nearest Longsys office.

© 2021 Shenzhen Longsys Electronics Co., Ltd. All rights reserved.

Revision History

Rev.	Date	Changes
1.0	2021/10/09	Document Create.
1.1	2021/11/18	Modify the frequency.

CONTENTS

Revision History 2

CONTENTS 3

1 Key Features 4

2 SDRAM Addressing 5

3 Functional Block Diagram 6

4 Ordering Information 7

5 Ball Assignment 8

6 Pin Description 9

7 Package Information 10

8 Input/Output Capacitance 11

 8.1 IDD Specification Parameters and Operating Conditions 11

 8.2 Absolute Maximum DC Ratings 14

 8.3 Recommended DC Operating Conditions 14

 8.4 Initialization Timing Parameters 15

 8.5 AC Timing 16

 8.5.1 Clock Timing 16

 8.5.2 Read Output Timing 16

 8.5.3 Write Timing 17

1 Key Features

Features

- Ultra-low-voltage core and I/O power supplies
 - VDD1 = 1.70–1.95V; 1.8V nominal
 - VDD2 = 1.06–1.17V; 1.10V nominal
 - VDDQ = 0.57–0.65V; 0.6V nominal
- Frequency range
 - 1866 –10 MHz (data rate range: 3733–20 Mbps/pin)
- 16n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =16,32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 15 GB/s per chip (2 channels x 7.5 GB/s)

- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable VSSQ (ODT) termination
- Single-ended CK and DQS support

Options

- VDD1/VDD2/VDDQ: 1.8V/1.1V/0.6V
- Array configuration
 - 512Meg x 32 (2 channels x16 I/O)
- Device configuration
 - 512M16 x 2 die in package
- FBGA “green” package
 - 200-ball VFBGA (10mm x 14.5mm x1.0mm max)
- Speed grade, cycle time
 - 536ps @ RL = 32/36
- Operating temperature range –25°C to +85°C

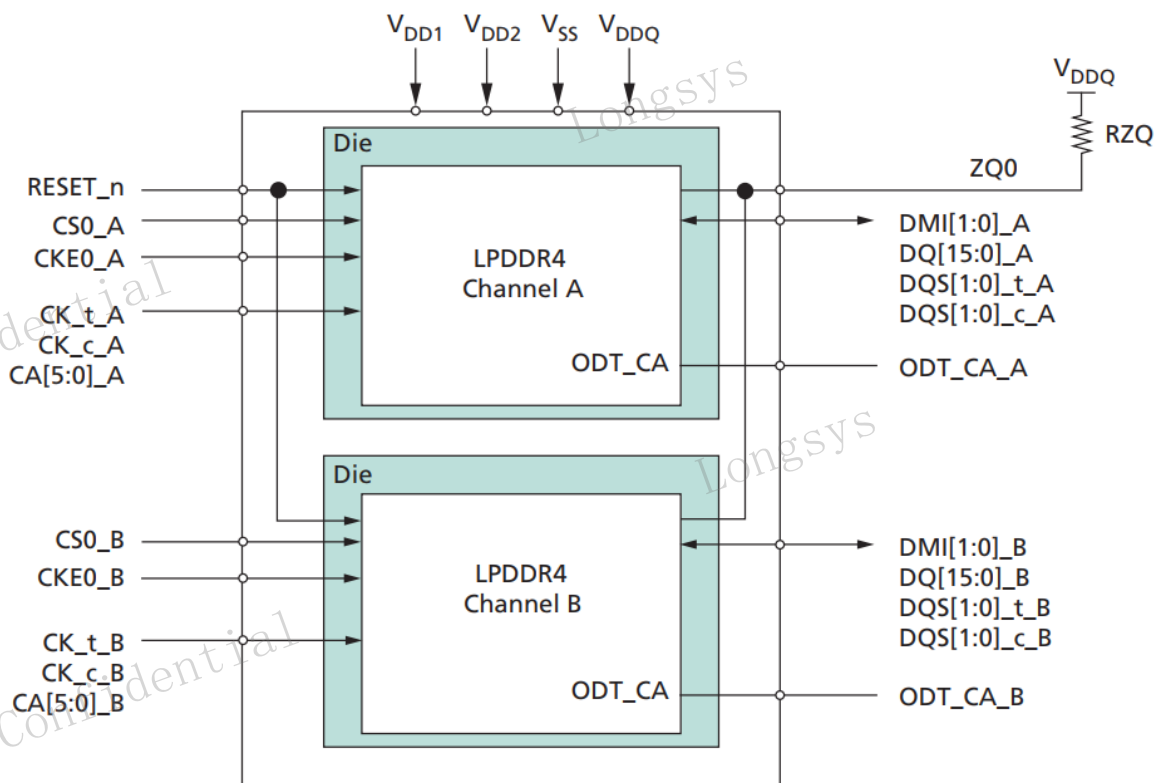
2 SDRAM Addressing

Configuration			512Meg x 32 (16Gb/Package)
Die Configuration	Channel A, Rank 0		x16 mode x 1 die
	Channel B, Rank 0		x16 mode x 1 die
	Channel A, Rank 1		NA
	Channel B, Rank 1		NA
Die Addressing	Device density (per die)		8Gb
	Device density (per channel)		8Gb
	Configuration(per die)		64Mb × 16 DQ × 8 banks
	Number of channels (per die)		1
	Number of banks (per channel)		8
	Array prefetch (bits, per channel)		256
	Number of rows (per channel)		65336
	Number of columns (fetch boundaries)		64
	Page size (bytes)		2048
	Channel density (bits per channel)		8,589,934,592
	Total density (bits per die)		8,589,934,592
	Bank address		BA[2:0]
	x16	Row address	R[15:0]
		Column address	C[9:0]
	Burst starting address boundary		

3 Functional Block Diagram

DRAM Block Diagrams

Dual -Die, Dual-Channel, Package Block Diagram



4 Ordering Information

Part Number	Package Size(mm)	Memory Combination	Operation Voltage	Density	Speed	Package
FLXC2002G-C4	10*14.5*1.0 (max)	LPDDR4X	1.8V/1.1V/0.6V	16Gb	3733Mbps	200ball FBGA (Lead & Halogen Free)

F L X C 2 002G- C4

FORESEE

Reserved

Product Name: LPDDR4X

LPDDR4X Capacity

Package:10x14.5 (mm²),200ball

Reserved

5 Ball Assignment

200-Ball Dual-Channel Discrete VFBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V _{SS}	V _{DD2}	ZQ0			NC	V _{DD2}	V _{SS}	DNU	DNU
B	DNU	DQ0_A	V _{DDQ}	DQ7_A	V _{DDQ}			V _{DDQ}	DQ15_A	V _{DDQ}	DQ8_A	DNU
C	V _{SS}	DQ1_A	DMI0_A	DQ6_A	V _{SS}			V _{SS}	DQ14_A	DMI1_A	DQ9_A	V _{SS}
D	V _{DDQ}	V _{SS}	DQS0_t_A	V _{SS}	V _{DDQ}			V _{DDQ}	V _{SS}	DQS1_t_A	V _{SS}	V _{DDQ}
E	V _{SS}	DQ2_A	DQS0_c_A	DQ5_A	V _{SS}			V _{SS}	DQ13_A	DQS1_c_A	DQ10_A	V _{SS}
F	V _{DD1}	DQ3_A	V _{DDQ}	DQ4_A	V _{DD2}			V _{DD2}	DQ12_A	V _{DDQ}	DQ11_A	V _{DD1}
G	V _{SS}	ODT_CA_A	V _{SS}	V _{DD1}	V _{SS}			V _{SS}	V _{DD1}	V _{SS}	NC	V _{SS}
H	V _{DD2}	CA0_A	NC	CS0_A	V _{DD2}			V _{DD2}	CA2_A	CA3_A	CA4_A	V _{DD2}
J	V _{SS}	CA1_A	V _{SS}	CKE0_A	NC			CK_t_A	CK_c_A	V _{SS}	CA5_A	V _{SS}
K	V _{DD2}	V _{SS}	V _{DD2}	V _{SS}	NC			NC	V _{SS}	V _{DD2}	V _{SS}	V _{DD2}
L												
M												
N	V _{DD2}	V _{SS}	V _{DD2}	V _{SS}	NC			NC	V _{SS}	V _{DD2}	V _{SS}	V _{DD2}
P	V _{SS}	CA1_B	V _{SS}	CKE0_B	NC			CK_t_B	CK_c_B	V _{SS}	CA5_B	V _{SS}
R	V _{DD2}	CA0_B	NC	CS0_B	V _{DD2}			V _{DD2}	CA2_B	CA3_B	CA4_B	V _{DD2}
T	V _{SS}	ODT_CA_B	V _{SS}	V _{DD1}	V _{SS}			V _{SS}	V _{DD1}	V _{SS}	RESET_n	V _{SS}
U	V _{DD1}	DQ3_B	V _{DDQ}	DQ4_B	V _{DD2}			V _{DD2}	DQ12_B	V _{DDQ}	DQ11_B	V _{DD1}
V	V _{SS}	DQ2_B	DQS0_c_B	DQ5_B	V _{SS}			V _{SS}	DQ13_B	DQS1_c_B	DQ10_B	V _{SS}
W	V _{DDQ}	V _{SS}	DQS0_t_B	V _{SS}	V _{DDQ}			V _{DDQ}	V _{SS}	DQS1_t_B	V _{SS}	V _{DDQ}
Y	V _{SS}	DQ1_B	DMI0_B	DQ6_B	V _{SS}			V _{SS}	DQ14_B	DMI1_B	DQ9_B	V _{SS}
AA	DNU	DQ0_B	V _{DDQ}	DQ7_B	V _{DDQ}			V _{DDQ}	DQ15_B	V _{DDQ}	DQ8_B	DNU
AB	DNU	DNU	V _{SS}	V _{DD2}	V _{SS}			V _{SS}	V _{DD2}	V _{SS}	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

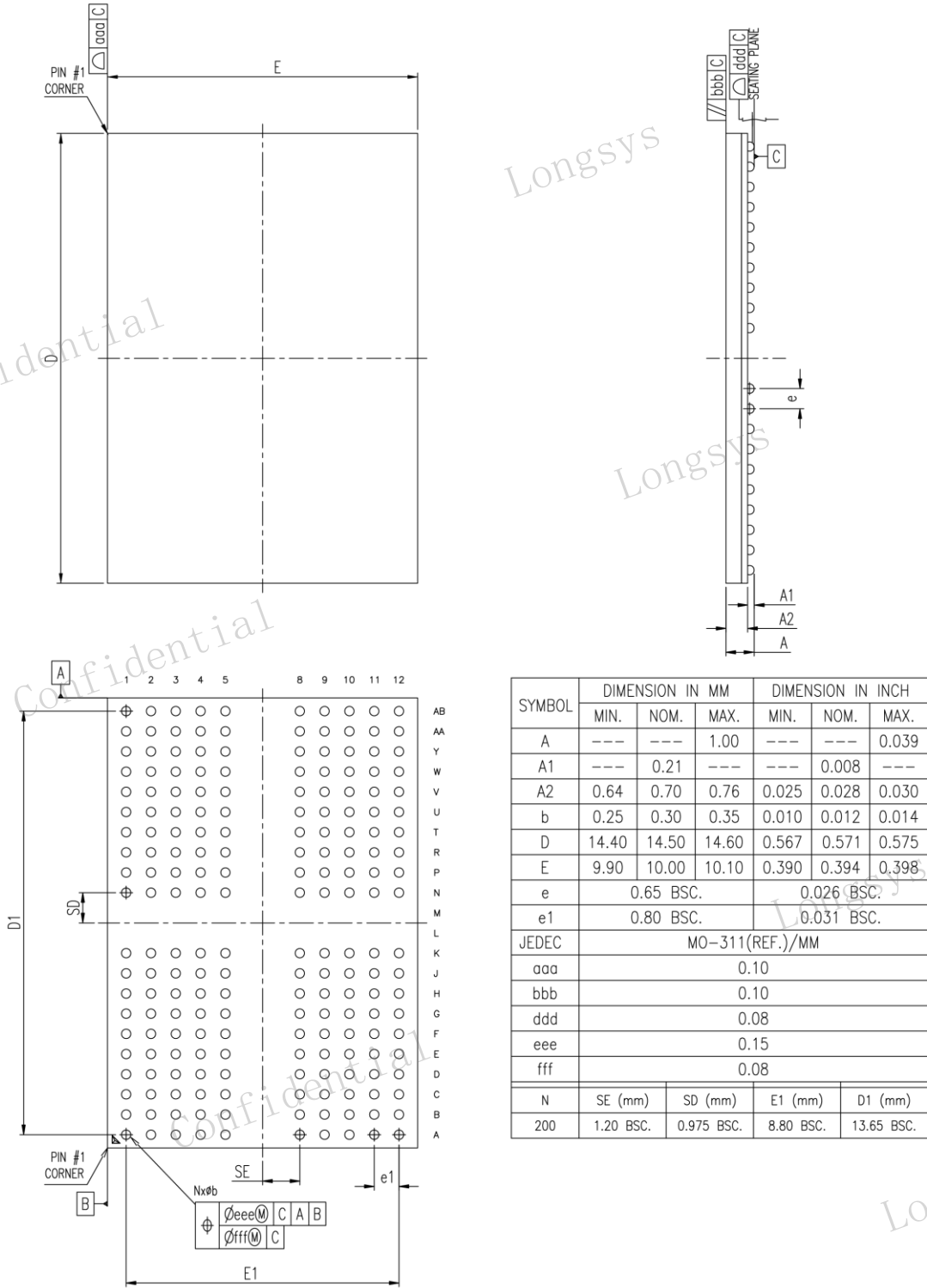
Top View (ball down)

LPDDR4_A(Channel A)
 LPDDR4_B(Channel B)
 ZQ, ODT_CA, RESET
 Supply
 Ground

6 Pin Description

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A, CKE0_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS0_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ0	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	-	Do not use: Must be grounded or left floating.
NC	-	No connect: Not internally connected.

7 Package Information



8 Input/Output Capacitance

Part Number	Parameter	Symbol	Min.	Max.	Unit	Notes
FLXC2002G-C4	Input capacitance, CK_t and CK_c	C _{CK}	0.5	0.9	pF	
	Input capacitance delta, CK_t and CK_c	C _{DCK}	0	0.09	pF	3
	Input capacitance, all other input-only pins	C _I	0.5	0.9	pF	4
	Input capacitance delta, all other input-only pins	C _{DI}	-0.10	0.10	pF	5
	Input/output capacitance, DQ, DMI, DQS_t, DQS_c	C _{IO}	0.7	1.3	pF	6
	Input/output capacitance delta, DQS_t, DQS_c	C _{DDQS}	0	0.1	pF	7
	Input/output capacitance delta, DQ, DMI	C _{DIO}	-0.1	0.1	pF	8
	Input/output capacitance ZQ pin	C _{ZQ}	0	5.0	pF	

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSS, VSS applied and all other pins floating).
3. Absolute value of CCK_t – CCK_c.
4. C_I applies to CS, CKE, and CA[5:0].
5. C_{DI} = C_I – 0.5 × (CCK_t + CCK_c); It does not apply to CKE.
6. DM loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. C_{DIO} = C_{IO} – Average (CDQn, CDMI, CDQS_t, CDQS_c) in byte-lane.

8.1 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Current	Notes
Operating one bank active-precharge current: tCK=tCK(MIN); tRC=tRC(MIN); CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD0 ₁	VDD1	TBD	
	IDD0 ₂	VDD2	TBD	
	IDD0 _Q	VDDQ	TBD	
Idle power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2P ₁	VDD1	TBD	
	IDD2P ₂	VDD2	TBD	
	IDD2P _Q	VDDQ	TBD	
Idle power-down standby current with clock stop: CK_t =LOW, CK_c = HIGH; CKE is LOW; CS is LOW; All banks	IDD2PS ₁	VDD1	TBD	

Parameter/Condition	Symbol	Power Supply	Current	Notes
are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2PS ₂	VDD2	TBD	
	IDD2PS _Q	VDDQ	TBD	
Idle non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2N ₁	VDD1	TBD	
	IDD2N ₂	VDD2	TBD	
	IDD2N _Q	VDDQ	TBD	
Idle non-power-down standby current with clock stopped: CK _t = LOW; CK _c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2NS ₁	VDD1	TBD	
	IDD2NS ₂	VDD2	TBD	
	IDD2NS _Q	VDDQ	TBD	
Active power-down standby current: tCK = tCK (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3P ₁	VDD1	TBD	
	IDD3P ₂	VDD2	TBD	
	IDD3P _Q	VDDQ	TBD	
Active power-down standby current with clock stop: CK _t = LOW, CK _c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3PS ₁	VDD1	TBD	
	IDD3PS ₂	VDD2	TBD	
	IDD3PS _Q	VDDQ	TBD	
Active non-power-down standby current: tCK = tCK (MIN); CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3N ₁	VDD1	TBD	
	IDD3N ₂	VDD2	TBD	
	IDD3N _Q	VDDQ	TBD	
Active non-power-down standby current with clock stopped: CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3NS ₁	VDD1	TBD	
	IDD3NS ₂	VDD2	TBD	
	IDD3NS _Q	VDDQ	TBD	

Parameter/Condition	Symbol	Power Supply	Current	Notes
Operating burst READ current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	IDD4R ₁	VDD1	TBD	
	IDD4R ₂	VDD2	TBD	
	IDD4R _Q	VDDQ	TBD	
Operating burst WRITE current: tCK = tCK (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WL(MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	IDD4W ₁	VDD1	TBD	
	IDD4W ₂	VDD2	TBD	
	IDD4W _Q	VDDQ	TBD	
All-bank REFRESH burst current: tCK = tCK (MIN); CKE is HIGH between valid commands; tRC = tRFCab (MIN); Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5 ₁	VDD1	TBD	
	IDD5 ₂	VDD2	TBD	
	IDD5 _Q	VDDQ	TBD	
All-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5AB ₁	VDD1	TBD	
	IDD5AB ₂	VDD2	TBD	
	IDD5AB _Q	VDDQ	TBD	
Per-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands tRC = Trefi/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5PB ₁	VDD1	TBD	
	IDD5PB ₂	VDD2	TBD	
	IDD5PB _Q	VDDQ	TBD	
Power-down self refresh current: CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled(25°C)	IDD6 ₁	VDD1	TBD	
	IDD6 ₂	VDD2	TBD	
	IDD6 _Q	VDDQ	TBD	

Notes:

- Published IDD values except IDD4RQ are the maximum of the distribution of the arithmetic mean. Refer to the following note for IDD4RQ.
- IDD4RQ value is reference only. Typical value. DBI disabled, VOH = VDDQ/3, TC = 25°C.
- Measurement conditions of IDD4R and IDD4W values: DBI disabled, BL = 16.

8.2 Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.5	V	1
VDDQ supply voltage relative to VSS	VDDQ	-0.4	1.5	V	1
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.5	V	
Storage temperature	TSTG	-55	125	°C	2

Notes:

- For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
- Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JESD51-2 standard.

8.3 Recommended DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit	Notes
VDD1	1.7	1.8	1.95	Core 1 power	V	1,2
VDD2	1.06	1.1	1.17	Core 2 power/Input buffer power	V	1,2,3
VDDQ	0.57	0.6	0.65	I/O buffer power	V	2,3

Notes:

- VDD1 uses significantly less power than VDD2.
- The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
- The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VREF(CA),max_r0	VREF(CA) range-0 MAX operating point	-	-	30%	VDD2	1,11
VREF(CA),min_r0	VREF(CA) range-0 MIN operating point	10%	-	-	VDD2	1,11
VREF(CA),max_r1	VREF(CA) range-1 MAX operating point	-	-	42%	VDD2	1,11
VREF(CA),min_r1	VREF(CA) range-1 MIN operating point	22%	-	-	VDD2	1,11
VREF(CA),step	VREF(CA) step size	0.30%	0.40%	0.50%	VDD2	2
VREF(CA),set_tol	VREF(CA) set tolerance	-1.00%	0.00%	1.00%	VDD2	3,4,6
		-0.10%	0.00%	0.10%	VDD2	3,5,7
tVREF_TIME-SHORT	VREF(CA) step time	-	-	100	ns	8
tVREF_TIME-MIDDLE		-	-	200	ns	12

Symbol	Parameter	Min	Typ	Max	Unit	Notes
tVREF_TIME-LONG		-	-	500	ns	9
tVREF_time_weak		-	-	1	ms	13,14
VREF(CA)_val_tol	VREF(CA) valid tolerance	-0.10%	0.00%	0.10%	VDD2	10

Notes:

1. $V_{REF(CA)}$ DC voltage referenced to $V_{DD2(DC)}$.
2. $V_{REF(CA)}$ step size increment/decrement range. $V_{REF(CA)}$ at DC level.
3. $V_{REF(CA),new} = V_{REF(CA),old} + n \times V_{REF(CA),step}$; n = number of steps; if increment, use "+"; if decrement, use "-".
4. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new} - 1.0\% \times V_{DD2}$. The maximum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new} + 1.0\% \times V_{DD2}$. For $n > 4$.
5. The minimum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new} - 0.10\% \times V_{DD2}$. The maximum value of $V_{REF(CA)}$ setting tolerance = $V_{REF(CA),new} + 0.10\% \times V_{DD2}$. For $n < 4$.
6. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output over the range, drawing a straight line between those points and comparing all other $V_{REF(CA)}$ output settings to that line.
7. Measured by recording the minimum and maximum values of the $V_{REF(CA)}$ output across four consecutive steps ($n = 4$), drawing a straight line between those points and comparing all other $V_{REF(CA)}$ output settings to that line.
8. Time from MRW command to increment or decrement one step size for $V_{REF(CA)}$.
9. Time from MRW command to increment or decrement $V_{REF,min}$ to $V_{REF,max}$ or $V_{REF,max}$ to $V_{REF,min}$ change across the $V_{REF(CA)}$ range in V_{REF} voltage.
10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.
11. DRAM range-0 or range-1 set by MR12 OP[6].
12. Time from MRW command to increment or decrement more than one step size up to a full range of VREF voltage within the same $V_{REF(CA)}$ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0b.
14. tVREF_time_weak covers all $V_{REF(CA)}$ range and value change conditions are applied to tVREF_TIME-SHORT/MIDDLE/LONG.

8.4 Initialization Timing Parameters

Parameter	Min	Max	Unit	Comment
tINIT0	-	20	ms	Maximum voltage ramp time
tINIT1	200	-	μs	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2	-	ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5	-	tCK	Minimum stable clock before first CKE HIGH
tINIT5	2	-	μs	Minimum idle time before first MRW/MRR command
tCKb	Note 1, 2	Note 1, 2	ns	Clock cycle time during boot

Notes:

1. Minimum tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by minimum tCKb. The higher boot frequency is system dependent.

8.5AC Timing

8.5.1 Clock Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit
			3200Mbps	3733Mbps	
Average clock period	$t_{CK(avg)}$	Min	625	536	ps
		Max	100		ns
Average HIGH pulse width	$t_{CH(avg)}$	Min	0.45		$t_{CK(avg)}$
		Max	0.55		
Average LOW pulse width	$t_{CL(avg)}$	Min	0.45		$t_{CK(avg)}$
		Max	0.55		
Absolute clock period	$t_{CK(abs)}$	Min	$t_{CK(avg)min} + t_{JIT(per)min}$		ps
Absolute clock HIGH pulse width	$t_{CH(abs)}$	Min	0.43		$t_{CK(avg)}$
		Max	0.57		
Absolute clock LOW pulse width	$t_{CL(abs)}$	Min	0.43		$t_{CK(avg)}$
		Max	0.57		
Clock period jitter	$t_{JIT(per)}$	Min	-40	-36	ps
		Max	40	36	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	$t_{JIT(cc)}$	Max	80	72	ps

8.5.2 Read Output Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit
			3200Mbps	3733Mbps	
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Disabled)	t_{DQSQ}	Max	0.18		UI
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	t_{QH}	Min	$Min(t_{QSH}, t_{QSL})$		ps
DQ output window time total, per pin (DBI-Disabled)	t_{QW_total}	Min	0.7		UI

Parameter	Symbol	Min/ Max	Data Rate		Unit
			3200Mbps	3733Mbps	
DQ output window time deterministic, per pin (DBI-Disabled)	t_{QW_dj}	Max	TBD		UI
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	t_{DQSQ_DBI}	Max	0.18		ps
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	t_{QH_DBI}	Min	$\text{Min}(t_{QSH_DBI}, t_{QSL_DBI})$		UI
DQ output window time total, per pin (DBI-Enabled)	$t_{QW_total_DBI}$	Min	0.7		UI
DQS_t, DQS_c differential output LOW time (DBI-Disabled)	t_{QSL}	Min	$t_{CL(ABS)} - 0.05$		$t_{CK(AVG)}$
DQS_t, DQS_c differential output HIGH time (DBI-Disabled)	t_{QSH}	Min	$t_{CH(ABS)} - 0.05$		$t_{CK(AVG)}$
DQS_t, DQS_c differential output LOW time (DBI-Enabled)	t_{QSL_DBI}	Min	$t_{CL(ABS)} - 0.045$		$t_{CK(AVG)}$
DQS_t, DQS_c differential output HIGH time (DBI-Enabled)	t_{QSH_DBI}	Min	$t_{CH(ABS)} - 0.045$		$t_{CK(AVG)}$

8.5.3 Write Timing

Parameter	Symbol	Min/ Max	Data Rate		Unit
			3200Mbps	3733Mbps	
Write command to 1st DQS latching	t _{DQSS}	Min	0.75		t _{ck(avg)}
		Max	1.25		
DQS input high-level width	t _{DQSH}	Min	0.4		t _{ck(avg)}
DQS input low-level width	t _{DQSL}	Min	0.4		t _{ck(avg)}

Parameter	Symbol	Min/ Max	Data Rate		Unit
			3200Mbps	3733Mbps	
DQS falling edge to CK setup time	t _{DSS}	Min	0.2		t _{ck(avg)}
DQS falling edge hold time from CK	t _{DSH}	Min	0.2		t _{ck(avg)}
Write preamble	t _{WPRE}	Min	2.0		t _{ck(avg)}
0.5 tCK Write postamble	t _{WPST}	Min	0.5		t _{ck(avg)}
1.5 tCK Write postamble	t _{WPST}	Min	1.5		t _{ck(avg)}