

野火_RK3528_LUBANCAT_Q1_原理图

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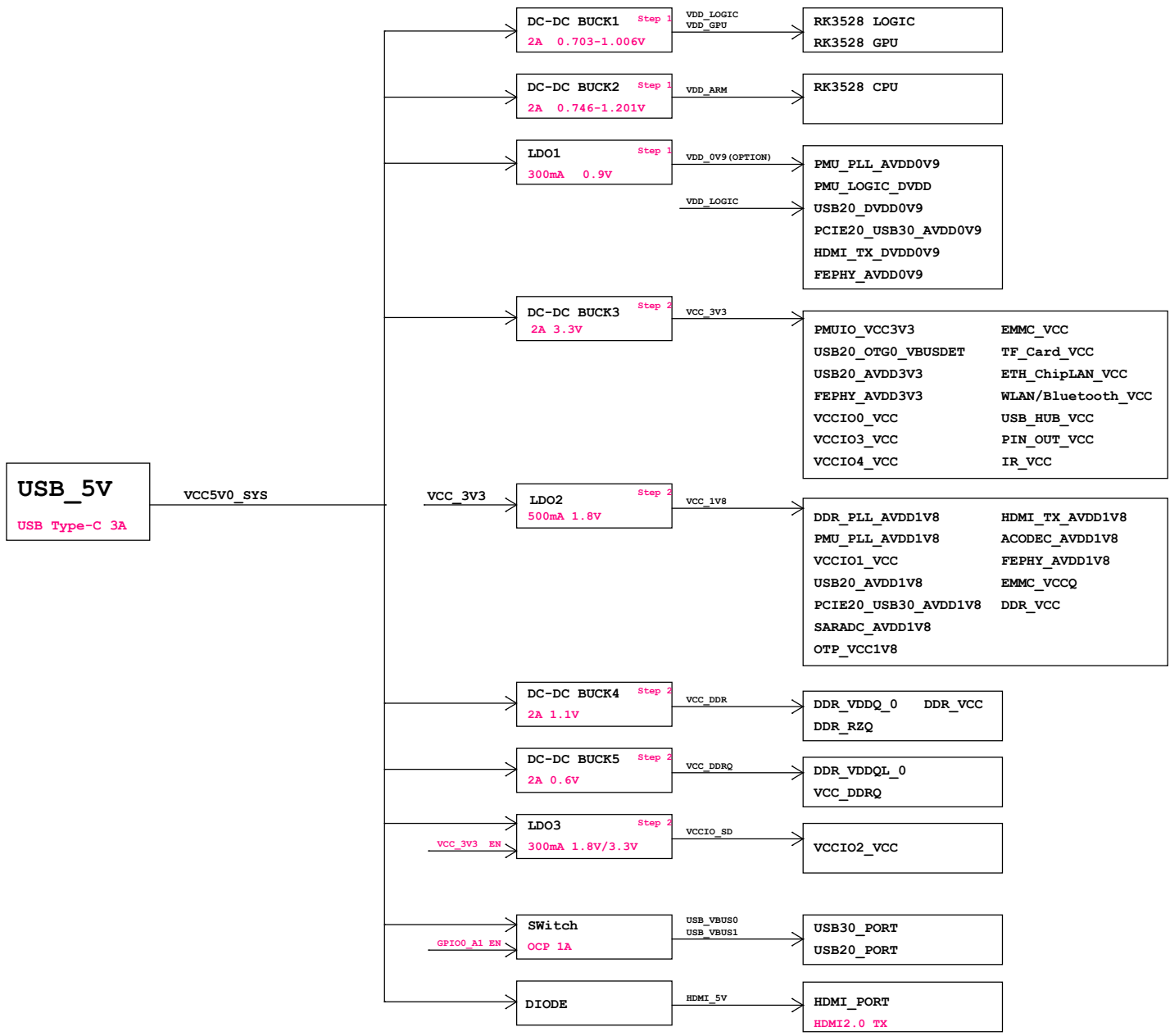
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历史版本

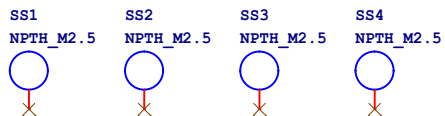
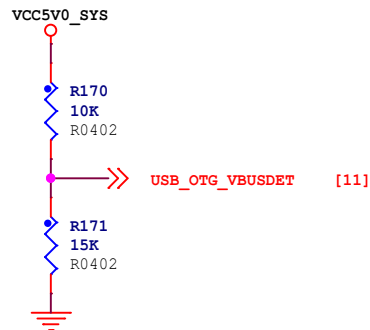
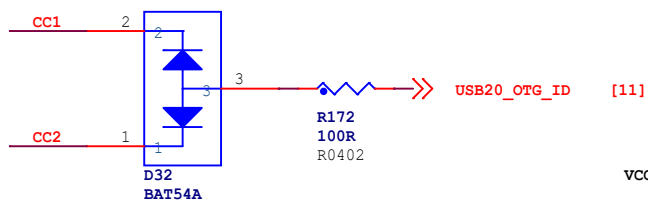
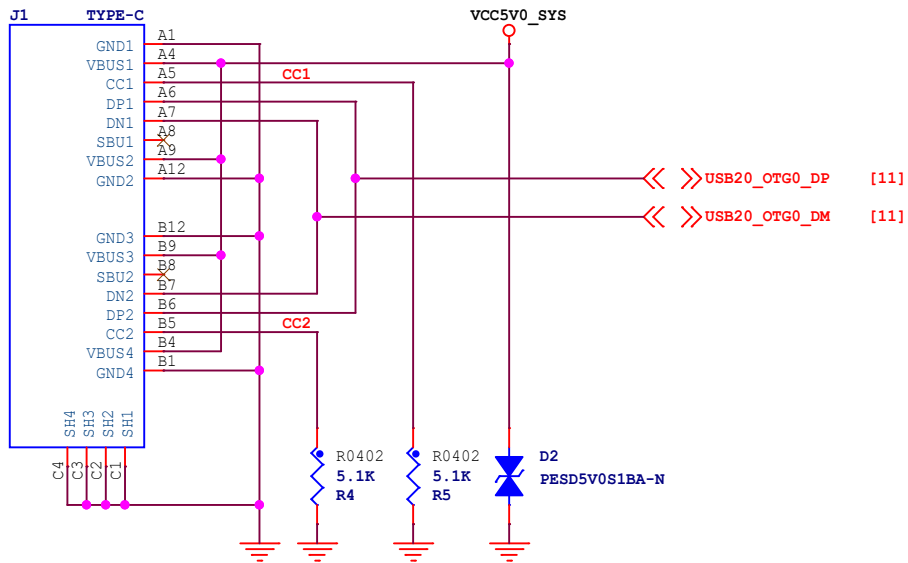
版本号	日期	设计	描述
V0.1	2023-11-22	ghs	初始版本
V0R2	2024-02-28	ghs	修正VCCIO3 Domain电源漏接与网卡LED接反问题
V1R0	2024-04-28	ghs	量产版本

POWER DIAGRAM

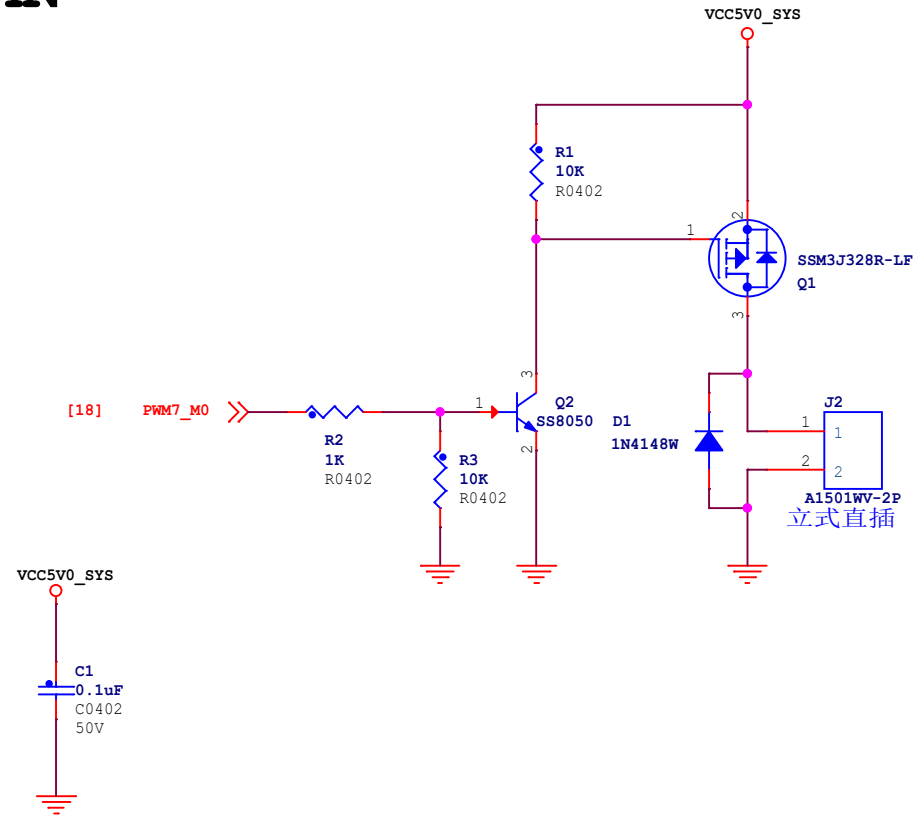


POWER IN OTG Download

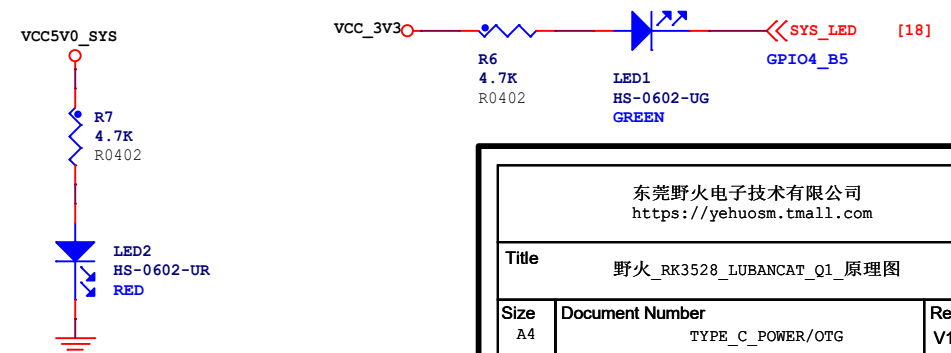
5V 3A



FAN



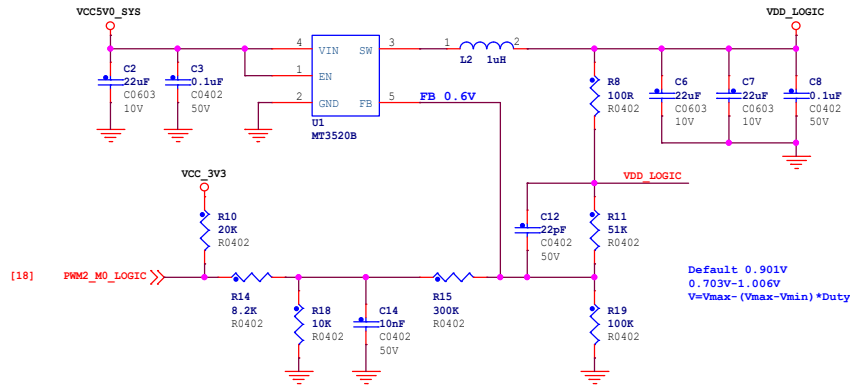
PWR/SYS_LED



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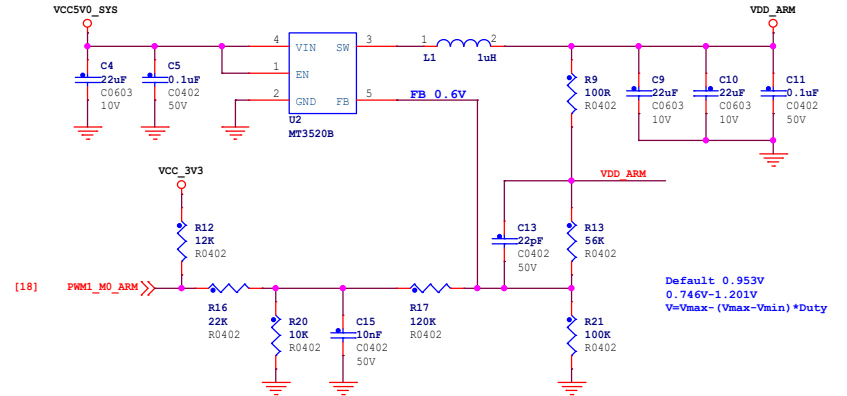
VCC5V0_SYS-->VDD_LOGIC

Step 1



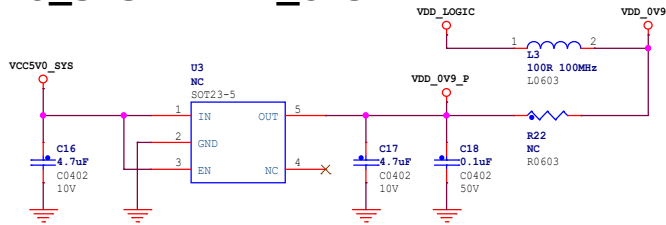
VCC5V0_SYS-->VDD_ARM

Step 1



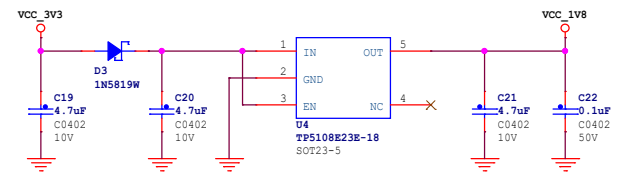
VCC5V0_SYS-->VDD_0V9

Step 1



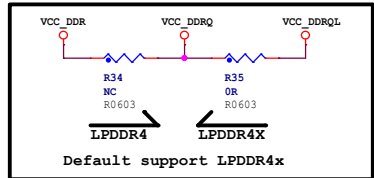
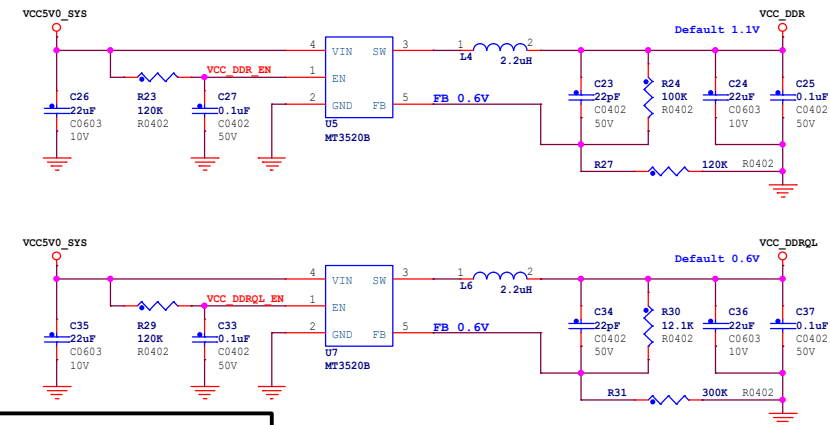
VCC_3V3-->VCC_1V8

Step 2



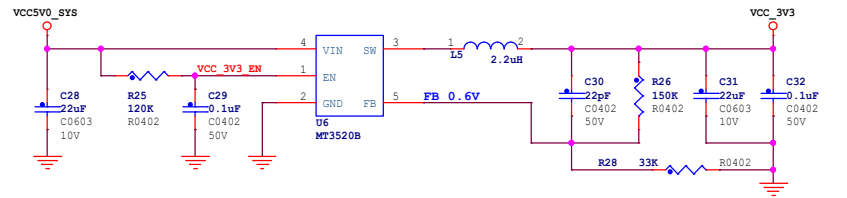
VCC5V0_SYS-->VCC_DDR/DDRQ

Step 2



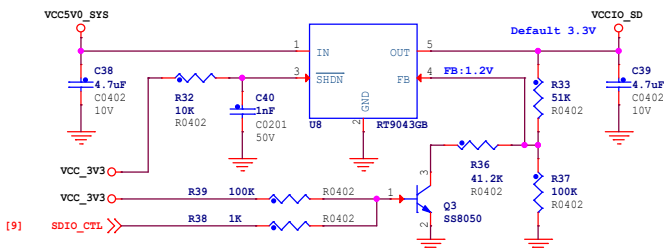
VCC5V0_SYS-->VCC_3V3

Step 2



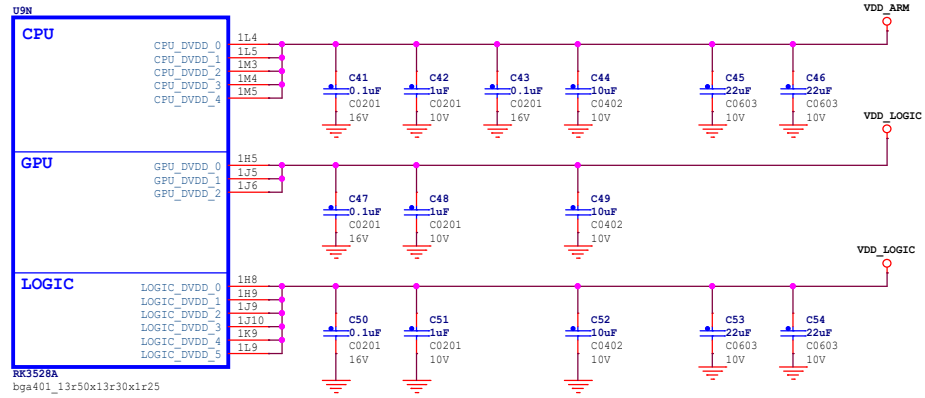
VCC5V0_SYS-->VCCIO_SD

Step 2

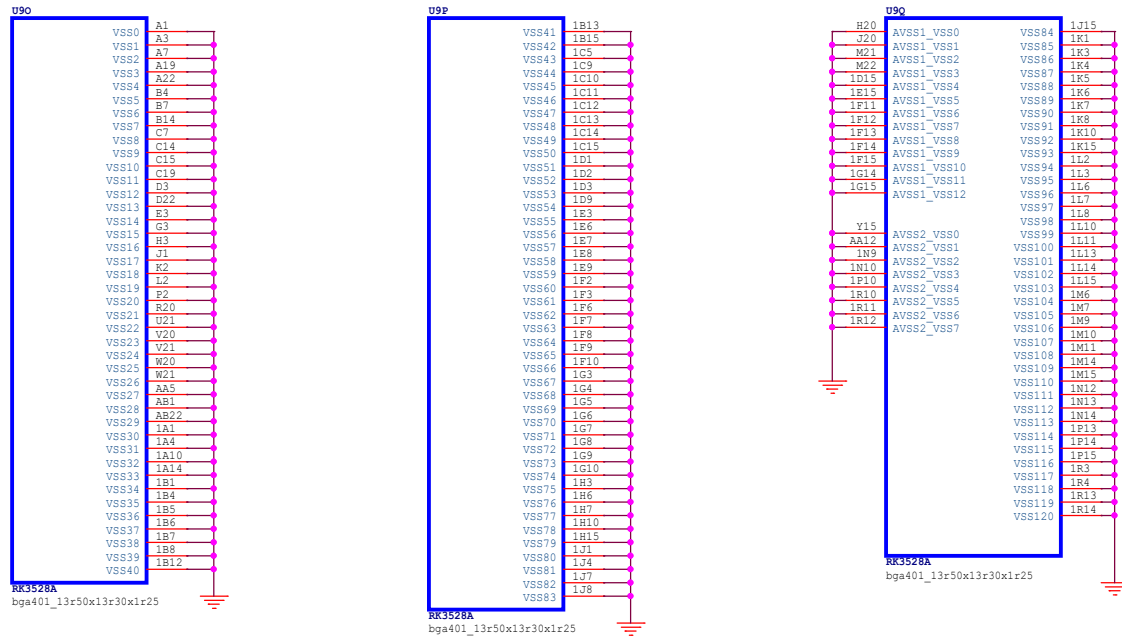


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RK3528_N (POWER)



RK3528_O/P/Q (GND)



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RK3528_A (DDR PHY)

U9A

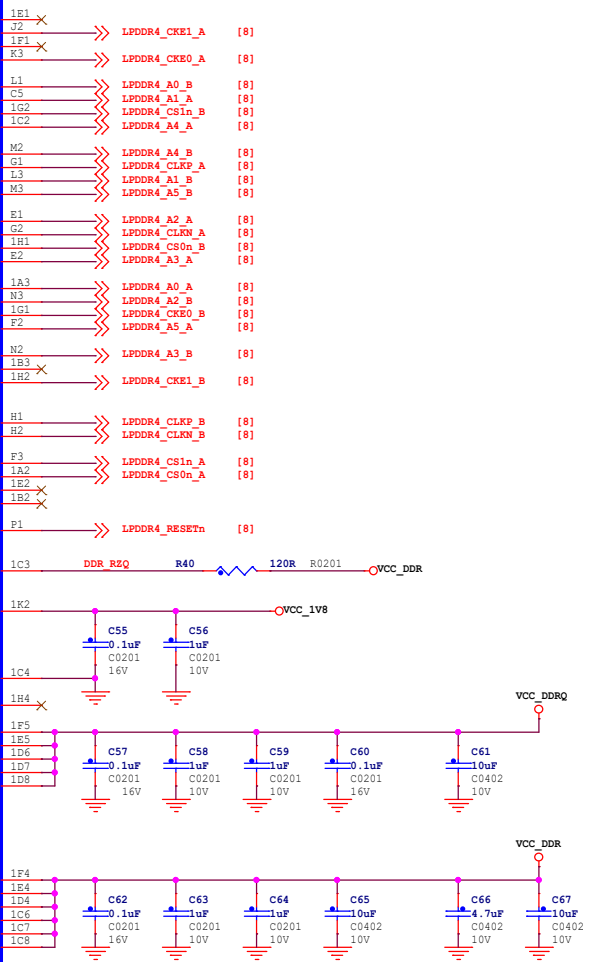
	DDR4	LPDDR4	DDR3	LPDDR3
(8) LPDDR4_D0_A	DDRPHY_A_DQ0	DDR4_DQ16_A	LPDDR4_DQ0_A	DDR3_D4
(8) LPDDR4_D1_A	DDRPHY_A_DQ1	DDR4_DQ17_A	LPDDR4_DQ1_A	DDR3_D0
(8) LPDDR4_D2_A	DDRPHY_A_DQ2	DDR4_DQ18_A	LPDDR4_DQ2_A	DDR3_D2
(8) LPDDR4_D3_A	DDRPHY_A_DQ3	DDR4_DQ19_A	LPDDR4_DQ3_A	DDR3_D1
(8) LPDDR4_D4_A	DDRPHY_A_DQ4	DDR4_DQ20_A	LPDDR4_DQ4_A	DDR3_D6
(8) LPDDR4_D5_A	DDRPHY_A_DQ5	DDR4_DQ21_A	LPDDR4_DQ5_A	DDR3_D7
(8) LPDDR4_D6_A	DDRPHY_A_DQ6	DDR4_DQ22_A	LPDDR4_DQ6_A	DDR3_D5
(8) LPDDR4_D7_A	DDRPHY_A_DQ7	DDR4_DQ23_A	LPDDR4_DQ7_A	DDR3_D3
(8) LPDDR4_DM0_A	DDRPHY_A_DM0	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0
(8) LPDDR4_DQS0P_A	DDRPHY_A_DQS0P	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P
(8) LPDDR4_DQS0N_A	DDRPHY_A_DQS0N	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N
(8) LPDDR4_D8_A	DDRPHY_A_DQ8	DDR4_DQ01_A	LPDDR4_DQ8_A	DDR3_D12
(8) LPDDR4_D9_A	DDRPHY_A_DQ9	DDR4_DQ02_A	LPDDR4_DQ9_A	DDR3_D14
(8) LPDDR4_D10_A	DDRPHY_A_DQ10	DDR4_DQ03_A	LPDDR4_DQ10_A	DDR3_D15
(8) LPDDR4_D11_A	DDRPHY_A_DQ11	DDR4_DQ04_A	LPDDR4_DQ11_A	DDR3_D9
(8) LPDDR4_D12_A	DDRPHY_A_DQ12	DDR4_DQ05_A	LPDDR4_DQ12_A	DDR3_D10
(8) LPDDR4_D13_A	DDRPHY_A_DQ13	DDR4_DQ06_A	LPDDR4_DQ13_A	DDR3_D8
(8) LPDDR4_D14_A	DDRPHY_A_DQ14	DDR4_DQ07_A	LPDDR4_DQ14_A	DDR3_D13
(8) LPDDR4_D15_A	DDRPHY_A_DQ15	DDR4_DQ08_A	LPDDR4_DQ15_A	DDR3_D11
(8) LPDDR4_DM1_A	DDRPHY_A_DM1	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1
(8) LPDDR4_DQS1P_A	DDRPHY_A_DQS1P	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P
(8) LPDDR4_DQS1N_A	DDRPHY_A_DQS1N	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N
(8) LPDDR4_D0_B	DDRPHY_B_DQ0	DDR4_DQ14_B	LPDDR4_DQ0_B	DDR3_D29
(8) LPDDR4_D1_B	DDRPHY_B_DQ1	DDR4_DQ15_B	LPDDR4_DQ1_B	DDR3_D31
(8) LPDDR4_D2_B	DDRPHY_B_DQ2	DDR4_DQ16_B	LPDDR4_DQ2_B	DDR3_D28
(8) LPDDR4_D3_B	DDRPHY_B_DQ3	DDR4_DQ17_B	LPDDR4_DQ3_B	DDR3_D30
(8) LPDDR4_D4_B	DDRPHY_B_DQ4	DDR4_DQ18_B	LPDDR4_DQ4_B	DDR3_D26
(8) LPDDR4_D5_B	DDRPHY_B_DQ5	DDR4_DQ19_B	LPDDR4_DQ5_B	DDR3_D24
(8) LPDDR4_D6_B	DDRPHY_B_DQ6	DDR4_DQ20_B	LPDDR4_DQ6_B	DDR3_D27
(8) LPDDR4_D7_B	DDRPHY_B_DQ7	DDR4_DQ21_B	LPDDR4_DQ7_B	DDR3_D25
(8) LPDDR4_DM0_B	DDRPHY_B_DM0	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM3
(8) LPDDR4_DQS0P_B	DDRPHY_B_DQS0P	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS3P
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(8) LPDDR4_D8_B	DDRPHY_B_DQ8	DDR4_DQ11_B	LPDDR4_DQ8_B	DDR3_D17
(8) LPDDR4_D9_B	DDRPHY_B_DQ9	DDR4_DQ12_B	LPDDR4_DQ9_B	DDR3_D19
(8) LPDDR4_D10_B	DDRPHY_B_DQ10	DDR4_DQ13_B	LPDDR4_DQ10_B	DDR3_D18
(8) LPDDR4_D11_B	DDRPHY_B_DQ11	DDR4_DQ14_B	LPDDR4_DQ11_B	DDR3_D22
(8) LPDDR4_D12_B	DDRPHY_B_DQ12	DDR4_DQ15_B	LPDDR4_DQ12_B	DDR3_D16
(8) LPDDR4_D13_B	DDRPHY_B_DQ13	DDR4_DQ16_B	LPDDR4_DQ13_B	DDR3_D20
(8) LPDDR4_D14_B	DDRPHY_B_DQ14	DDR4_DQ17_B	LPDDR4_DQ14_B	DDR3_D21
(8) LPDDR4_D15_B	DDRPHY_B_DQ15	DDR4_DQ18_B	LPDDR4_DQ15_B	DDR3_D23
(8) LPDDR4_DM1_B	DDRPHY_B_DM1	DDR4_DMU_B	LPDDR4_DM1_B	DDR3_DM2
(8) LPDDR4_DQS1P_B	DDRPHY_B_DQS1P	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS2P
(8) LPDDR4_DQS1N_B	DDRPHY_B_DQS1N	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS2N

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_ODT1_B	DDR3_A9	LPDDR3_ODT2
DDR4_A1	LPDDR4_CKE1_A	DDR3_A14	--
DDR4_A2	LPDDR4_ODT0_B	DDR3_A13	LPDDR3_ODT3
DDR4_A3	LPDDR4_CKE0_A	DDR3_A1	--
DDR4_A4	LPDDR4_A0_B	DDR3_A2	LPDDR3_A5
DDR4_A5	LPDDR4_A1_A	DDR3_A4	--
DDR4_A6	LPDDR4_CSNI_B	DDR3_A3	LPDDR3_CSNI2
DDR4_A7	LPDDR4_A4_A	DDR3_A6	--
DDR4_A8	LPDDR4_A4_B	DDR3_A5	LPDDR3_A6
DDR4_A9	LPDDR4_CLKP_A	DDR3_A11	LPDDR3_A2
DDR4_A10	LPDDR4_A1_B	DDR3_A0	--
DDR4_A11	LPDDR4_A5_B	DDR3_A7	LPDDR3_A7
DDR4_A12	LPDDR4_A2_A	DDR3_A10	LPDDR3_A4
DDR4_A13	LPDDR4_CLKN_A	DDR3_A8	LPDDR3_A3
DDR4_WEN/A14	LPDDR4_CSNI_B	DDR3_ODT0	LPDDR3_CSNI3
DDR4_CASW/A15	LPDDR4_A3_A	DDR3_BA1	LPDDR3_A0
DDR4_RASN/A16	LPDDR4_A0_A	DDR3_CKE0	--
DDR4_ACTN	LPDDR4_A2_B	DDR3_CSNI	LPDDR3_A9
DDR4_BA0	LPDDR4_CKE0_B	DDR3_BA2	LPDDR3_CKE0
DDR4_BA1	LPDDR4_A5_A	DDR3_A12	LPDDR3_A1
DDR4_BG0	LPDDR4_A3_B	DDR3_BA0	LPDDR3_A8
DDR4_BG1	--	DDR3_A15	--
DDR4_CKE	LPDDR4_CKE1_B	DDR3_RASN	--
DDR4_CLKP	LPDDR4_CLKP_B	DDR3_CLKP	LPDDR3_CLKP
DDR4_CLKN	LPDDR4_CLKN_B	DDR3_CLKN	LPDDR3_CLKN
DDR4_CSNI	LPDDR4_CSNI_A	DDR3_CASN	LPDDR3_CSNI1
DDR4_ODT0	LPDDR4_CSNI_B	DDR3_CSNI	LPDDR3_CSNI0
DDR4_ODT1	LPDDR4_ODT1_A	DDR3_WEN	LPDDR3_ODT0
DDR4_ODT1	LPDDR4_ODT1_A	DDR3_ODT1	LPDDR3_ODT1
DDR4_RESETN	LPDDR4_RESETN	DDR3_RESETN	--

Note: Sequences can not be swap

DDR3L = 1.35V
DDR3 = 1.5V
DDR4 = 1.2V
LPDDR3 = 1.2V
LPDDR4 = 1.1V
LPDDR4x = 0.6V

DDR3L = 1.35V
DDR3 = 1.5V
DDR4 = 1.2V
LPDDR3 = 1.2V
LPDDR4 = 1.1V
LPDDR4x = 1.1V



RK3528A
bga401_13r50x13r30x1r25

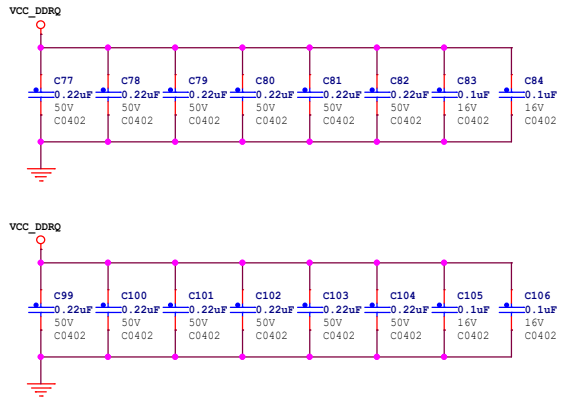
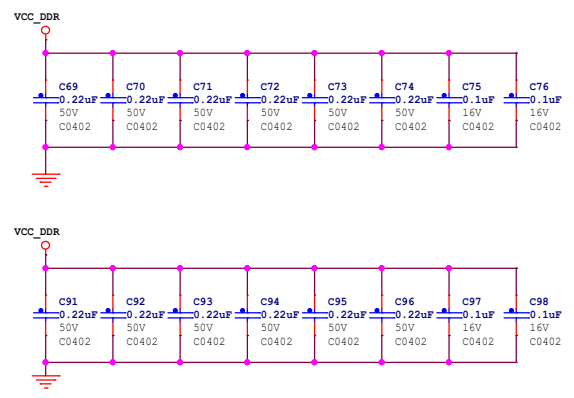
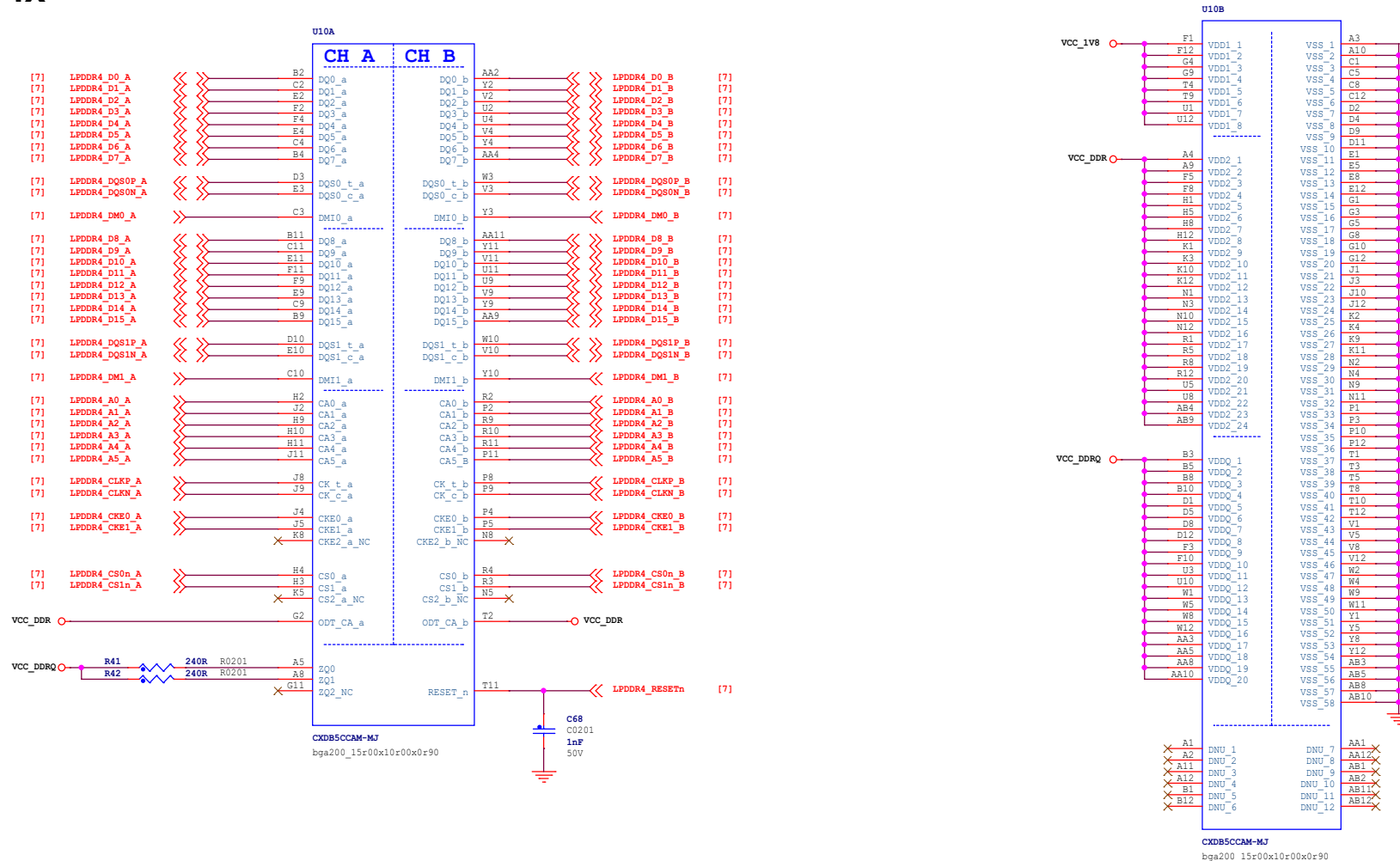
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Title: 野火_RK3528_LUBANCAT_q1_原理图

Size A3	Document Number: DDR Controller	Rev V1R0
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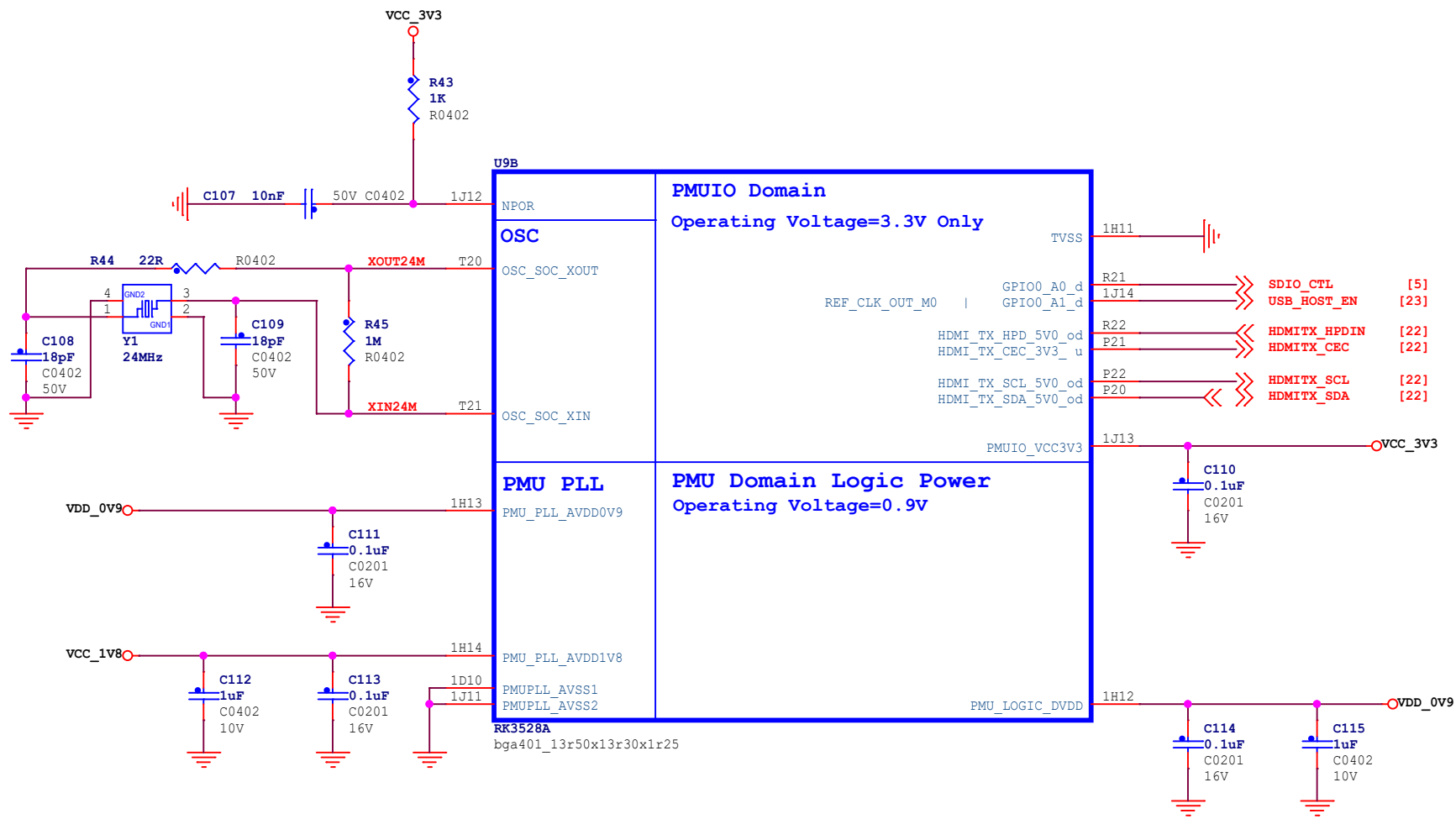
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LPDDR4/4X



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RK3528_B (OSC/PLL/PMUIO Domain)



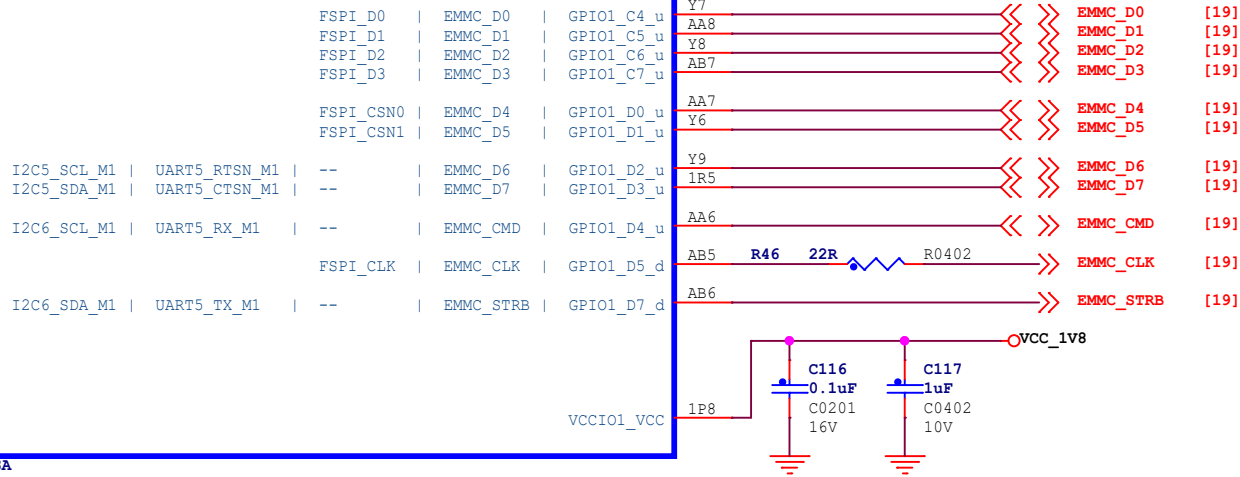
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RK3528_E (VCCIO1 Domain)

U9E

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

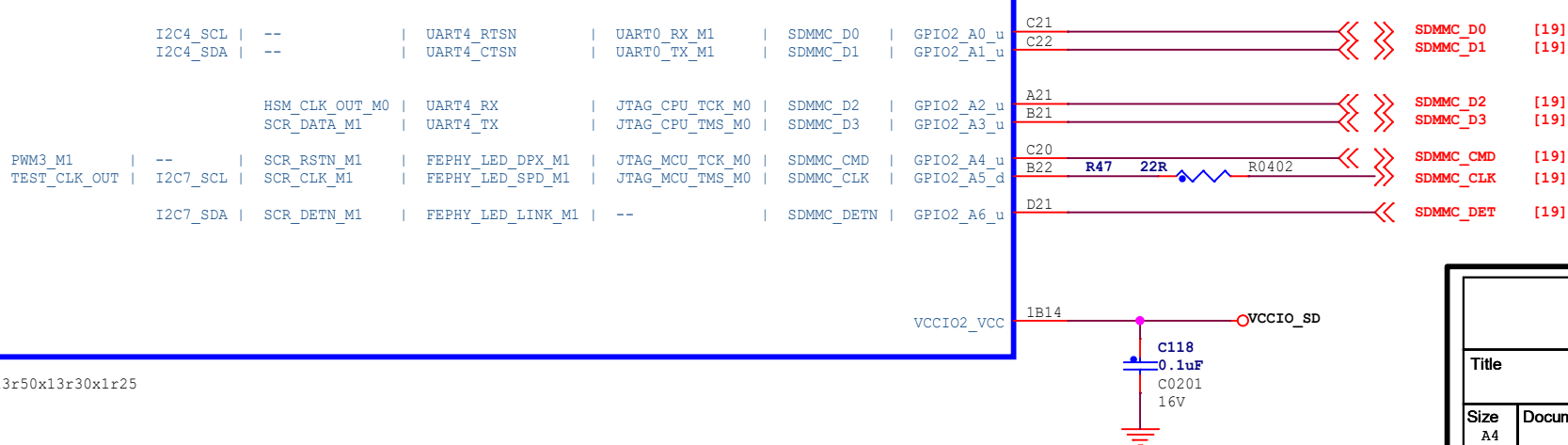


RK3528_F (VCCIO2 Domain)

U9F

VCCIO2 Domain

Operating Voltage=1.8V/3.3V



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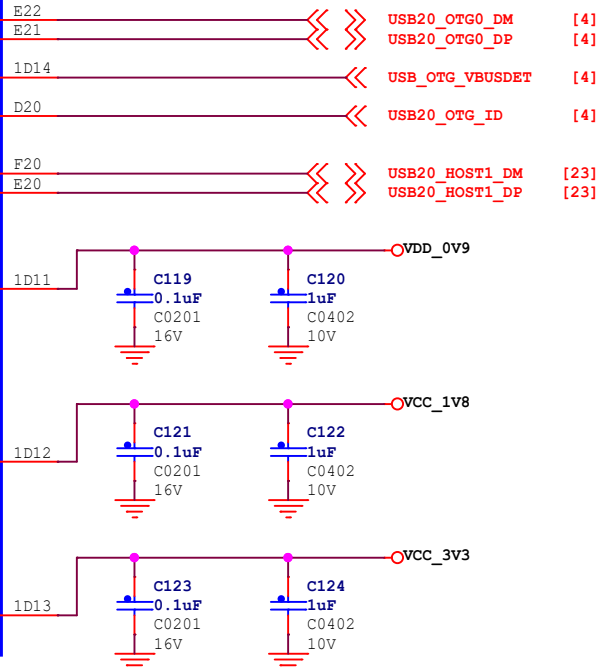
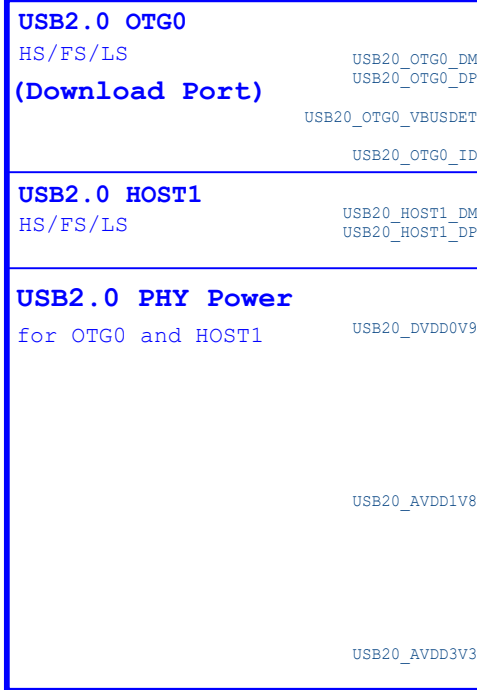
Title
野火_RK3528_LUBANCAT_Q1_原理图

Size A4	Document Number FLASH/SD Controller	Rev V1R0
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RK3528_I (USB2.0 OTG/HOST)

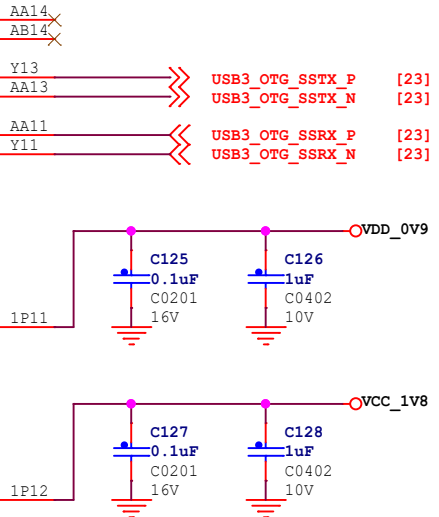
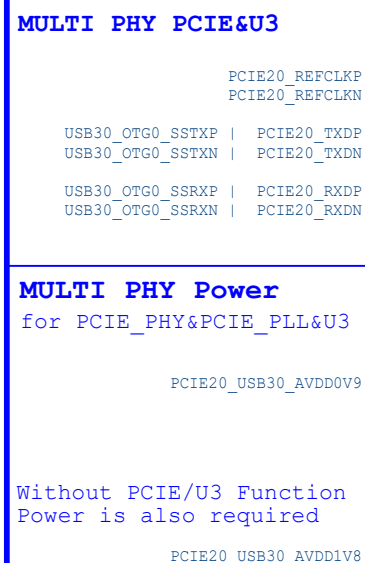
U9I



RK3528A
bga401_13r50x13r30x1r25

RK3528_J (PCIE2.0/U3 PHY)

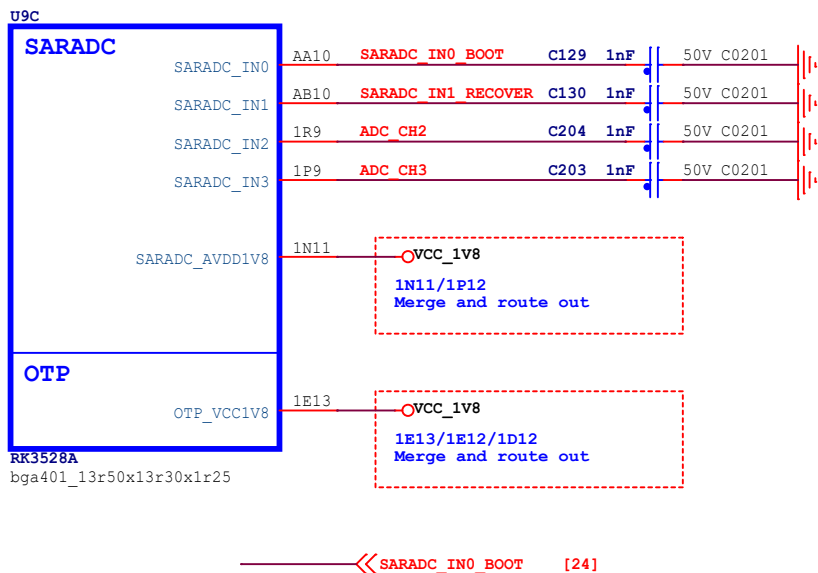
U9J



RK3528A
bga401_13r50x13r30x1r25

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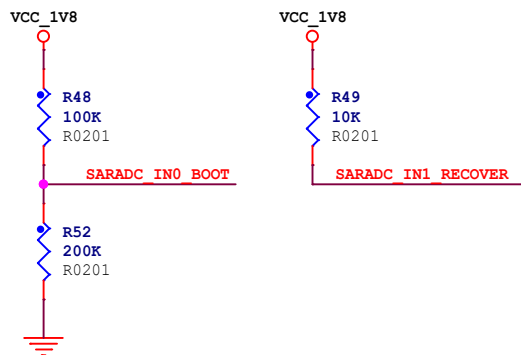
RK3528_C (Saradc/OTP)



TABLE

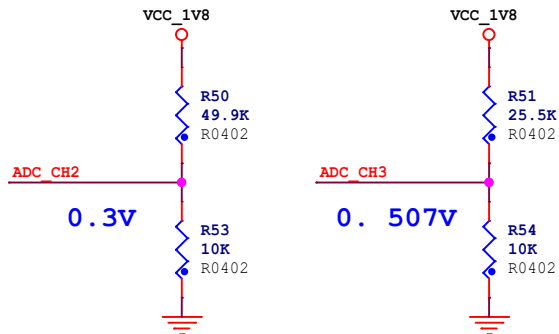
Item	Rup	Rdown	ADC	BOOT MODE
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	12K	114	
LEVEL3	100K	27K	228	FSPI--USB
LEVEL4	100K	51K	342	
LEVEL5	100K	82K	456	
LEVEL6	100K	120K	570	EMMC--USB
LEVEL7	100K	200K	683	EMMC--SD Card--USB
LEVEL8	100K	330K	796	SD Card--USB
LEVEL9	100K	820K	910	
LEVEL10	100K	DNP	1023	FSPI--EMMC--SD Card--USB

BOOT_SET



BOARD ID

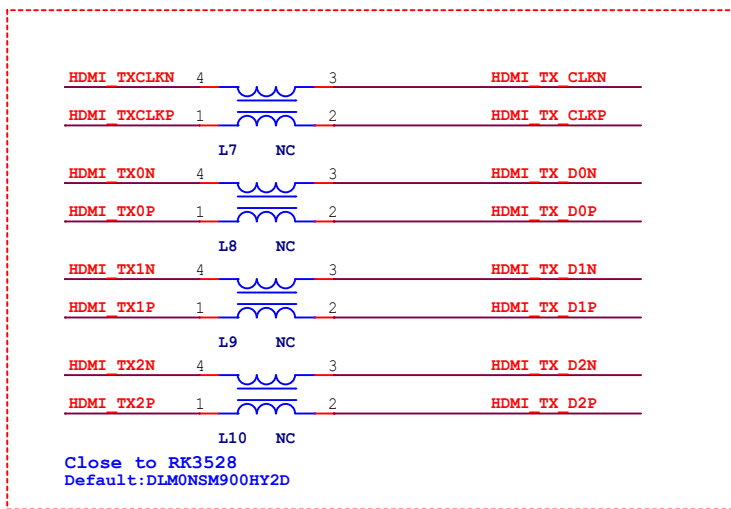
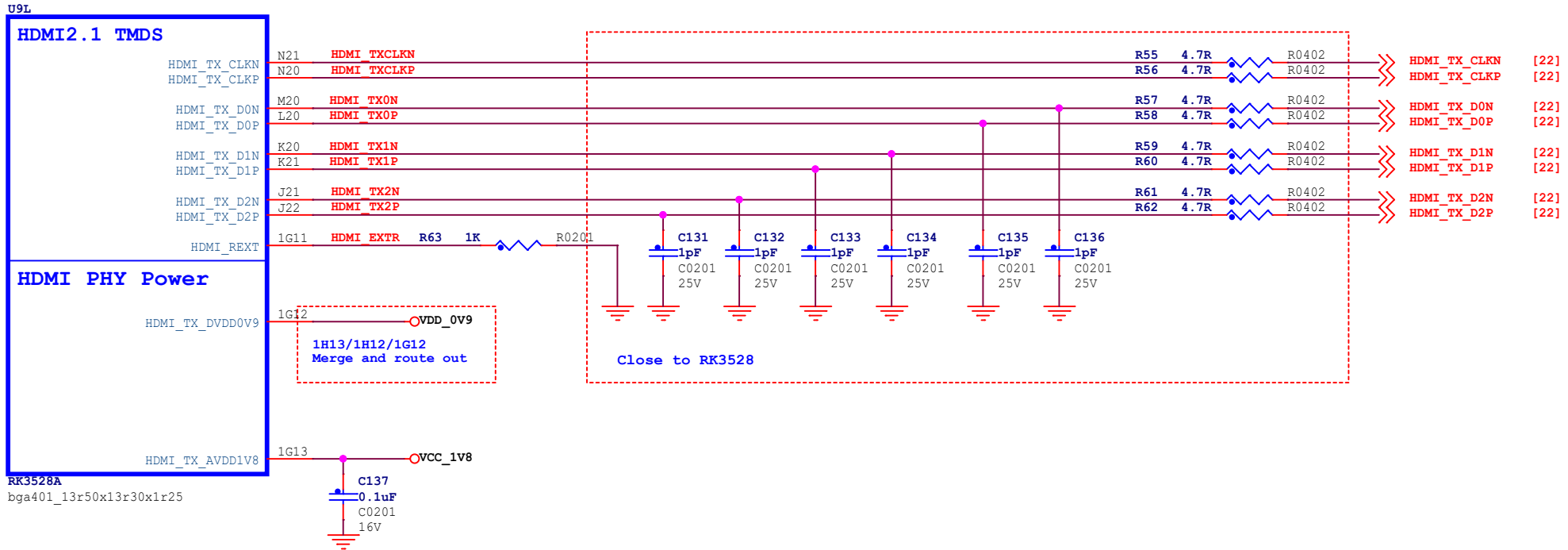
BOARD ID: 0x0001
CH2值: 170
CH3值: 288



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<https://yehuosm.tmall.com>

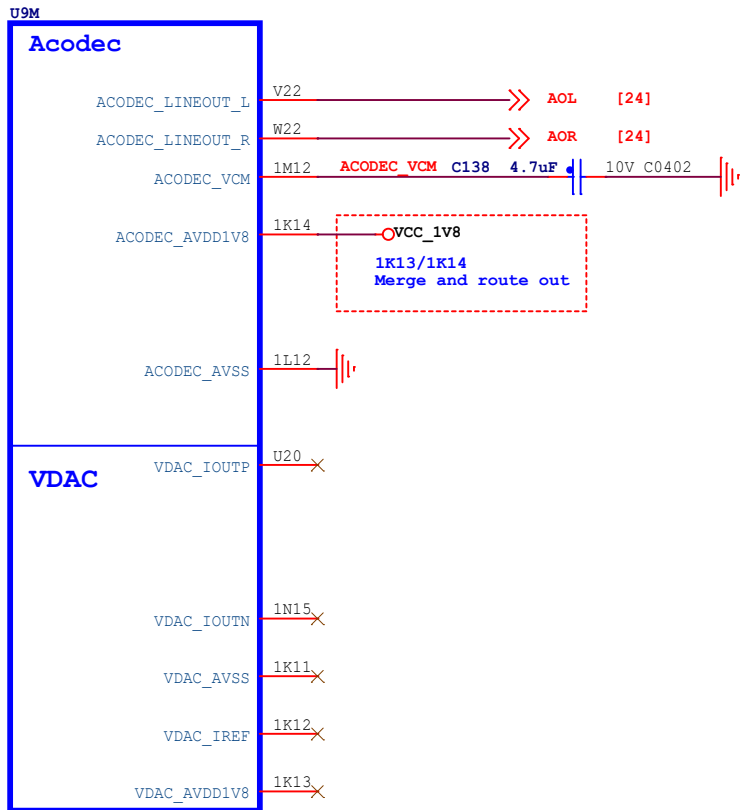
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RK3528_L (HDMI PHY)



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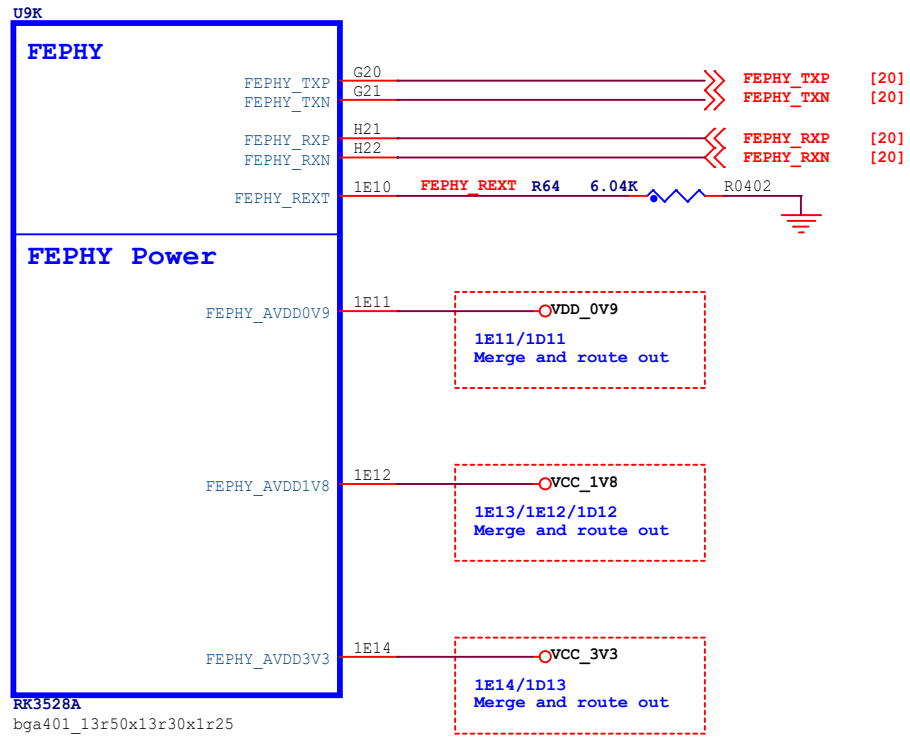
RK3528_M (Acodec/VDAC)



RK3528A
bga401_13r50x13r30x1r25

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RK3528_K (Embed FEPHY)



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RK3528_K (VCCIO0 Domain)

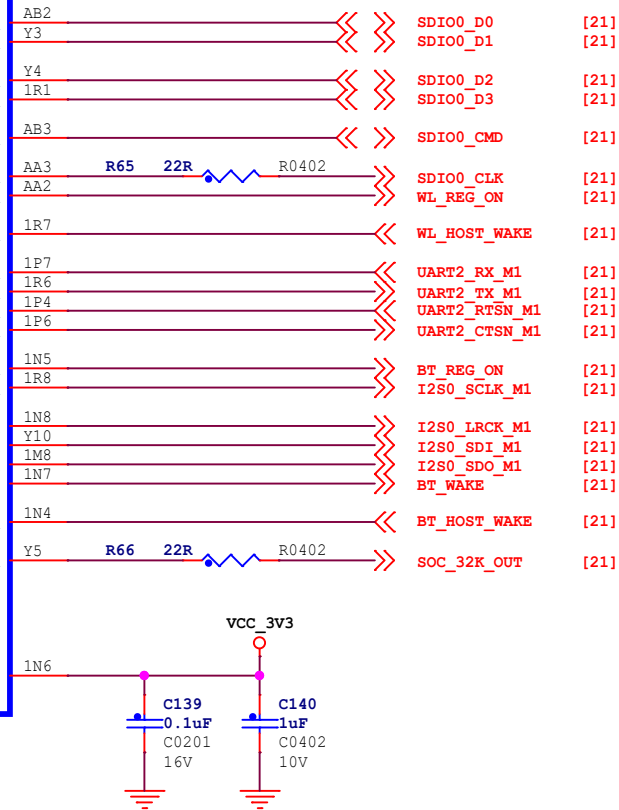
U9D

VCCIO0 Domain

Operating Voltage=1.8V/3.3V

	I2C3_SCL_M0	SCR_DET_N_M0	PCIE_CLKREQN_M1	SDIO0_D0	GPIO1_A0_d	AB2	SDIO0_D0	[21]
	I2C3_SDA_M0	SCR_DATA_M0	PCIE_WAKEN_M1	SDIO0_D1	GPIO1_A1_d	Y3	SDIO0_D1	[21]
PWM0_M1	UART5_RX_M0	SCR_CLK_M0	PCIE_PERSTN_M1	SDIO0_D2	GPIO1_A2_d	Y4	SDIO0_D2	[21]
PWM1_M1	UART5_TX_M0	SCR_RSTN_M0	--	SDIO0_D3	GPIO1_A3_d	1R1	SDIO0_D3	[21]
PWM4_M1	--	HSM_CLK_OUT_M1	--	SDIO0_CMD	GPIO1_A4_d	AB3	SDIO0_CMD	[21]
	UART5_RTSN_M0	I2C2_SCL_M1	--	SDIO0_CLK	GPIO1_A5_d	AA3	SDIO0_CLK	[21]
	UART5_CTSN_M0	I2C2_SDA_M1	--	SDIO0_DET_N	GPIO1_A6_d	AA2	WL_REG_ON	[21]
PWM2_M1	--	--	--	SDIO0_PWREN	GPIO1_A7_d	1R7	WL_HOST_WAKE	[21]
	UART7_CTSN_M1	--	--	UART2_RX_M1	GPIO1_B0_d	1P7	UART2_RX_M1	[21]
	UART7_RTSN_M1	--	--	UART2_TX_M1	GPIO1_B1_d	1R6	UART2_TX_M1	[21]
	UART7_TX_M1	I2C5_SCL_M0	--	UART2_RTSN_M1	GPIO1_B2_d	1P4	UART2_RTSN_M1	[21]
	UART7_RX_M1	I2C5_SDA_M0	--	UART2_CTSN_M1	GPIO1_B3_d	1P6	UART2_CTSN_M1	[21]
				I2S0_MCLK_M1	GPIO1_B4_d	1N5	BT_REG_ON	[21]
				I2S0_SCLK_M1	GPIO1_B5_d	1R8	I2S0_SCLK_M1	[21]
			SPI1_CLK	I2S0_LRCK_M1	GPIO1_B6_d	1N8	I2S0_LRCK_M1	[21]
			SPI1_MOSI	I2S0_SDI_M1	GPIO1_B7_d	Y10	I2S0_SDI_M1	[21]
			SPI1_MISO	I2S0_SDO_M1	GPIO1_C0_d	1M8	I2S0_SDO_M1	[21]
			SPI1_CSN0	--	GPIO1_C1_u	1N7	BT_WAKE	[21]
PWM7_M1	--	--	SPI1_CSN1	--	GPIO1_C2_d	1N4	BT_HOST_WAKE	[21]
PWM6_M1	--	SPDIF_TX_M1	--	CLK_32K_OUT_M1	GPIO1_C3_d	Y5	SOC_32K_OUT	[21]

VCCIO0_VCC



RK3528A
bga401_13r50x13r30x1r25

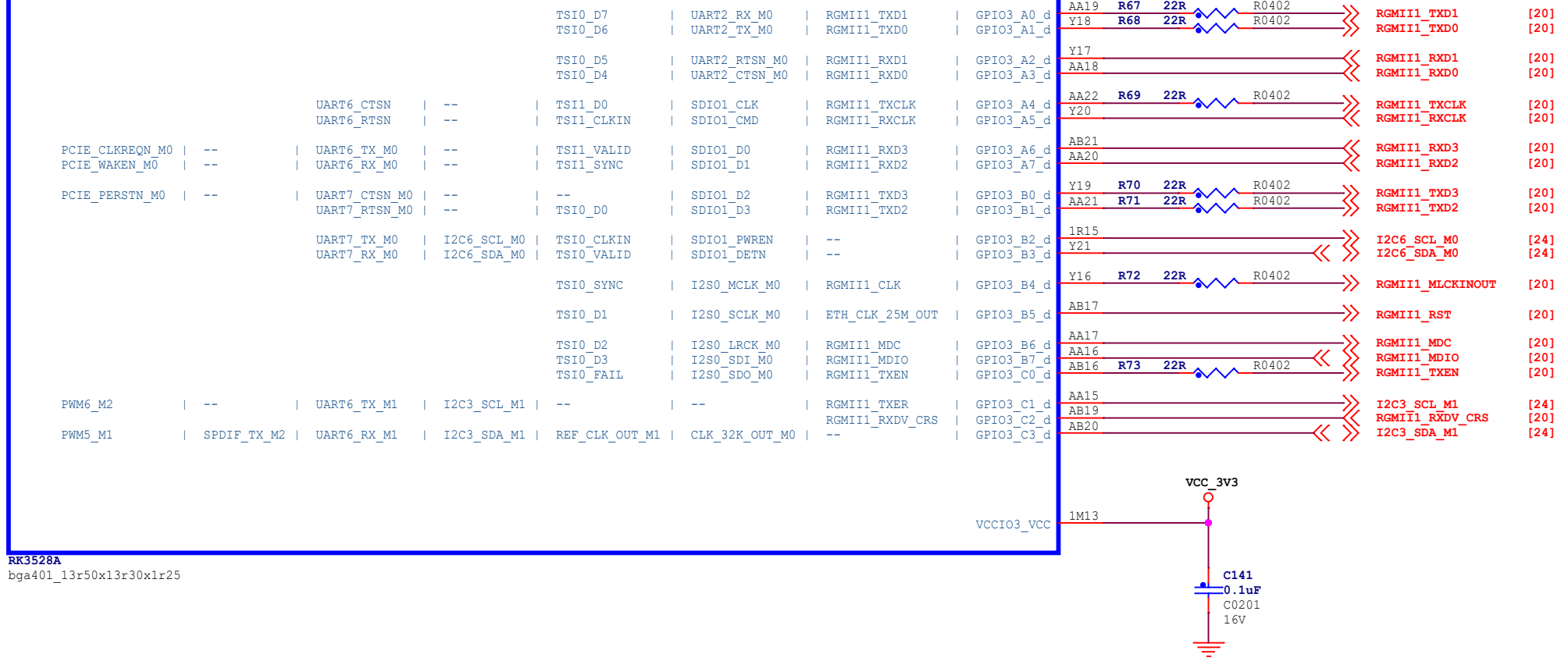
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RK3528_K (VCCIO3 Domain)

U9G

VCCIO3 Domain

Operating Voltage=1.8V/3.3V



RK3528A
bga401_13r50x13r30x1r25

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RK3528_H (VCCIO4 Domain)

U9H

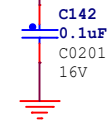
VCCIO4 Domain

Operating Voltage=1.8V/3.3V

PMU_DEBUG	--	I2C0_SDA_M1	--	SPDIF_TX_M0	--	--	GPIO4_A0_d	R3	GPIO4_A0	[24]
		I2C0_SCL_M1	--	SDMMC0_PWREN	--	--	GPIO4_A1_d	R1	GPIO4_A1	[24]
		I2C1_SDA_M0	UART3_RTSN	--	--	I2S1_SDI3	GPIO4_A2_d	U2	GPIO4_A2	[24]
		I2C1_SCL_M0	UART3_CTSN	--	--	I2S1_SDI2	GPIO4_A3_d	U3	GPIO4_A3	[24]
		UART1_CTSN	--	--	PDM_CLK1	I2S1_MCLK	GPIO4_A4_d	1M2	GPIO4_A4	[24]
		UART1_RTSN	--	--	--	I2S1_SCLK	GPIO4_A5_d	1P2	GPIO4_A5	[24]
		UART1_TX_M0	--	--	--	I2S1_LRCK	GPIO4_A6_d	1M1	UART1_TX_M0	[24]
		UART1_RX_M0	--	--	--	I2S1_SDO0	GPIO4_A7_d	1P3	UART1_RX_M0	[24]
		UART3_RX_M0	--	--	--	I2S1_SDO1	GPIO4_B0_d	1R2	GPIO4_B0	[24]
		UART3_TX_M0	--	--	PDM_SDI1	I2S1_SDO2	GPIO4_B1_d	1N2	GPIO4_B1	[24]
				SPI0_MOSI	PDM_SDI0	I2S1_SDO3	GPIO4_B2_d	1N3	SPI0_MOSI	[24]
				SPI0_MISO	PDM_SDI2	I2S1_SDI1	GPIO4_B3_d	W3	SPI0_MISO	[24]
				SPI0_CLK	--	I2S1_SDI0	GPIO4_B4_d	R2	SPI0_CLK	[24]
		FEPHY_LED_DPX_M0	--	--	PDM_CLK0	--	GPIO4_B5_d	Y1	SYS_LED	[4]
				SPI0_CSNO	--	PWR_CTRL1	GPIO4_B6_u	1L1	SPI0_CSNO	[24]
PWM4_M0	--	FEPHY_LED_SPD_M0	UART3_RX_M1	--	--	--	GPIO4_B7_d	V3	FEPHY_LED_SPD_M0	[20]
PWM5_M0	--	FEPHY_LED_LINK_M0	UART3_TX_M1	--	--	--	GPIO4_C0_d	Y2	FEPHY_LED_LINK_M0	[20]
PWM6_M0	--	--	--	SPI0_CSNO	PDM_SDI3	--	GPIO4_C1_d	W2	PWM6_M0	[24]
PWM7_M0	--	--	--	--	--	PWR_CTRL0	GPIO4_C2_d	P3	PWM7_M0	[4]
PWM0_M0	--	--	--	GPU_AVS	--	I2C0_SDA_M0	GPIO4_C3_d	1N1	PWM0_M0	[24]
PWM1_M0	--	--	--	ARM_AVS	--	I2C0_SCL_M0	GPIO4_C4_d	V1	PWM1_M0_ARM	[5]
PWM2_M0	--	UART1_TX_M1	--	--	--	I2C1_SCL_M1	GPIO4_C5_d	1P1	PWM2_M0_LOGIC	[5]
PWM3_M0	--	UART1_RX_M1	--	--	--	I2C1_SDA_M1	GPIO4_C6_d	AA1	PWM3_IR_RX	[24]
		UART0_RX_M0	JTAG_MCU_TMS_M1	JTAG_CPU_TMS_M1	--	--	GPIO4_C7_u	T3	UART0_RX_M0	[24]
		UART0_TX_M0	JTAG_MCU_TCK_M1	JTAG_CPU_TCK_M1	--	--	GPIO4_D0_d	T2	UART0_TX_M0	[24]

VCCIO4_VCC

1J3 VCC_3V3



RK3528A

bga401_13r50x13r30x1r25

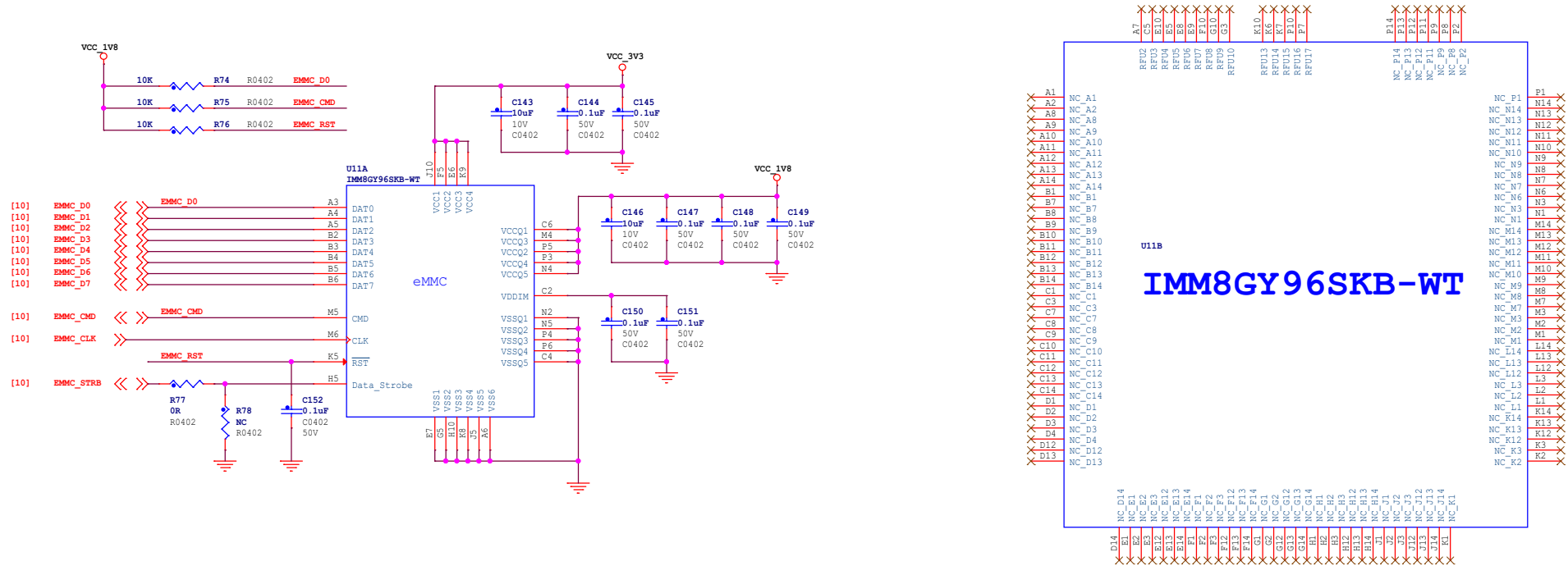
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Title
野火_RK3528_LUBANCAT_Q1_原理图

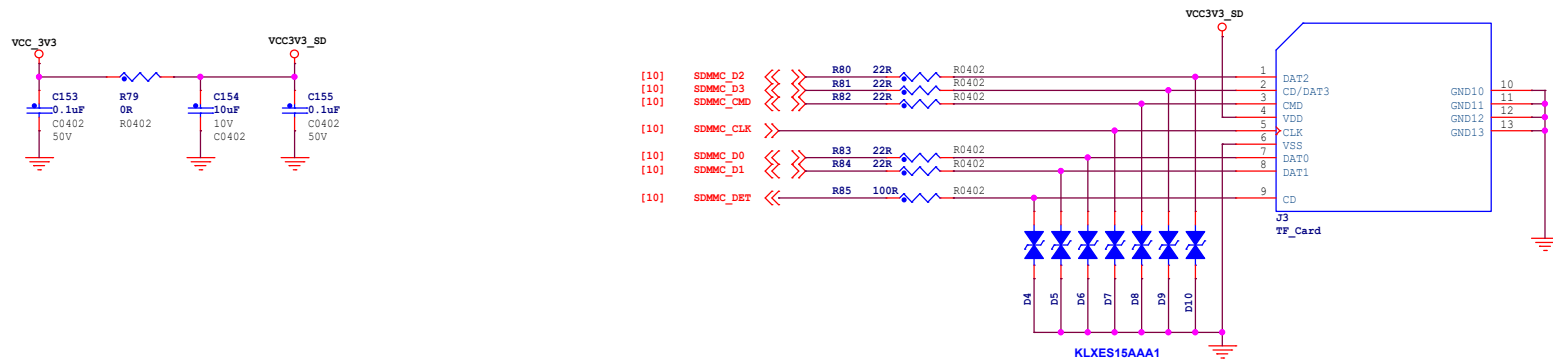
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EMMC FLASH



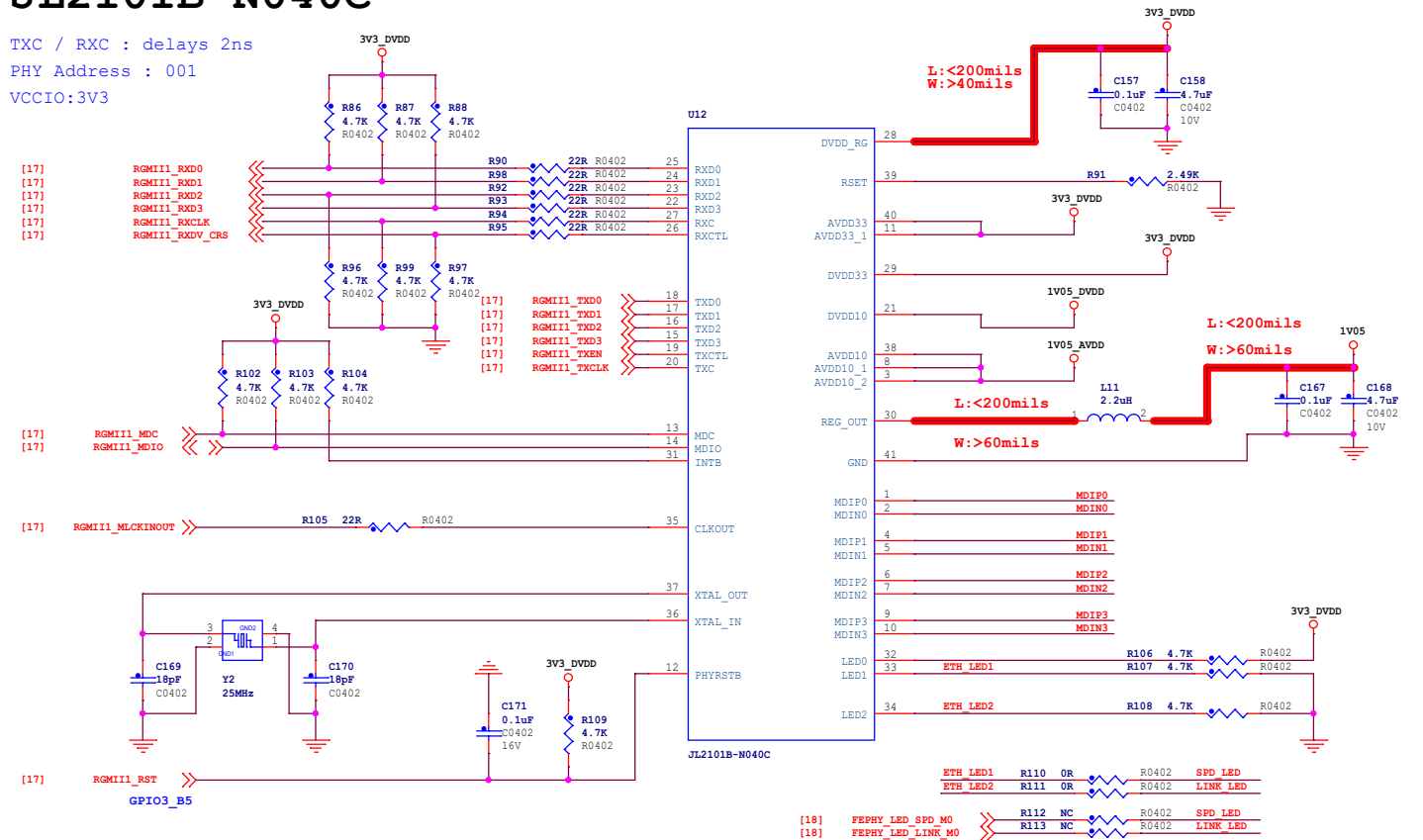
TF Card



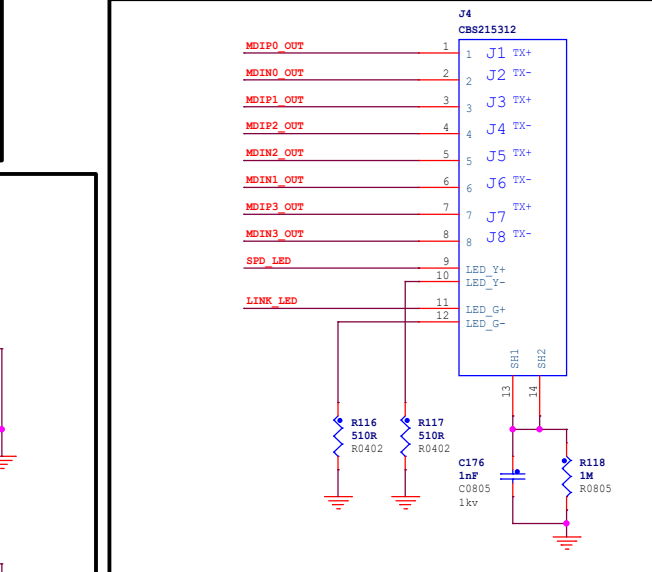
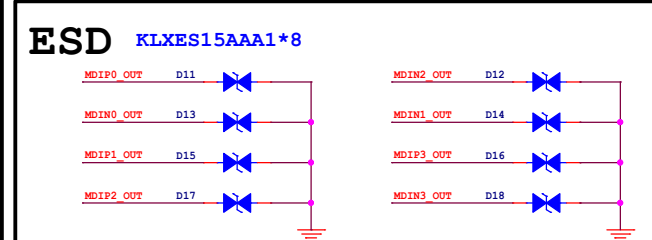
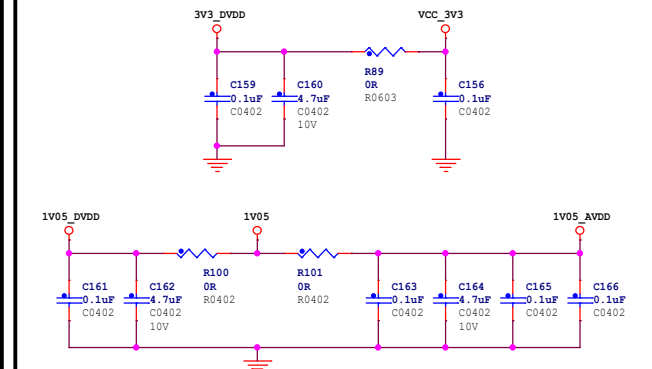
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Title 野火_RK3528_LUBANCAT_Q1_原理图		
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JL2101B-N040C

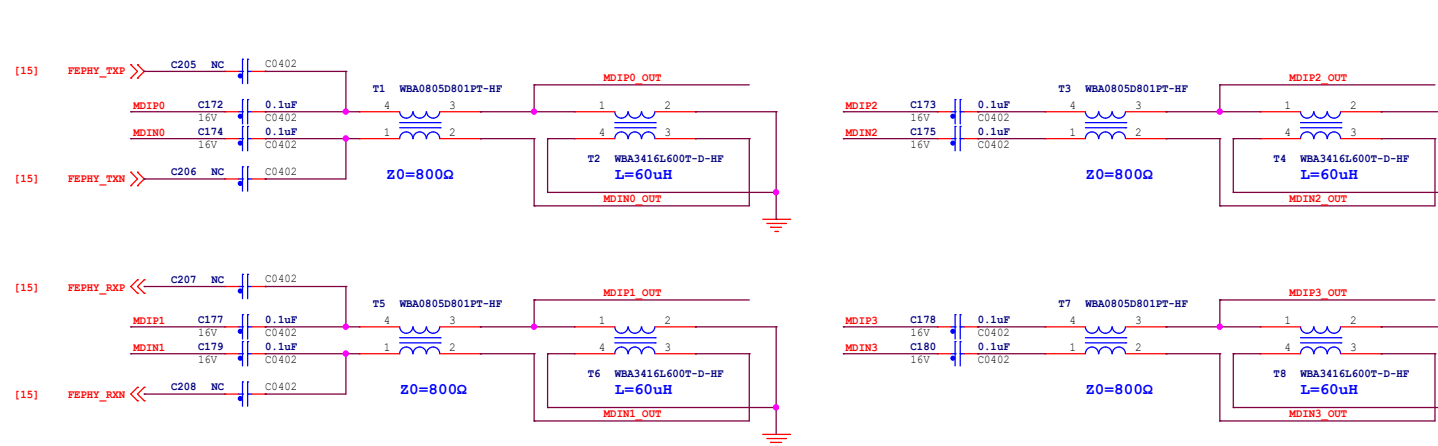
TXC / RXC : delays 2ns
PHY Address : 001
VCCIO:3V3



Power Filter

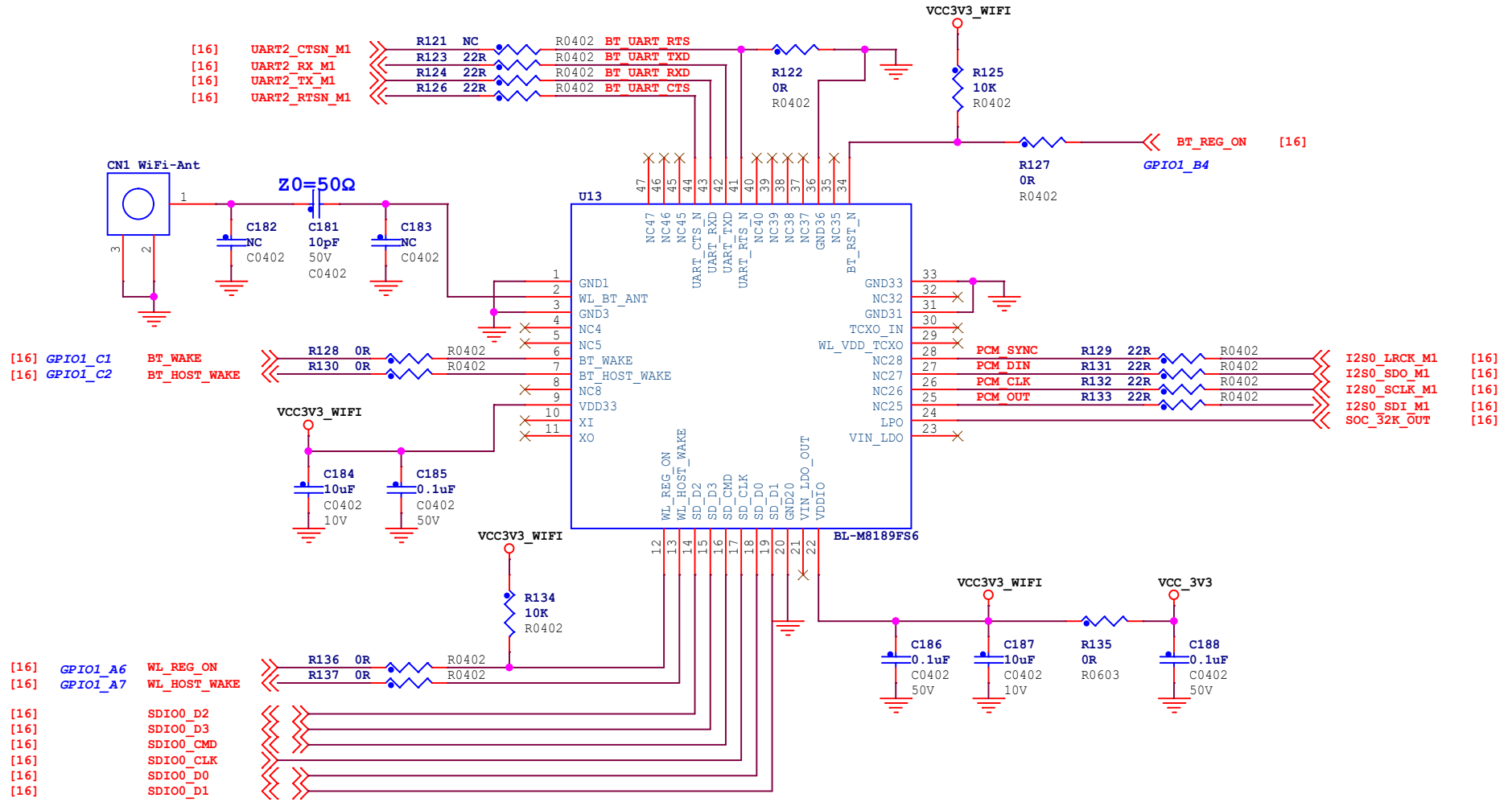


Chip LAN



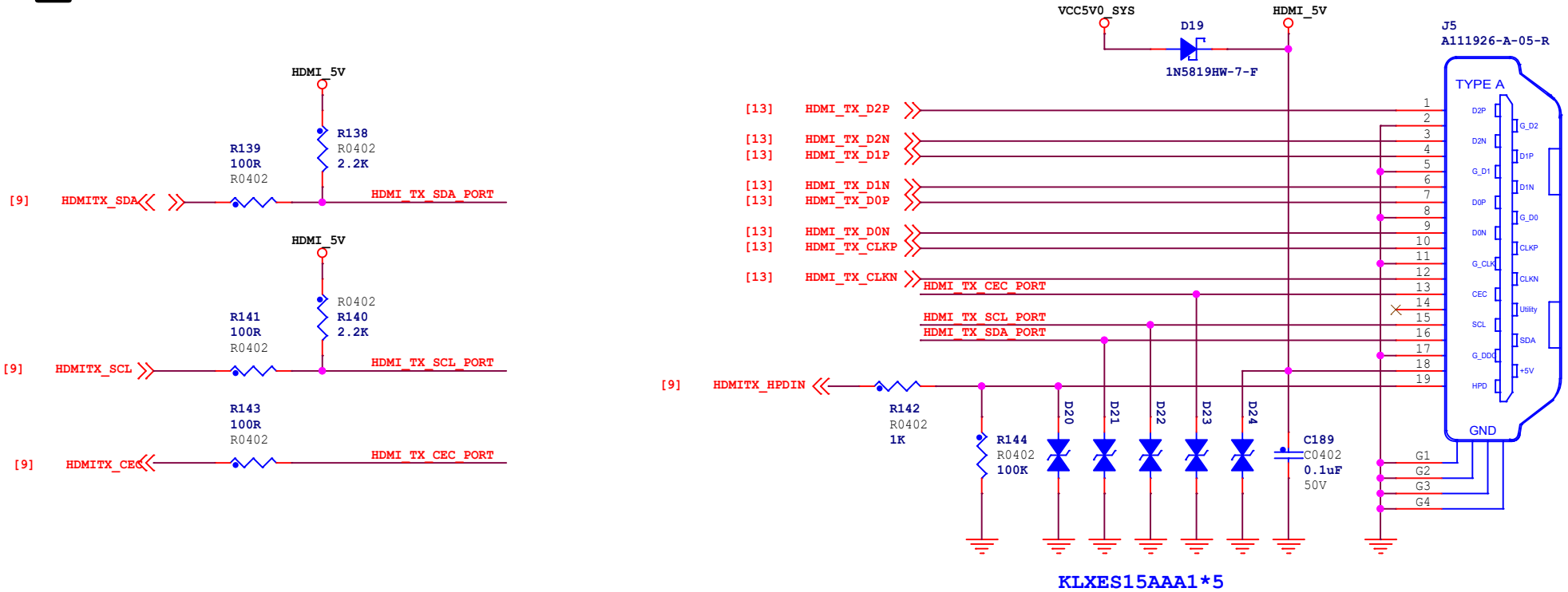
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Title	野火_RK3528_LUBANCAT_q1_原理图	
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A3	ETH_ChipLAN	V1R0
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WLAN

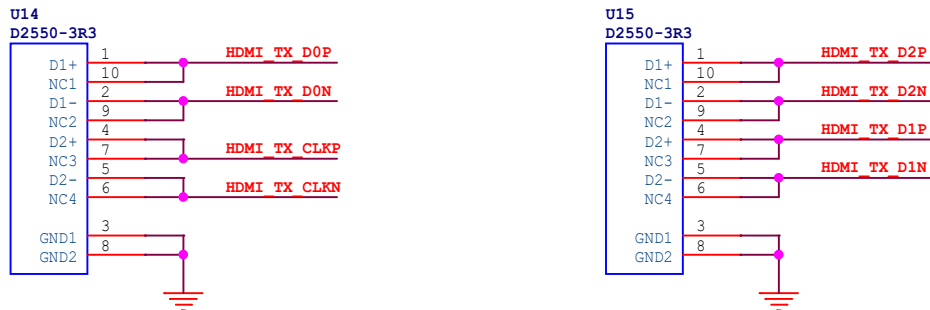


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Title 野火_RK3528_LUBANCAT_Q1_原理图		
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HDMI_PORT

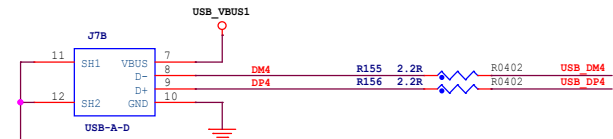
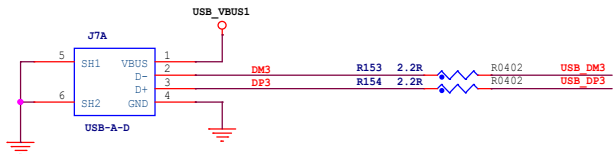
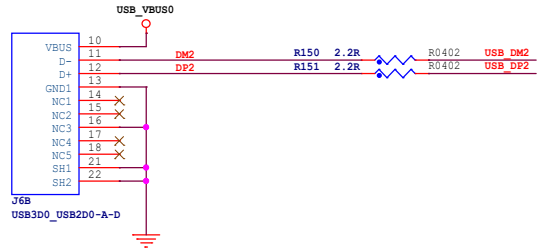
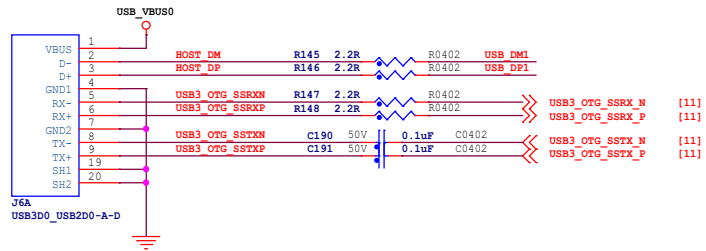


HDMI_ESD

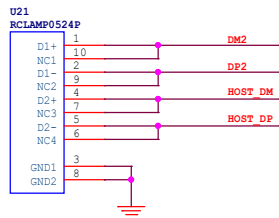
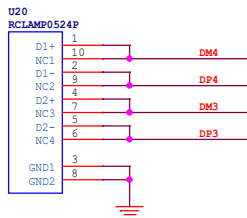
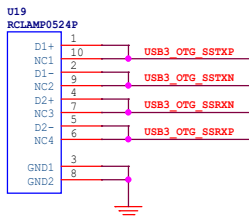


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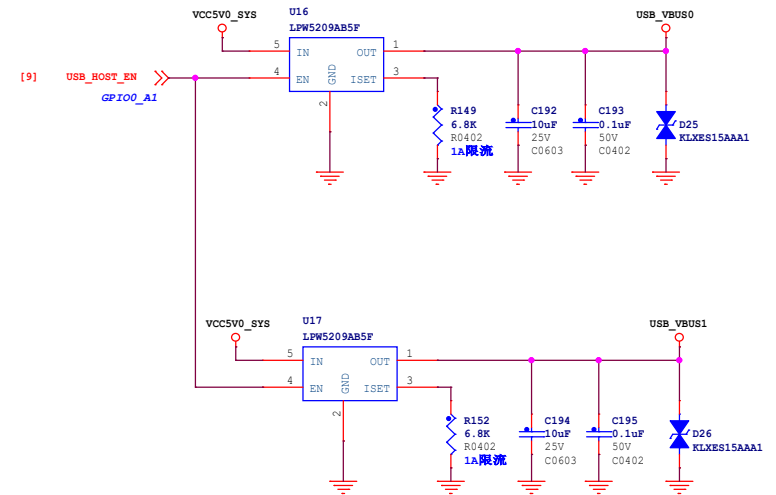
USB 30 / 20 PORT



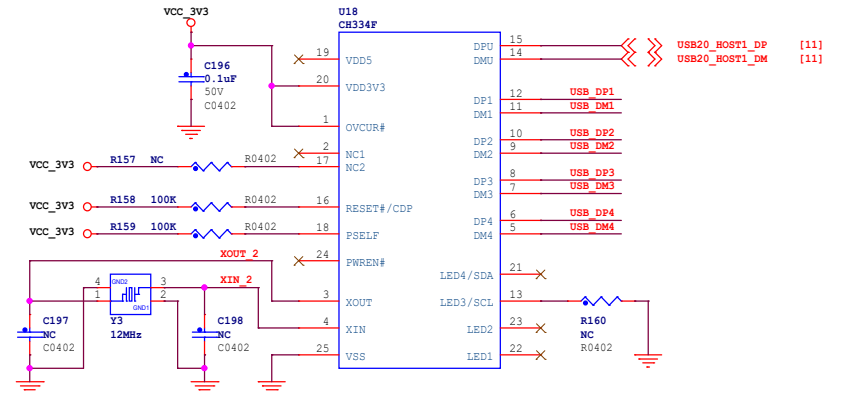
ESD



USB POWER

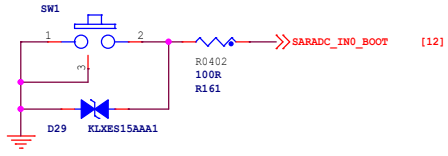


USB HUB

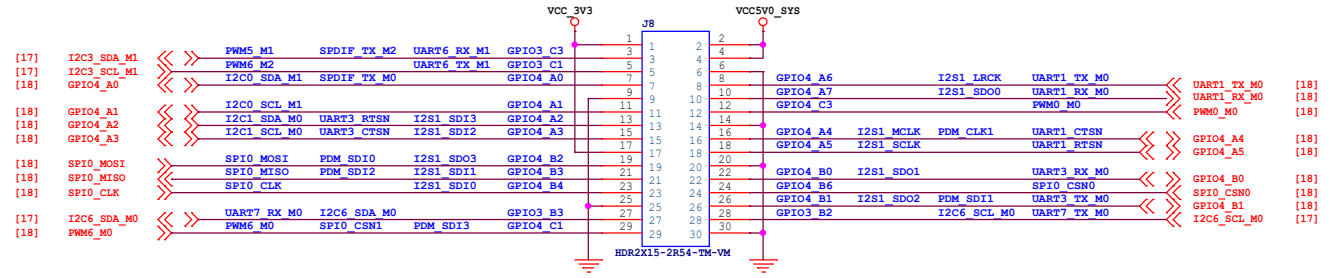


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BOOT KEY

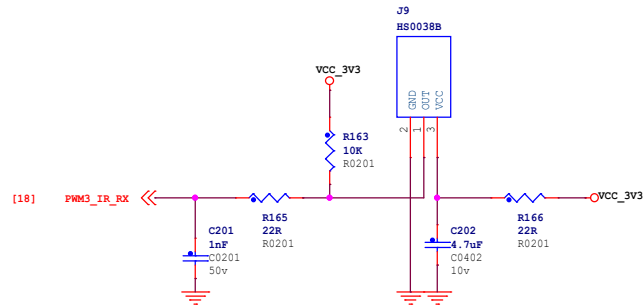


Pin Out

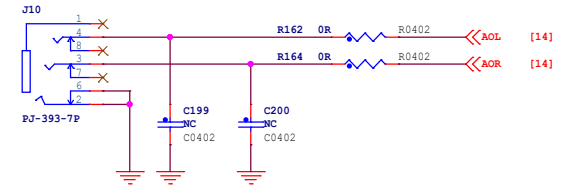


Only Support 3.3V

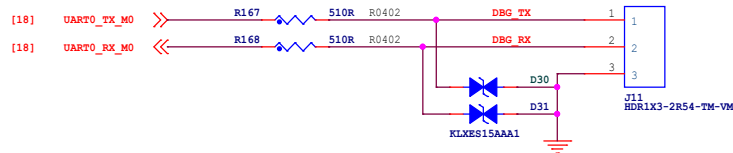
IR_INPUT



Earphone



Debug UART2



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Title	野火_RK3528_LUBANCAT_Q1_原理图	
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