

野火 EBF RK3568 BTB 核心板

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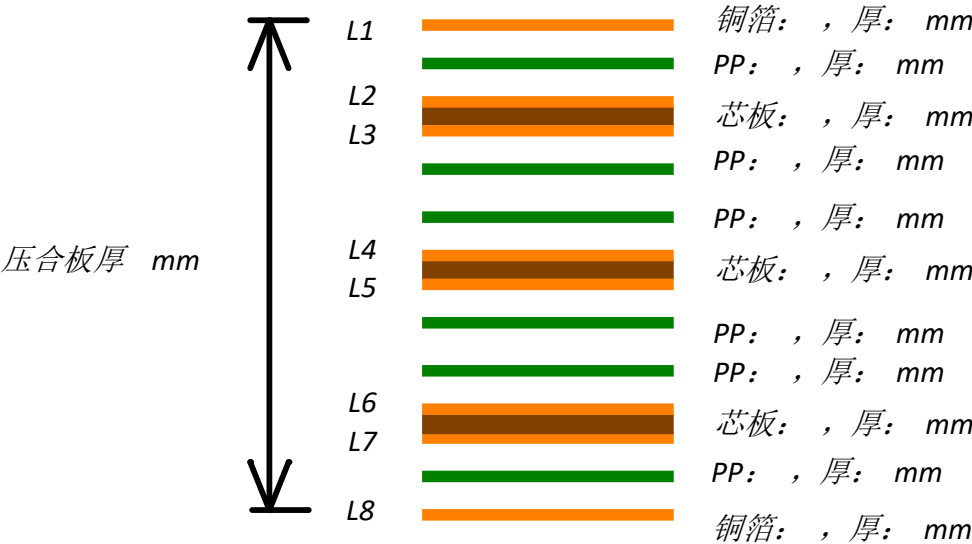
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Title 野火 EBF RK3568 BTB核心板		
Size A4	Document Number 目录	Rev V1.0
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历史版本

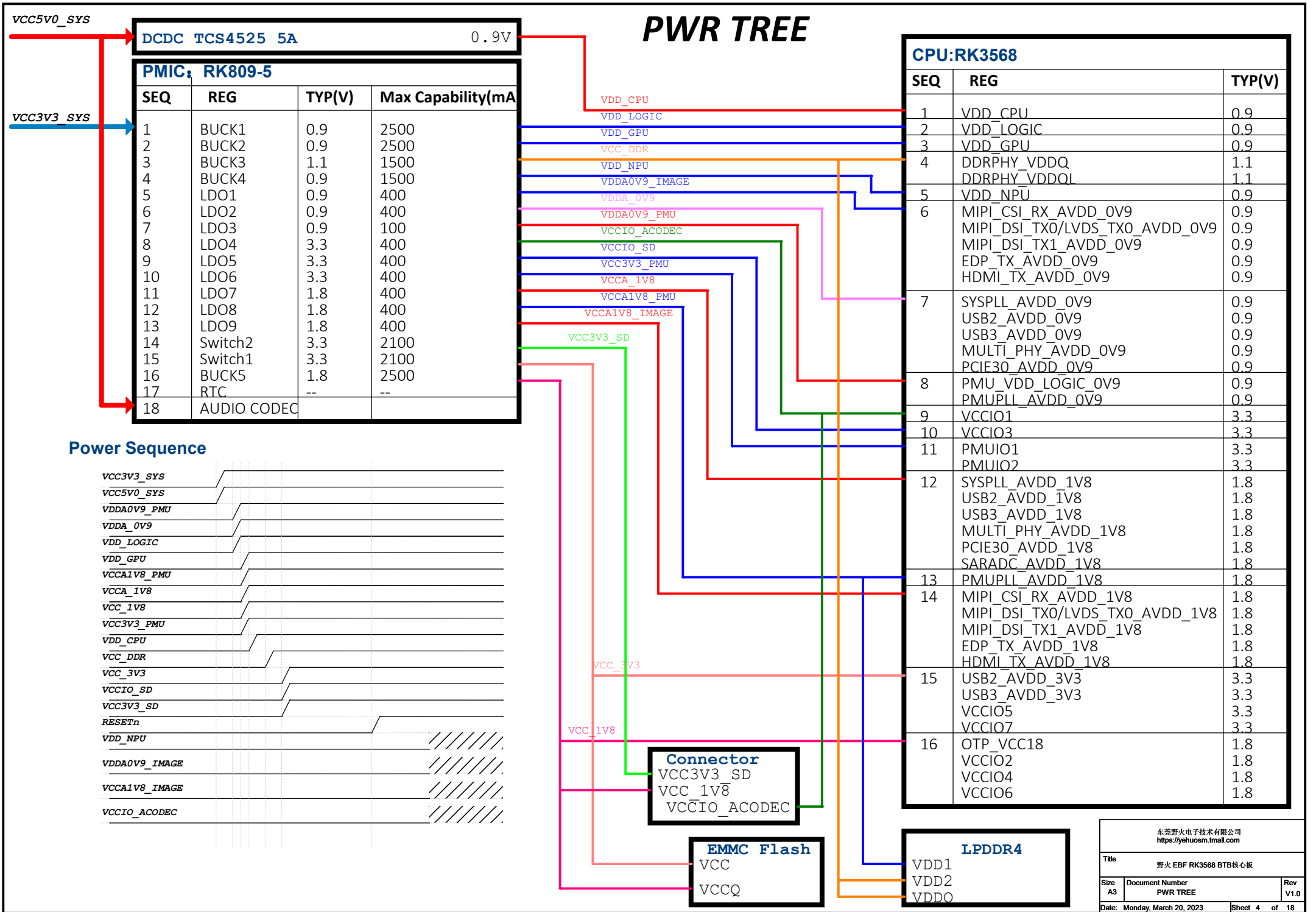
版本号	日期	设计	描述
V1.0	2021-10-15	llm	初始版本, 开发阶段
V1.1	2021-11-26	llm	预留LPDDR4 1.8V LDO单独供电
V1.2	2021-12-07	llm	Connector引脚网络对调如下: 1.203与205引脚网络对调 2.33与35引脚网络对调 3.107与109引脚网络对调 4.141与143引脚网络对调 5.217与219引脚网络对调
V1.3	2022-07-07	llm	1.把定位孔改为M3的定位孔，数量改为2个 2.增加LPDDR4x兼容电路 3.金手指去掉VCC_3V3引出

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ebf_rk3568 core board



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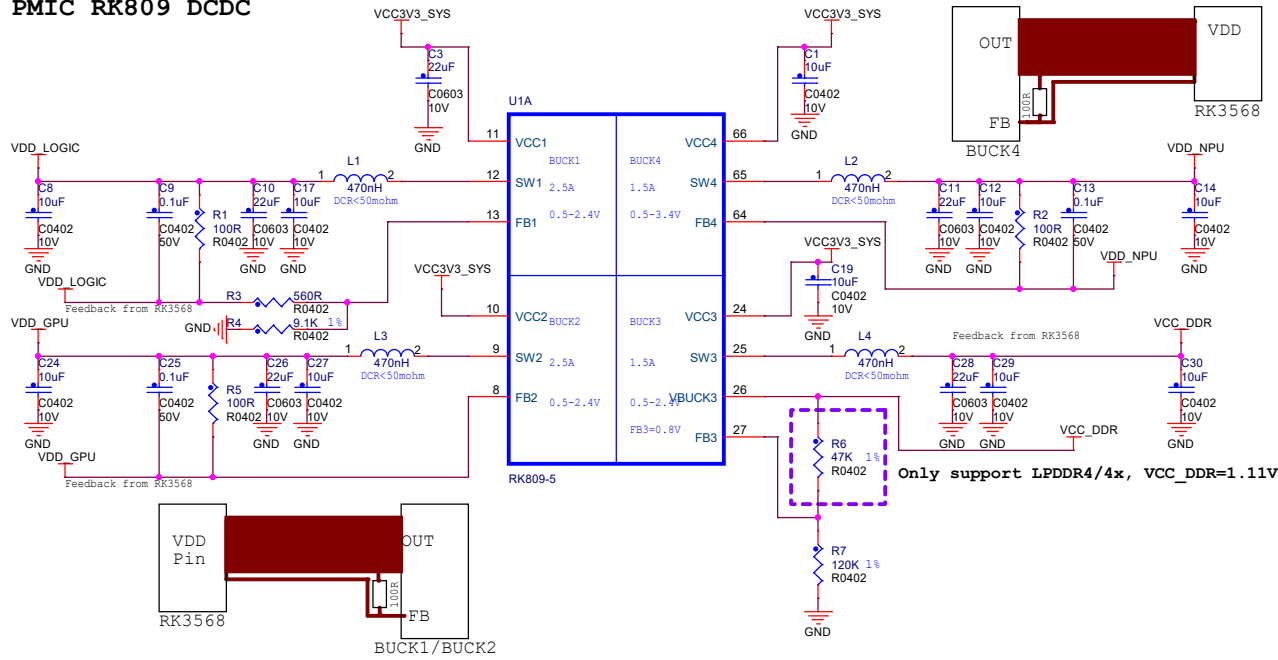
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https://yehuosm.tmall.com

Title
野火 EBF RK3568 BTB核心板

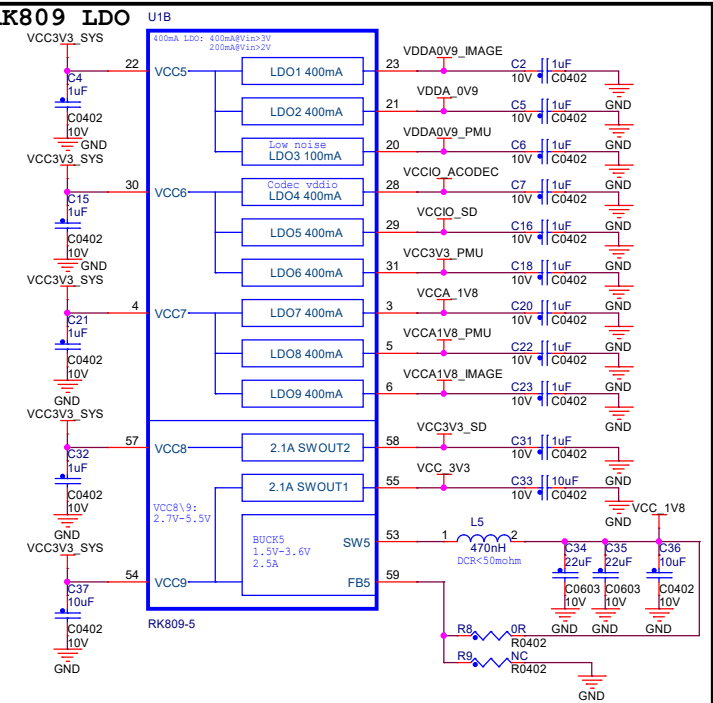
Size A3 Document Number PWR TREE Rev V1.0

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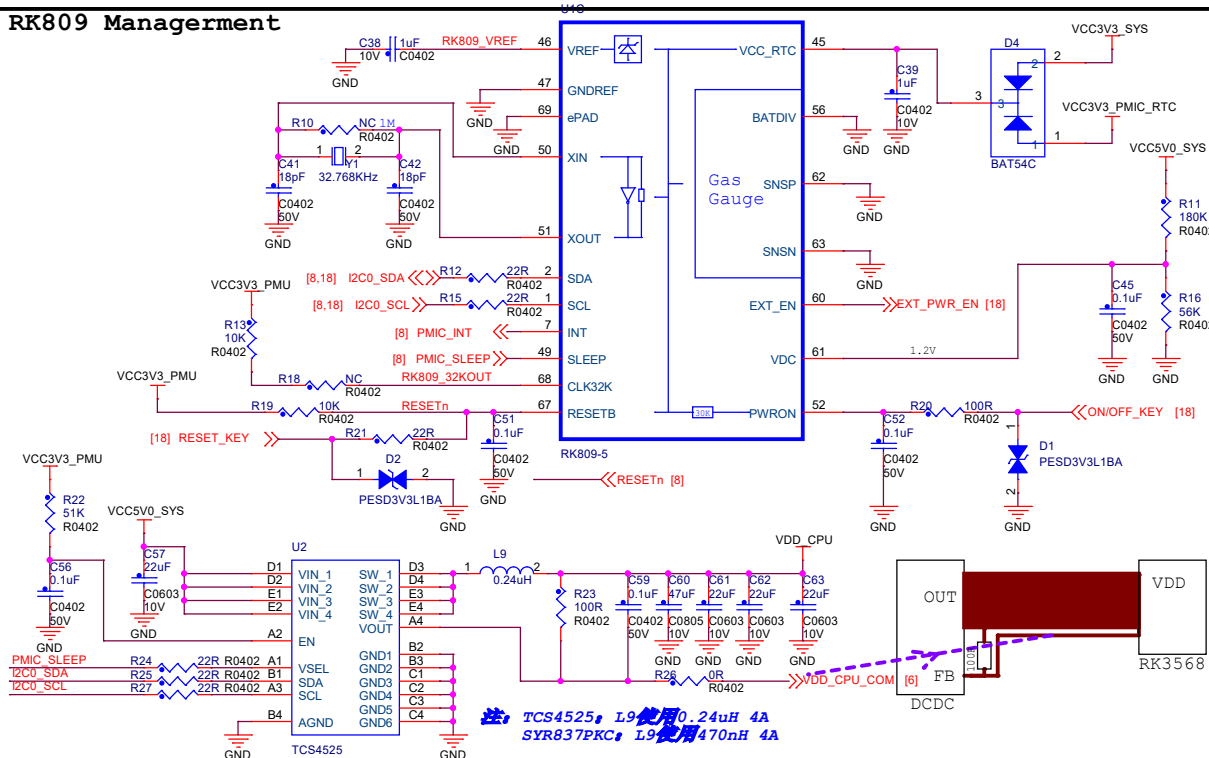
PMIC RK809 DCDC



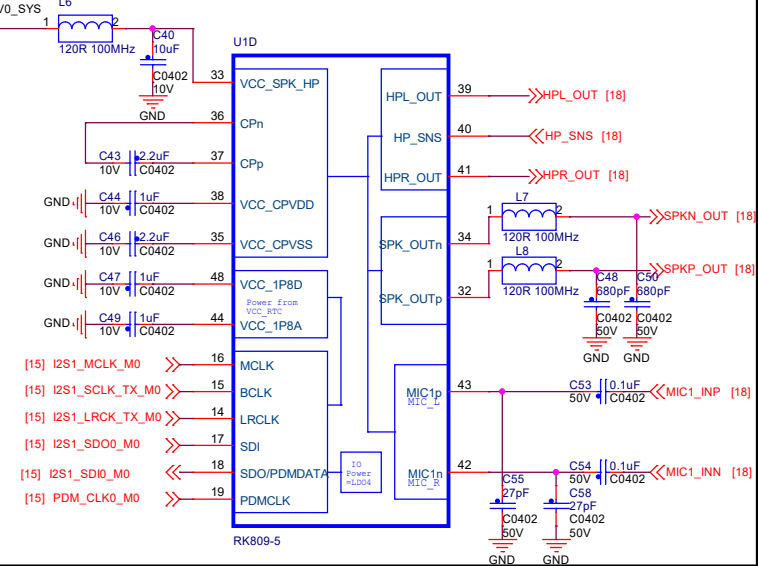
PMIC RK809 LDO



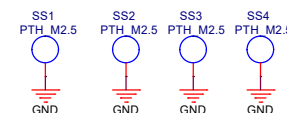
PMIC RK809 Management



PMIC RK809 CODEC

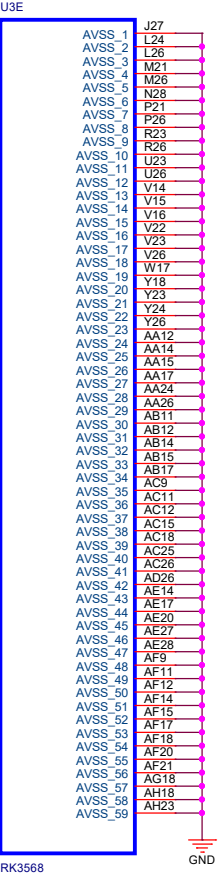
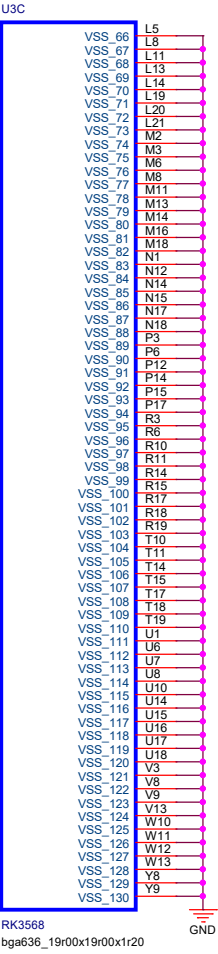
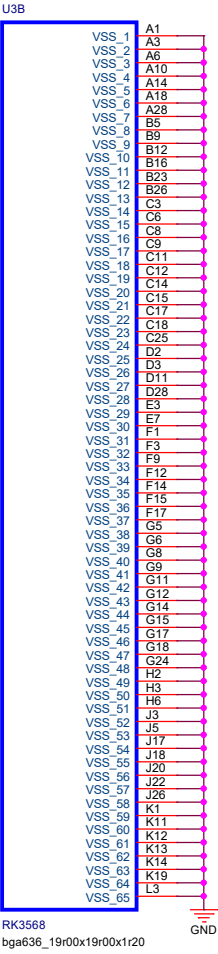
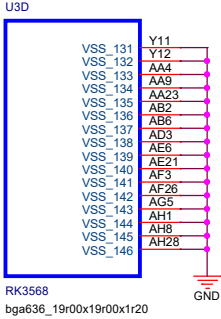
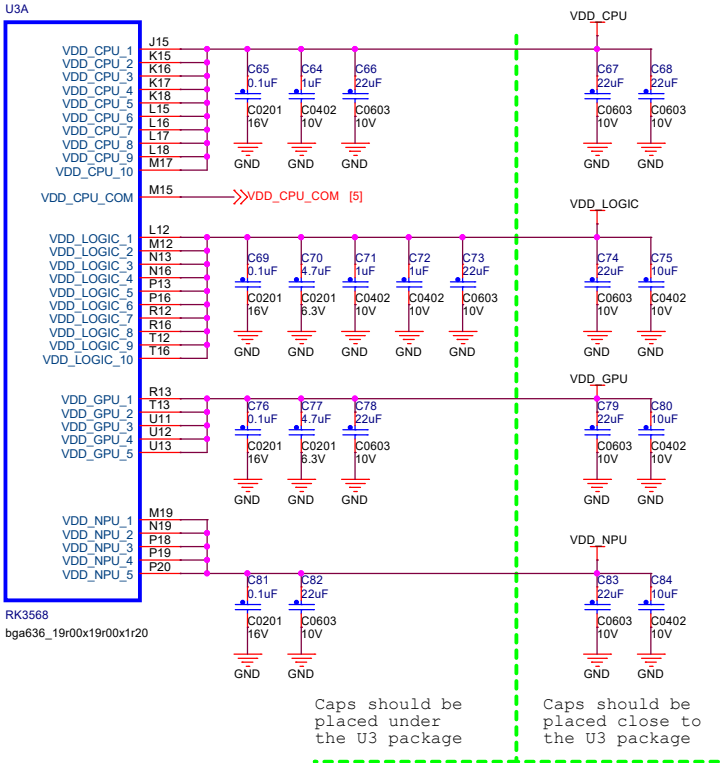


定位孔

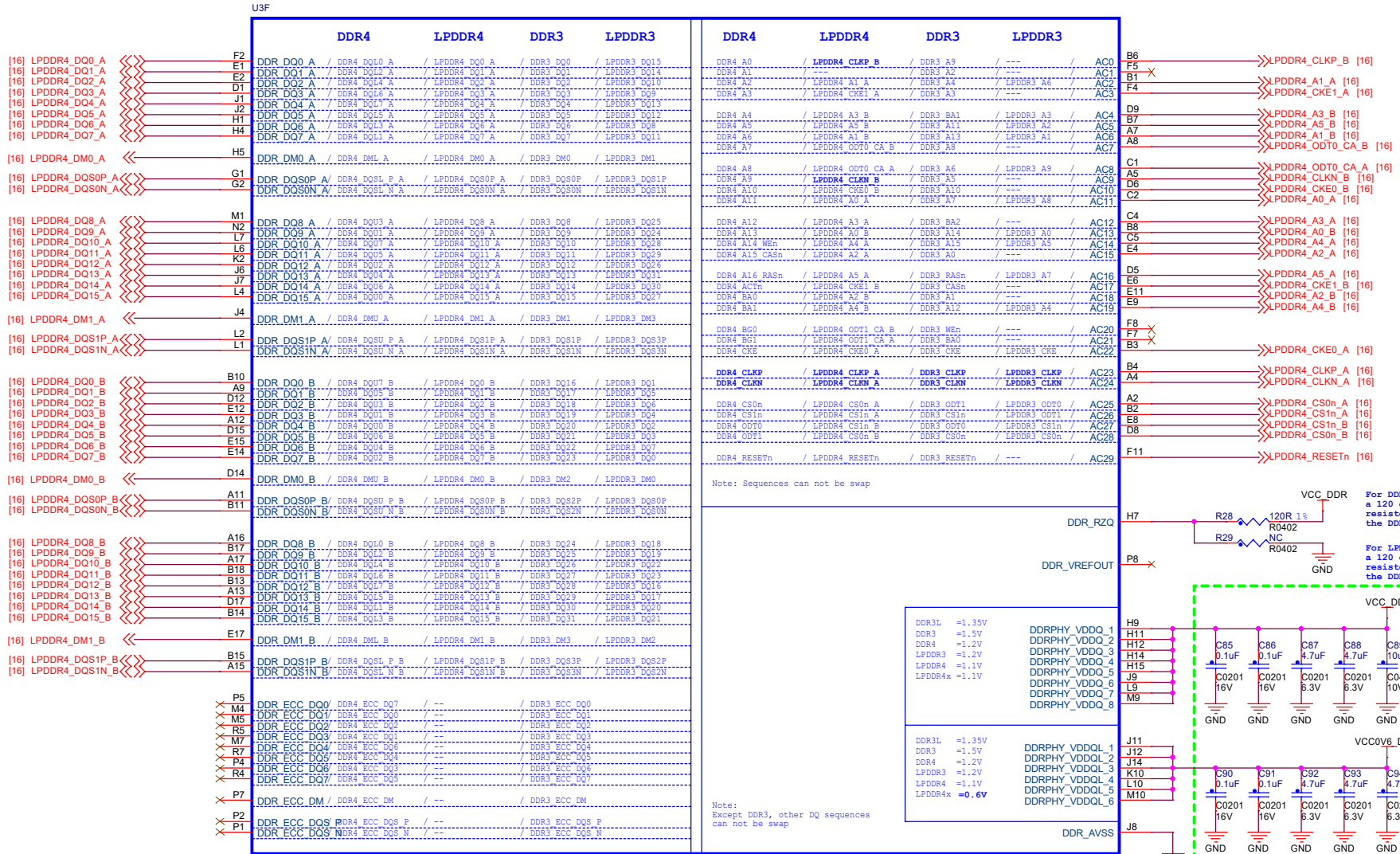


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Size A3	Document Number SYS PMIC	Rev V1.0
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RK3568 PWR

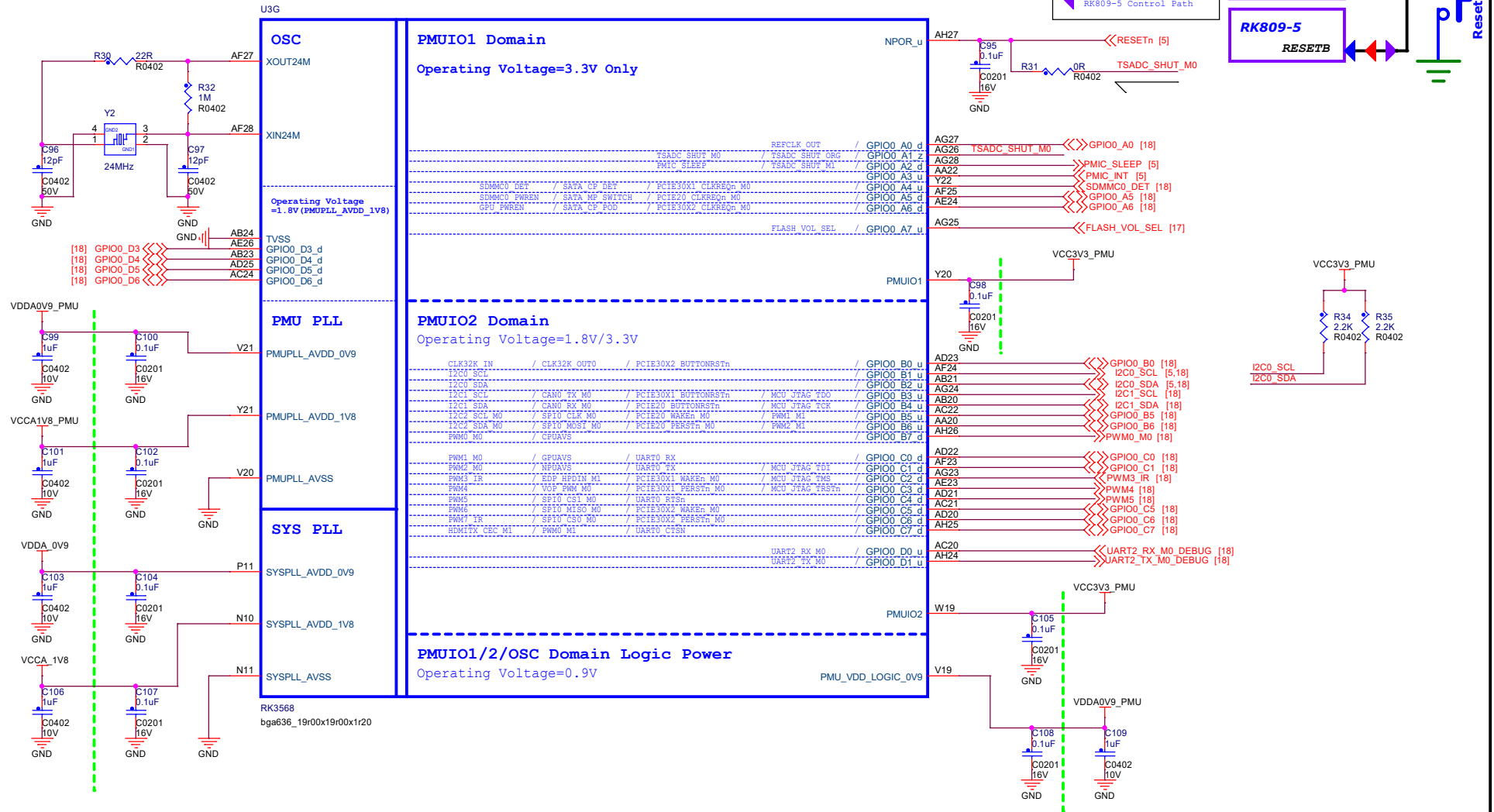


RK3568 DDR PHY



RK3568
bga636_19r00x19r00x1r20

RK3568 OSC/PLL/PMUIO

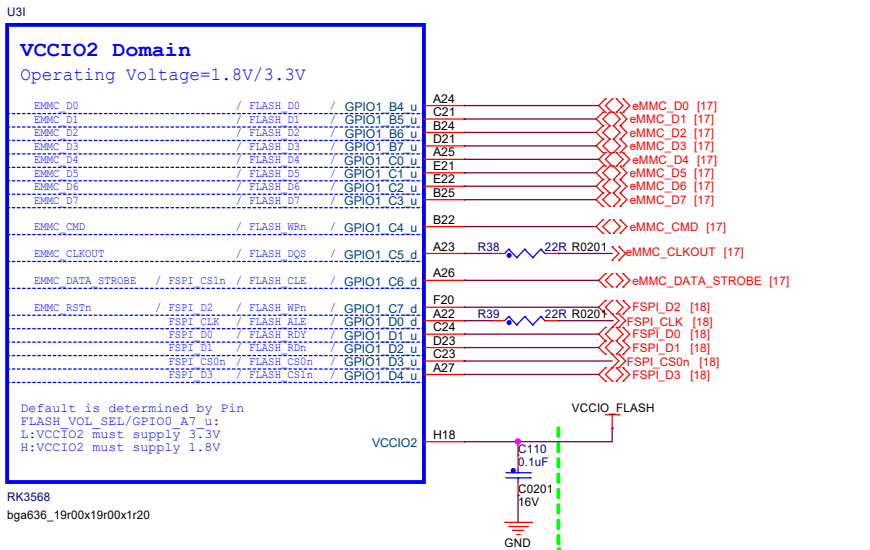


Note:

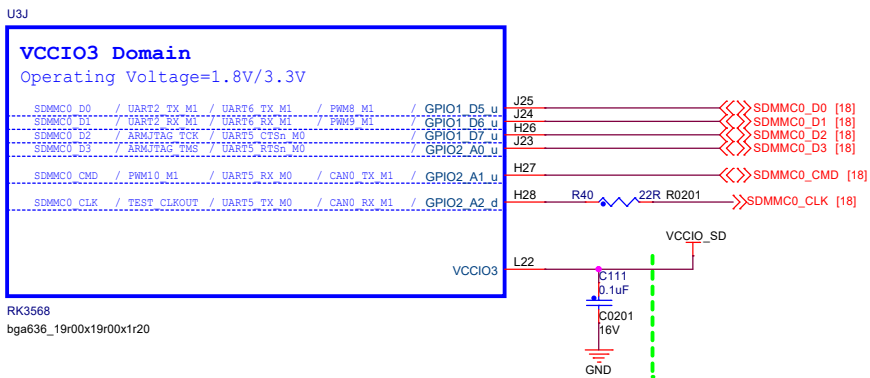
Caps of between dashed green lines and U3 should be placed under the U3 package.
Other caps should be placed close to the U3 package

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Title 野火 EBF RK3568 BTB核心板		
Size A3	Document Number OSC/PLL/PMUIO	Rev V1.0
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RK3568 VCCIO2 Domain



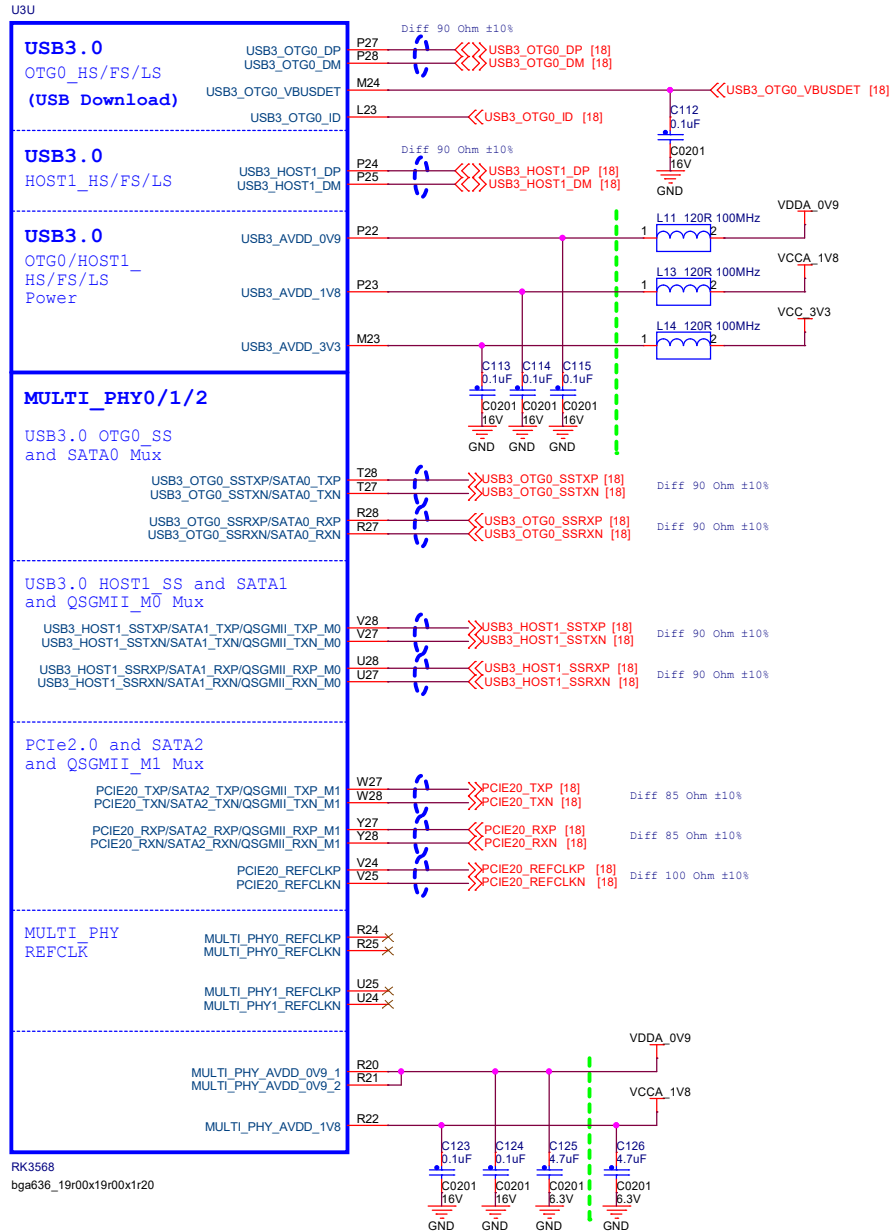
RK3568 VCCIO3 Domain



Note:
Caps of between dashed green lines and U3 should be placed under the U3 package.
Other caps should be placed close to the U3 package

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Size A3	Document Number SARADC/GPIO	Rev V1.0
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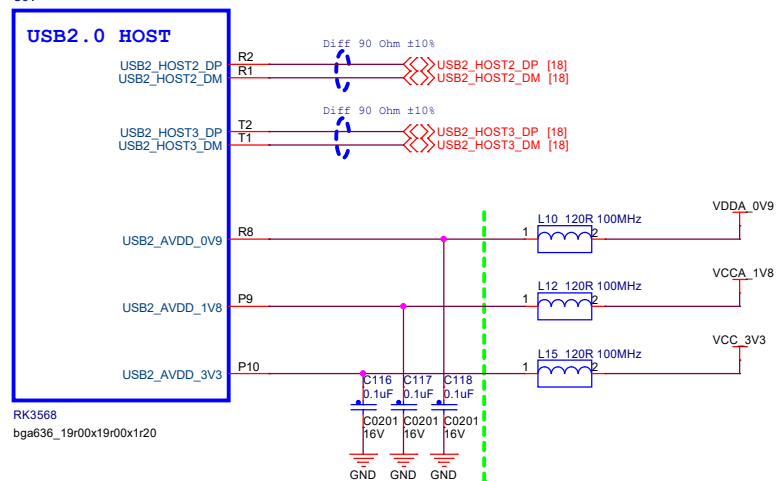
RK3568 USB3.0/SATA/QSGMII/PCIE2.0 x1



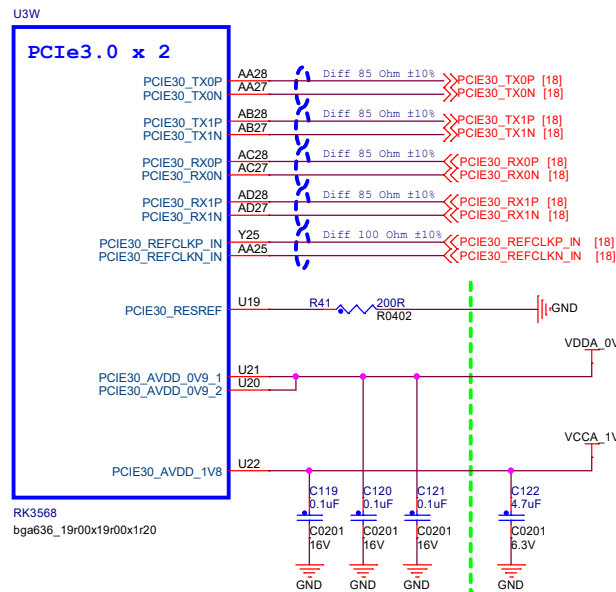
Note:

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RK3568 USB2.0 HOST



RK3568 PCIE3.0 x2



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野火 EBF RK3568 BTB核心板

Size A3 Document Number USB/PCIE/STAT PHY Rev V1.0

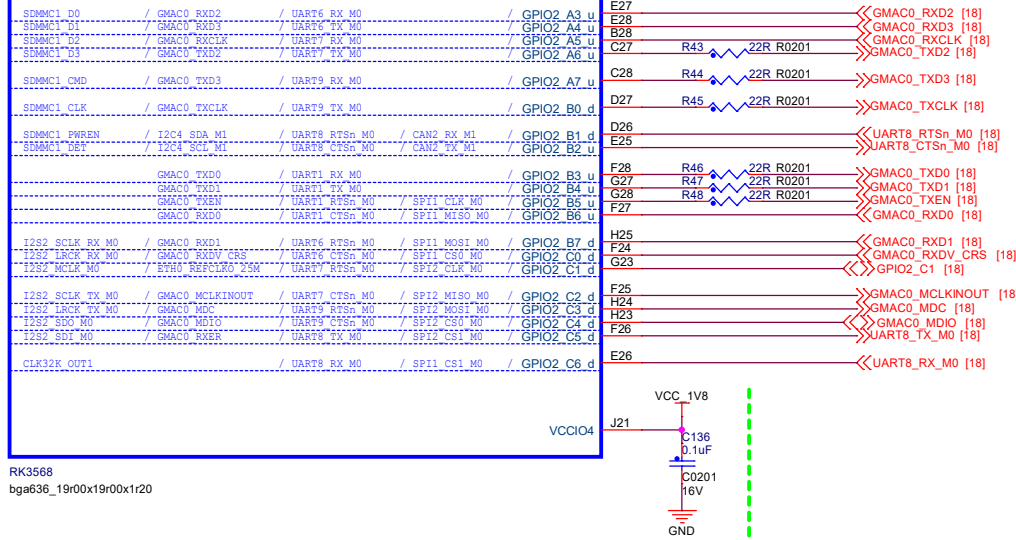
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RK3568 VCCIO4 Domain

U3K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V



RK3568

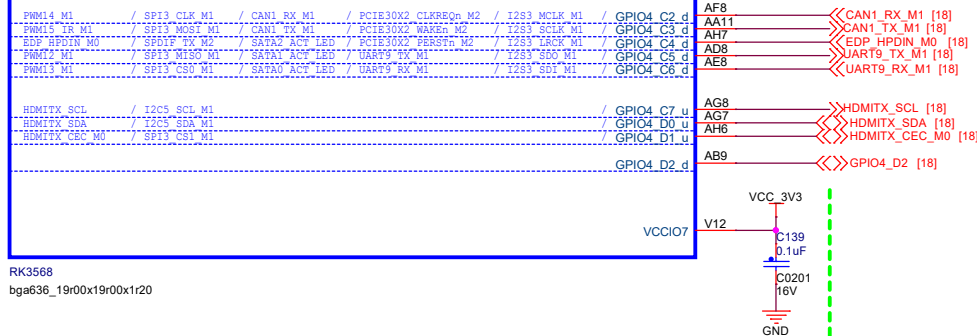
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RK3568 VCCIO7 Domain

U3N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V



RK3568

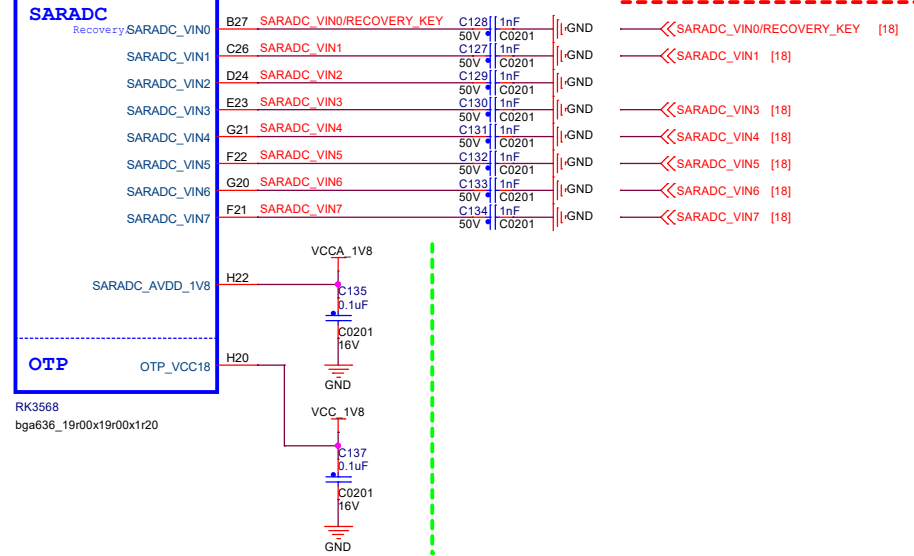
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Note:

Caps of between dashed green lines and U3 should be placed under the U3 package. Other caps should be placed close to the U3 package

RK3568 SARADC/OTP

U3O



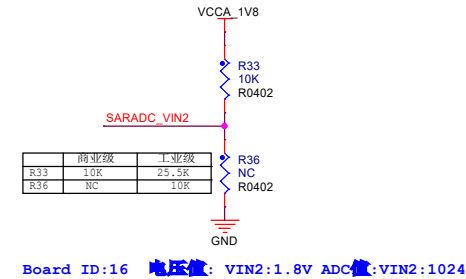
RK3568

bga636_19r00x19r00x1r20

Note:

Must be mounted

SARADC_VIN0/RECOVERY_KEY



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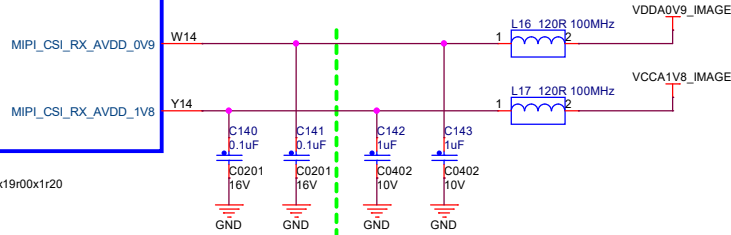
RK3568 MIPI_CSI_RX

U3P

MIPI CSI RX

MIPI_CSI_RX_D0P	AG12	Diff 100 Ohm ±10%	MIPI_CSI_RX_D0P [18]
MIPI_CSI_RX_D0N	AH12		MIPI_CSI_RX_D0N [18]
MIPI_CSI_RX_D1P	AG11	Diff 100 Ohm ±10%	MIPI_CSI_RX_D1P [18]
MIPI_CSI_RX_D1N	AH11		MIPI_CSI_RX_D1N [18]
MIPI_CSI_RX_D2P	AE11	Diff 100 Ohm ±10%	MIPI_CSI_RX_D2P [18]
MIPI_CSI_RX_D2N	AD11		MIPI_CSI_RX_D2N [18]
MIPI_CSI_RX_D3P	AD9	Diff 100 Ohm ±10%	MIPI_CSI_RX_D3P [18]
MIPI_CSI_RX_D3N	AE9		MIPI_CSI_RX_D3N [18]
MIPI_CSI_RX_CLK0P	AG10	Diff 100 Ohm ±10%	MIPI_CSI_RX_CLK0P [18]
MIPI_CSI_RX_CLK0N	AH10		MIPI_CSI_RX_CLK0N [18]
MIPI_CSI_RX_CLK1P	AG9	Diff 100 Ohm ±10%	MIPI_CSI_RX_CLK1P [18]
MIPI_CSI_RX_CLK1N	AH9		MIPI_CSI_RX_CLK1N [18]

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1



RK3568
bga636_19r00x19r00x1r20

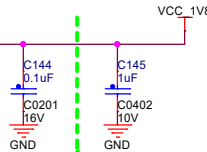
RK3568 VCCIO6 Domain

U3M

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

CIF_D0	/ EBC SDD00	/ SDMMC2_D0_M0	/ I2S1_MCLK_M1	/ VOP BT656_D0_M1	/ GPIO3_C6_d	AC5		>SDMMC2_D0_M0 [18]
CIF_D1	/ EBC SDD01	/ SDMMC2_D1_M0	/ I2S1_SCLK_TX_M1	/ VOP BT656_D1_M1	/ GPIO3_C7_d	AA6		>SDMMC2_D1_M0 [18]
CIF_D2	/ EBC SDD02	/ SDMMC2_D2_M0	/ I2S1_LCLK_RX_M1	/ VOP BT656_D2_M1	/ GPIO3_D0_d	AB5		>SDMMC2_D2_M0 [18]
CIF_D3	/ EBC SDD03	/ SDMMC2_D3_M0	/ I2S1_SDO_M1	/ VOP BT656_D3_M1	/ GPIO3_D1_d	AB1		>SDMMC2_D3_M0 [18]
CIF_D4	/ EBC SDD04	/ SDMMC2_CMD_M0	/ I2S1_SDI0_M1	/ VOP BT656_D4_M1	/ GPIO3_D2_d	Y7		>SDMMC2_CMD_M0 [18]
CIF_D5	/ EBC SDD05	/ SDMMC2_CLK_M0	/ I2S1_SDI1_M1	/ VOP BT656_D5_M1	/ GPIO3_D3_d	AA1	R52 22R R0201	>SDMMC2_CLK_M0 [18]
CIF_D6	/ EBC SDD06	/ SDMMC2_DET_M0	/ I2S1_SDI2_M1	/ VOP BT656_D6_M1	/ GPIO3_D4_d	AA5		>GPIO3_D4 [18]
CIF_D7	/ EBC SDD07	/ SDMMC2_FAREN_M0	/ I2S1_SDI3_M1	/ VOP BT656_D7_M1	/ GPIO3_D5_d			>GPIO3_D5 [18]
CIF_D8	/ EBC SDD08	/ GMAC1_TXD2_M1	/ UART1_TX_M1	/ PWM_CLK0_M1	/ GPIO3_D6_d	Y6	R53 22R R0201	>GMAC1_TXD2_M1 [18]
CIF_D9	/ EBC SDD09	/ GMAC1_TXD3_M1	/ UART1_RX_M1	/ PWM_SDI0_M1	/ GPIO3_D7_d	Y5	R54 22R R0201	>GMAC1_TXD3_M1 [18]
CIF_D10	/ EBC SDD010	/ GMAC1_RXD0_M1	/ UART1_TX_M1	/ PWM_CLK1_M1	/ GPIO4_A0_d	AA3	R55 22R R0201	>GMAC1_TXCLK_M1 [18]
CIF_D11	/ EBC SDD011	/ GMAC1_RXD2_M1	/ UART1_TX_M2	/ PWM_SDI1_M1	/ GPIO4_A1_d	Y4		>GMAC1_RXD2_M1 [18]
CIF_D12	/ EBC SDD012	/ GMAC1_RXD3_M1	/ UART1_TX_M2	/ PWM_SDI2_M1	/ GPIO4_A2_d	Y3		>GMAC1_RXD3_M1 [18]
CIF_D13	/ EBC SDD013	/ GMAC1_RXD0_M1	/ UART1_RX_M2	/ I2S2_LCLK_RX_M1	/ GPIO4_A3_d	Y2	R56 22R R0201	>GMAC1_RXCLK_M1 [18]
CIF_D14	/ EBC SDD014	/ GMAC1_TXD0_M1	/ UART1_RX_M2	/ I2S2_LCLK_RX_M1	/ GPIO4_A4_d	Y1	R57 22R R0201	>GMAC1_TXD0_M1 [18]
CIF_D15	/ EBC SDD015	/ GMAC1_TXD1_M1	/ UART1_RX_M2	/ I2S2_LCLK_RX_M1	/ GPIO4_A5_d			>GMAC1_TXD1_M1 [18]
ISP_FLASHTRIGOUT	/ EBC SDCE0	/ GMAC1_TXEN_M1	/ SPI3_CS0_M0	/ I2S1_SCLK_RX_M1	/ GPIO4_A6_d	W2	R58 22R R0201	>GMAC1_TXEN_M1 [18]
CAM_CLKOUT0	/ EBC SDCE1	/ GMAC1_RXD0_M1	/ SPI3_CS1_M0	/ I2S1_LCLK_RX_M1	/ GPIO4_A7_d	W1		>GMAC1_RXD0_M1 [18]
CAM_CLKOUT1	/ EBC SDCE2	/ GMAC1_RXD1_M1	/ SPI3_MISO_M0	/ I2S1_SDI0_M1	/ GPIO4_B0_d	V7		>GMAC1_RXD1_M1 [18]
ISP_PRELIGHT_TRIG	/ EBC SDCE3	/ GMAC1_RXDV_CRS_M1	/ I2S1_SDO2_M1	/ I2S1_SDO2_M1	/ GPIO4_B1_d	V2		>GMAC1_RXDV_CRS_M1 [18]
I2C4_SDA_M0	/ EBC VCOM	/ GMAC1_RXER_M1	/ SPI3_MOSI_M0	/ I2S2_SDI_M1	/ GPIO4_B2_d	V4		>>I2C4_SDA_M0 [18]
I2C4_SCL_M0	/ EBC GD08	/ ETH1_REFCLK0_25M_M1	/ SPI3_CLK_M0	/ I2S2_SDO_M1	/ GPIO4_B3_d	V1		>>I2C4_SCL_M0 [18]
I2C2_SDA_M1	/ EBC GDSP	/ CAN2_RX_M0	/ I2S1_FLASH_TRIGIN	/ VOP BT656_CLK_M1	/ GPIO4_B4_d	V6		>>CAN2_RX_M0 [18]
I2C2_SCL_M1	/ EBC SD58A	/ CAN2_TX_M0	/ I2S1_SDO3_M1	/ I2S1_SDO3_M1	/ GPIO4_B5_d	V5		>>CAN2_TX_M0 [18]
CIF_HREF	/ EBC SDLE	/ GMAC1_MDC_M1	/ UART1_RTS_M1	/ I2S2_MCLK_M1	/ GPIO4_B6_d	U5		>>GMAC1_MDC_M1 [18]
CIF_VSYNC	/ EBC SD0E	/ GMAC1_MDIO_M1	/ I2S2_SCLK_TX_M1	/ I2S2_SCLK_TX_M1	/ GPIO4_B7_d	U4		>>GMAC1_MDIO_M1 [18]
CIF_CLKOUT	/ EBC GDCLK	/ PWM1_IR_M1	/ I2S2_SCLK_RX_M1	/ I2S2_SCLK_RX_M1	/ GPIO4_C0_d	U3		>>GPIO4_C0 [18]
CIF_CLKIN	/ EBC SDCLK	/ GMAC1_MCLKINOUT_M1	/ UART1_CTS_M1	/ I2S2_SCLK_RX_M1	/ GPIO4_C1_d	U2		>>GMAC1_MCLKINOUT_M1 [18]



RK3568
bga636_19r00x19r00x1r20

Note:

Caps of between dashed green lines and U3 should be placed under the U3 package.
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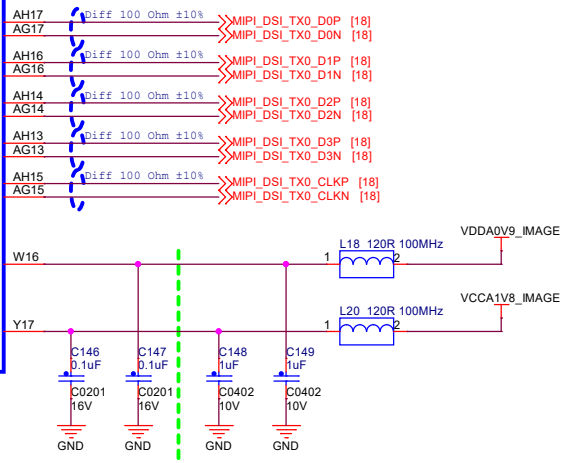
Title 野火 EBF RK3568 BTB核心板		
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RK3568 MIPI_DSI_TX0/LVDS_TX0

U3R

MIPI DSI TX0/LVDS TX0

MIPI_DSI_TX0_D0P/LVDS_TX0_D0P
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP
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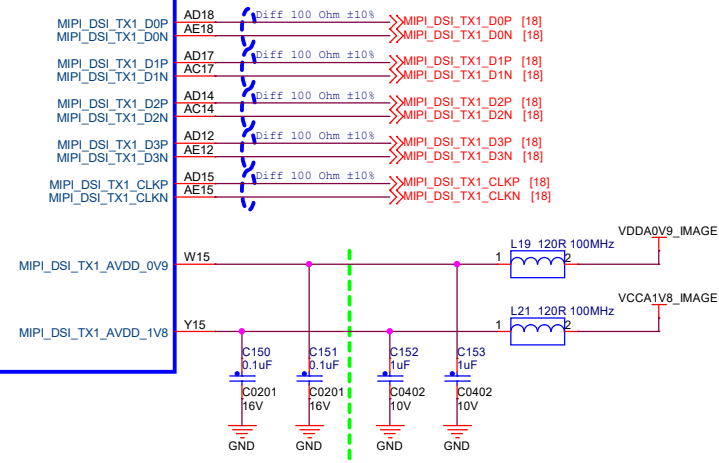
RK3568
bga636_19r00x19r00x1r20

RK3568 MIPI_DSI_TX1

U3S

MIPI DSI TX1

MIPI_DSI_TX1_D0P
MIPI_DSI_TX1_D0N
MIPI_DSI_TX1_D1P
MIPI_DSI_TX1_D1N
MIPI_DSI_TX1_D2P
MIPI_DSI_TX1_D2N
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MIPI_DSI_TX1_CLKP
MIPI_DSI_TX1_CLKN



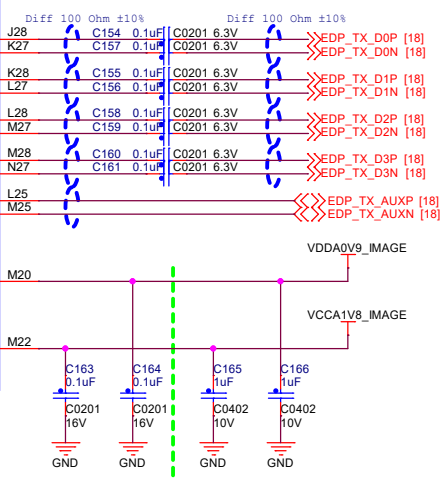
RK3568
bga636_19r00x19r00x1r20

RK3568 eDP TX

U3T

eDP_TX

eDP_TX_D0P
eDP_TX_D0N
eDP_TX_D1P
eDP_TX_D1N
eDP_TX_D2P
eDP_TX_D2N
eDP_TX_D3P
eDP_TX_D3N
eDP_TX_AUXP
eDP_TX_AUXN



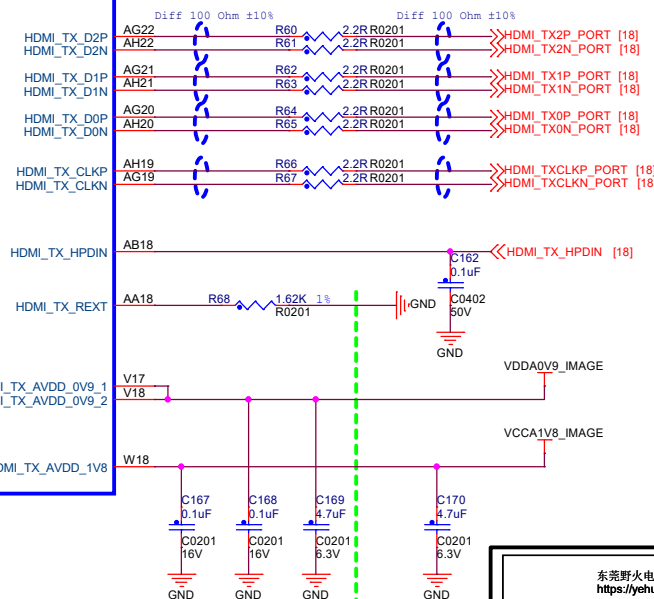
RK3568
bga636_19r00x19r00x1r20

RK3568 HDMI2.0 TX

U3Q

HDMI2.0 TX

HDMI_TX_D2P
HDMI_TX_D2N
HDMI_TX_D1P
HDMI_TX_D1N
HDMI_TX_D0P
HDMI_TX_D0N
HDMI_TX_CLKP
HDMI_TX_CLKN



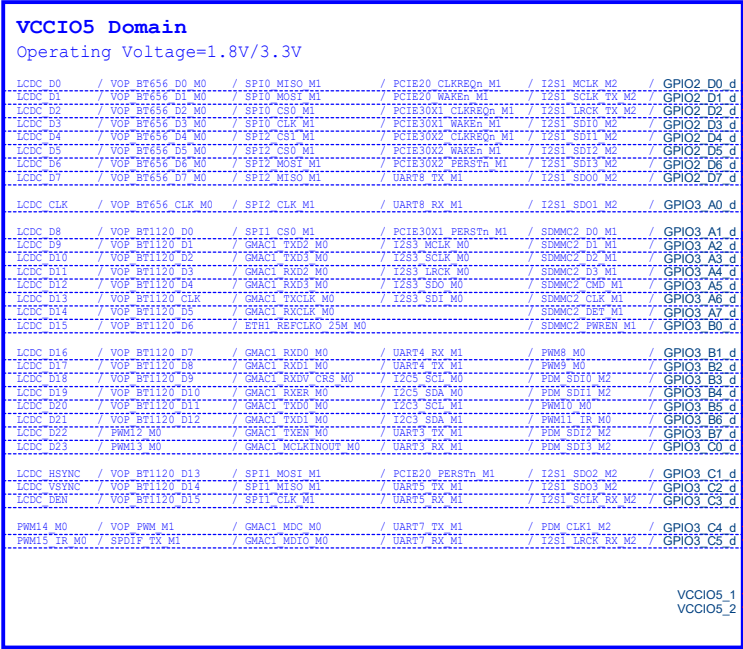
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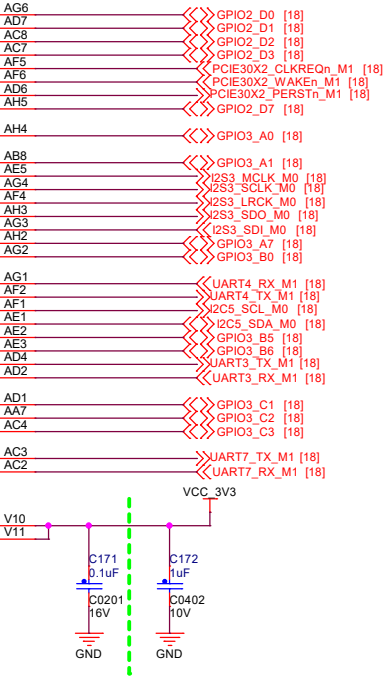
Title		
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Size	Document Number	Rev
A3	VO Interface_1	V1.0
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RK3568 VCCIO5 Domain

U3L



RK3568
bga636_19r00x19r00x120

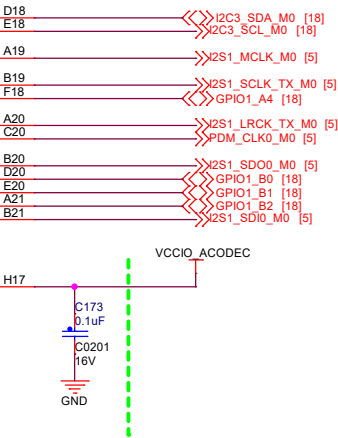
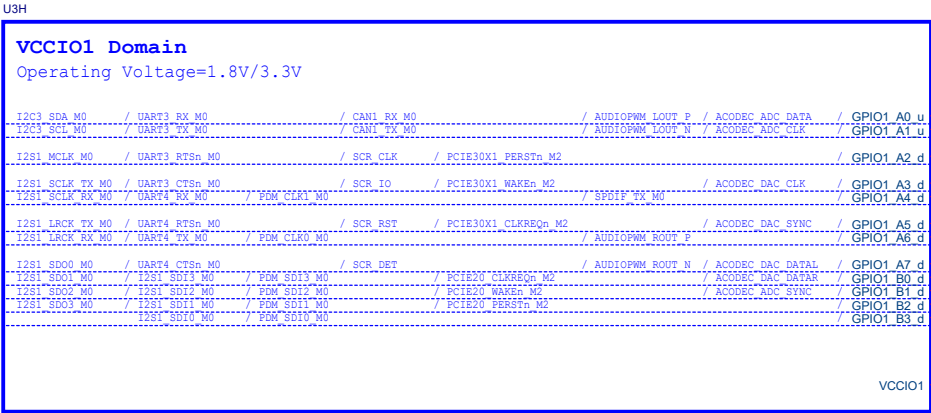


Note:

Caps of between dashed green lines and U3 should be placed under the U3 package.
Other caps should be placed close to the U3 package

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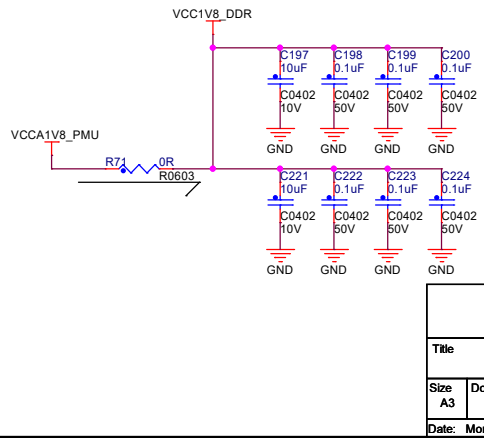
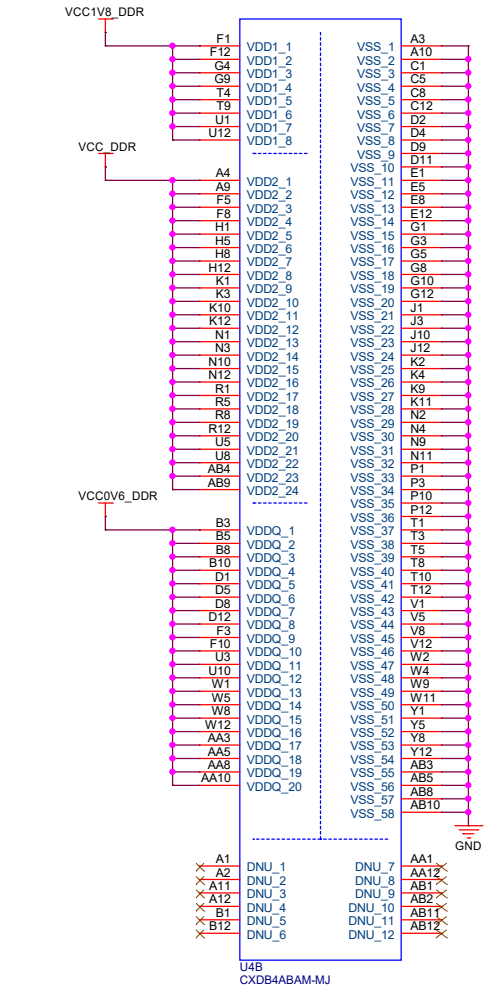
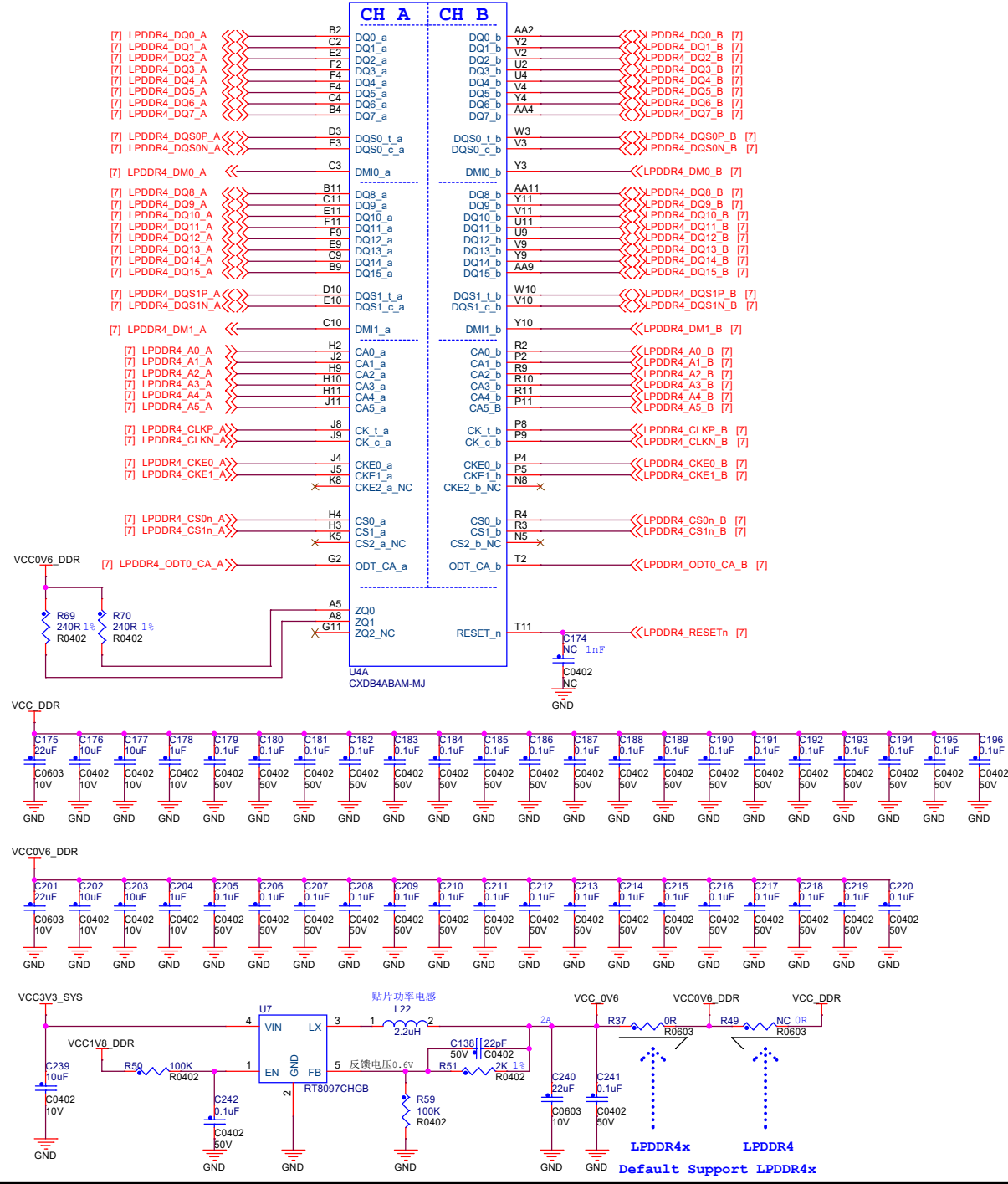
RK3568 VCCIO1 Domain



Note:
Caps of between dashed green lines and U3
should be placed under the U3 package.
Other caps should be placed close to the U3 package

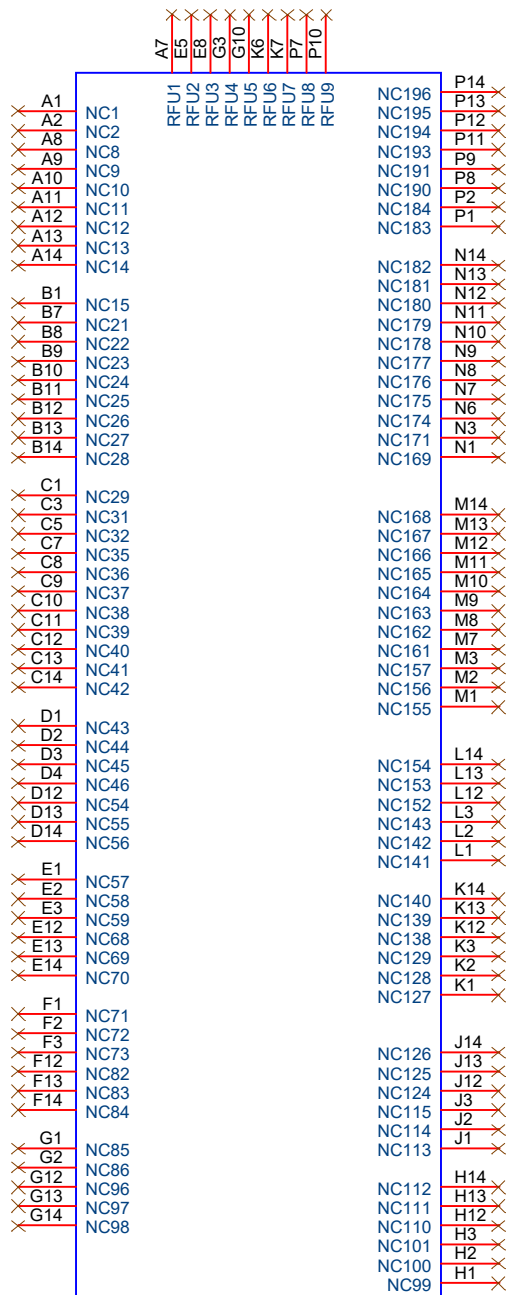
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LPDDR4/LPDDR4x

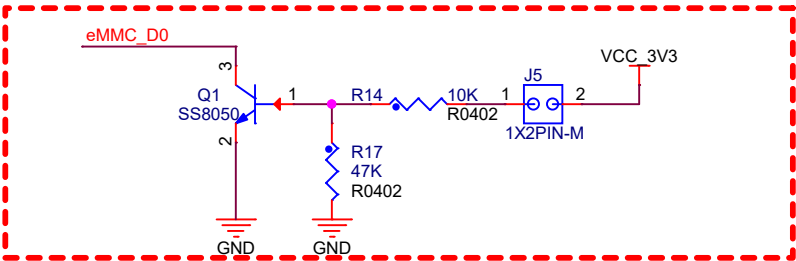
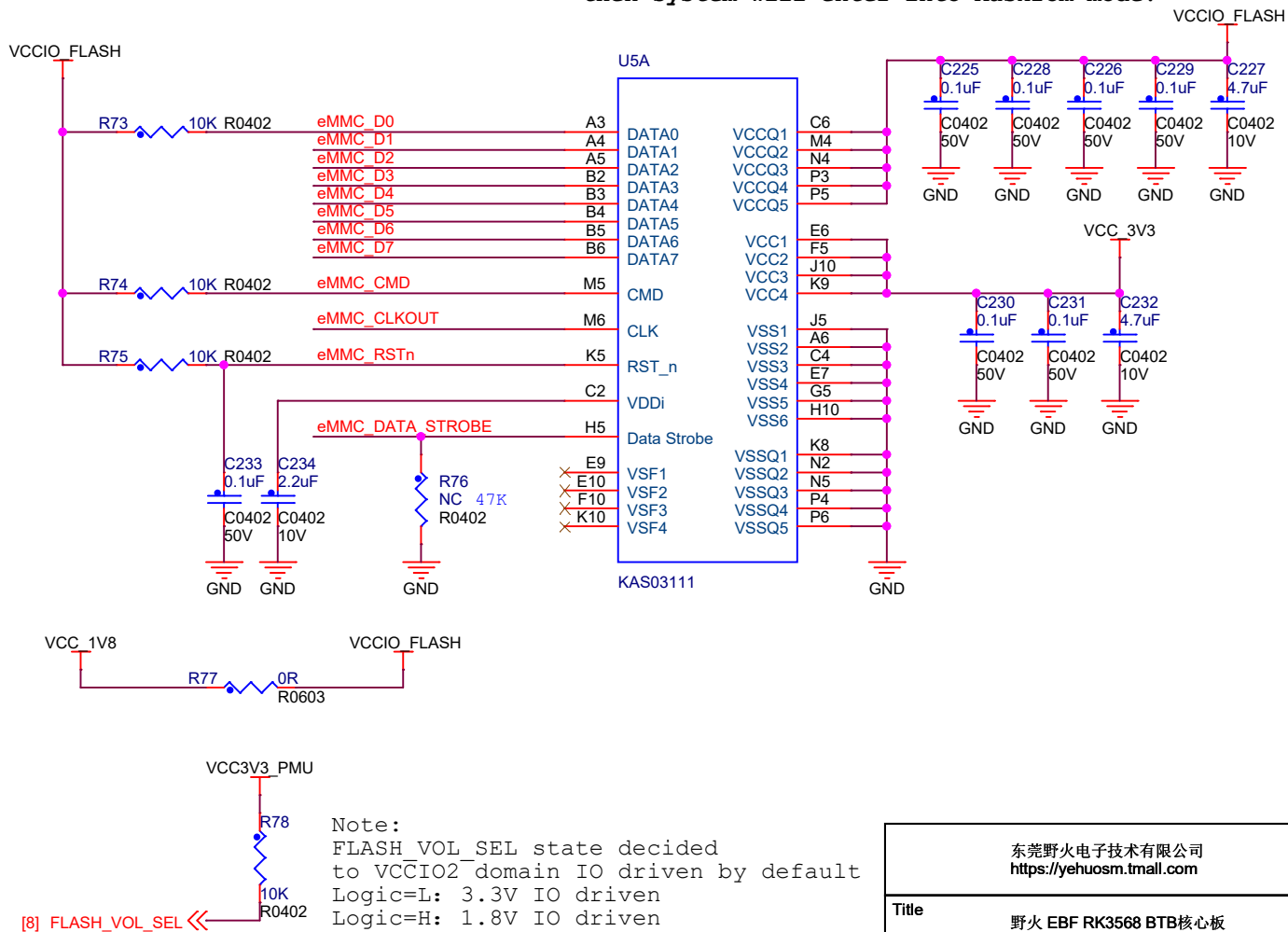
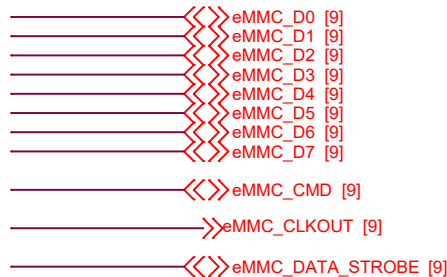


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eMMC Flash



U5B
KAS03111



Note:
For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset,
then system will enter into Maskrom mode.

Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

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