

野火_RK3568_LubanCat_2_N_原理图

目录

Page 1	Content
Page 2	Historic Version
Page 3	POWER DIAGRAM
Page 4	DC_IN/OTG_Download
Page 5	PMIC_DCDC/LDO
Page 6	PMIC_Management/CODE
Page 7	Power_other
Page 8	RK3568_Power/GND
Page 9	DDR PHY
Page 10	LPDDR4/4x
Page 11	RK3566_OSC/PLL/PMUIO
Page 12	EMMC/SD Controller
Page 13	USB/PCIe/SATA PHY
Page 14	SARADC/GPIO
Page 15	VI Interface
Page 16	VO Interface_1
Page 17	VO Interface_2
Page 18	Audio Interface
Page 19	EMMC_FLASH
Page 20	ETH_1
Page 21	ETH_2
Page 22	USB_PORT
Page 23	HDMI_PORT/SATA_PORT
Page 24	MIPI DSI/MIPI CSI_PORT 1
Page 25	MIPI DSI/MIPI CSI_PORT 2
Page 26	PCIE3.0 REFCLK

[illegible]

历史版本

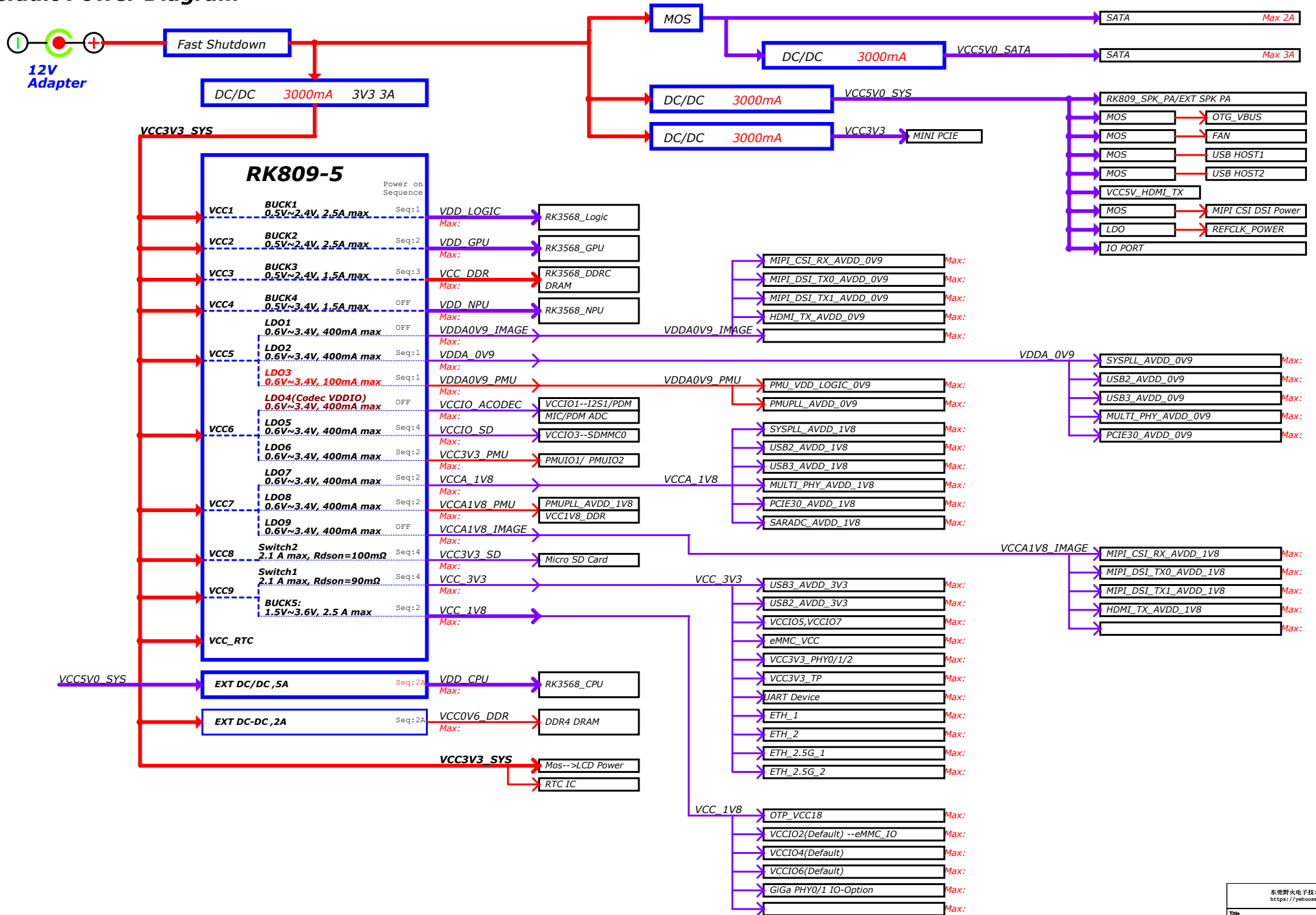
版本号	日期	设计	描述
V0.1	2022-05-05	ghs	初始版本
V1.0	2022-09-09	ghs	修正U27开启信号接反的问题，解决调试接口漏电的问题
V1.1	2022-09-09	ghs	修正BOARD ID的ID识别电阻的电源域，修正PHY芯片的复位引脚电压不匹配问题
V1.2	2022-12-13	ghs	增加网卡上拉电阻，更新mini pcie的固定螺丝柱
V1.3	2023-07-13	ghs	新增一个MIPI CSI，一个MIPI DSI
V3R0	2024-03-22	ghs	由于PMIC内置RTC电路功耗大，由此停用内置的RTC电路，增加外挂RTC模块电路 添加RTC_INT唤醒电路，调整SATA_PWR的I/O引脚

东莞野火电子有限公司
<https://yehuosm.tmall.com>

Title野火_RK3568 LubanCat 2 N_原理图

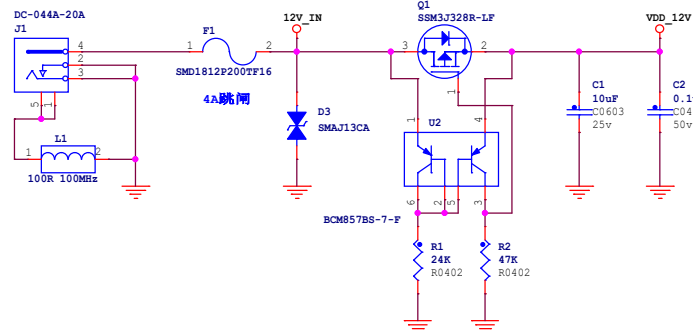
SizeA3	Document NumberHistoric Version	RevV3R0
Date: Friday, March 22, 2024	Sheet 2	of 29

Default Power Diagram

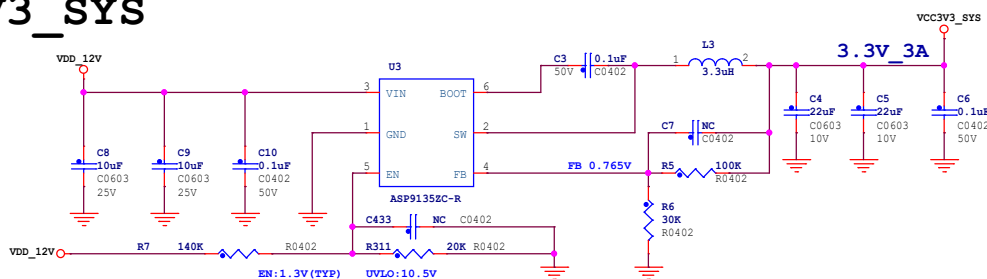


DC 12V 3A POWER IN

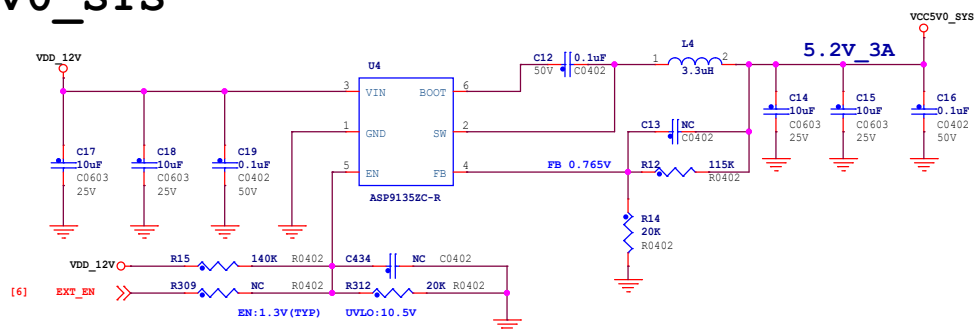
12V/3A



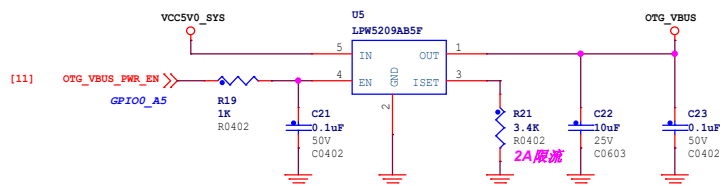
3V3_SYS



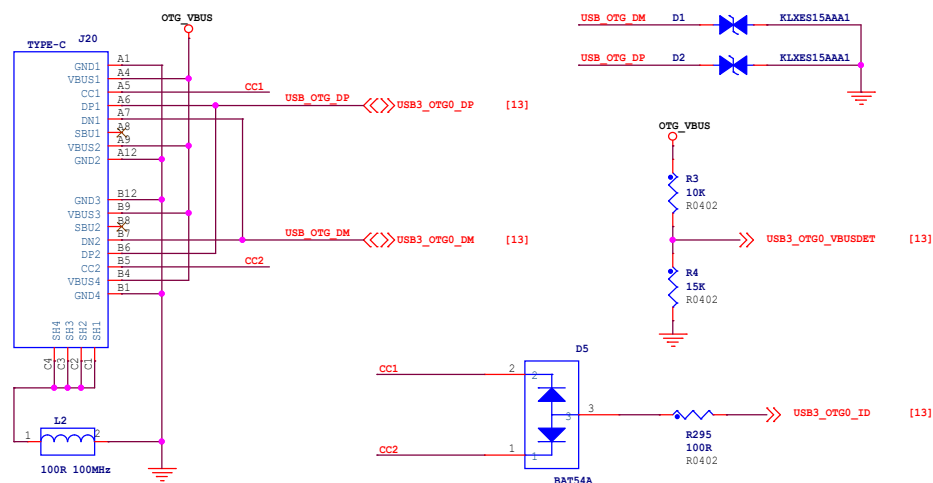
5V0_SYS



OTG POWER

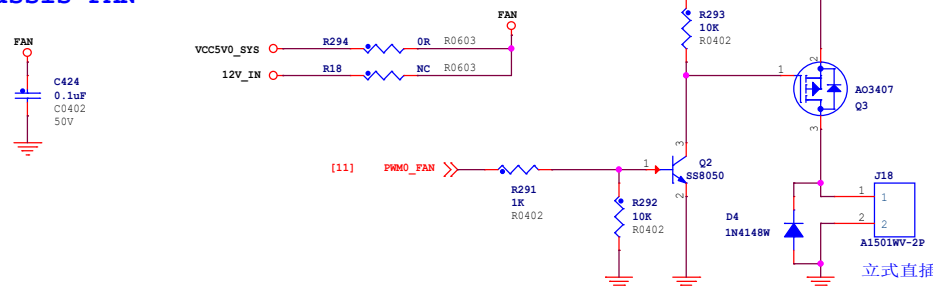


OTG/Download



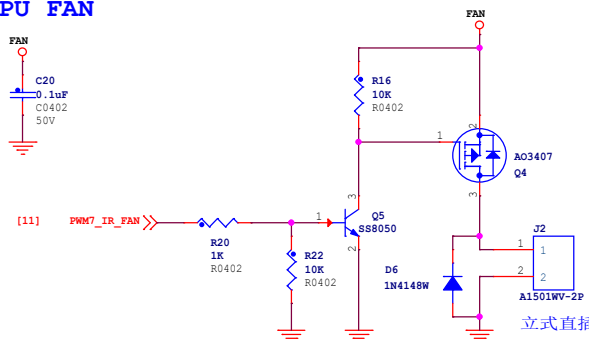
Active Cooling

Chassis FAN



Active Cooling

CPU FAN



Fix Hole

4*M3



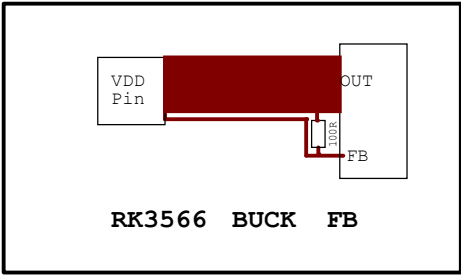
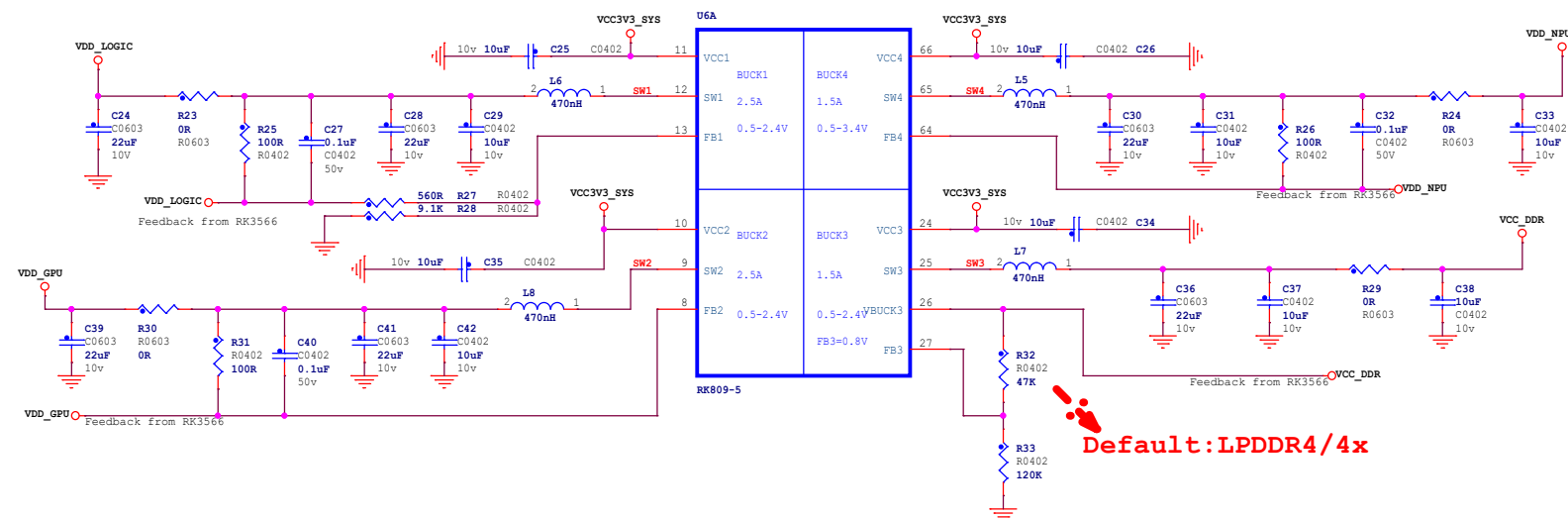
东莞野火电子技术有限公司
https://yehuosm.taobao.com

Title 野火_RK3568 LubanCat 2 N_原理图

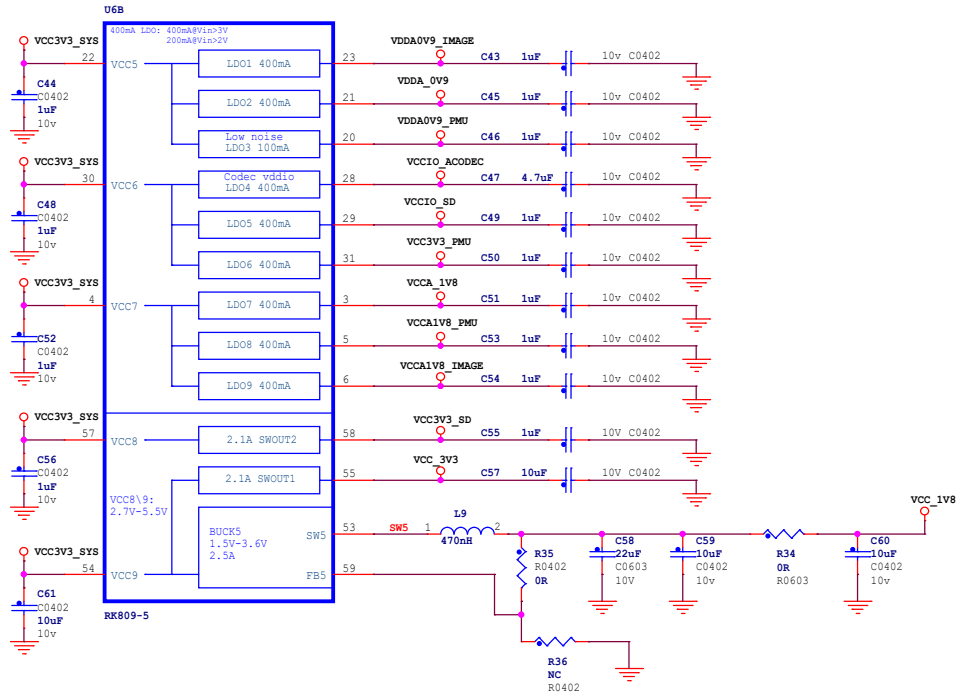
Size A3 Document Number DC_IN/OTG_Download Rev V3R0

Date: Tuesday, October 22, 2024 Sheet 4 of 29

PMIC RK809 DCDC

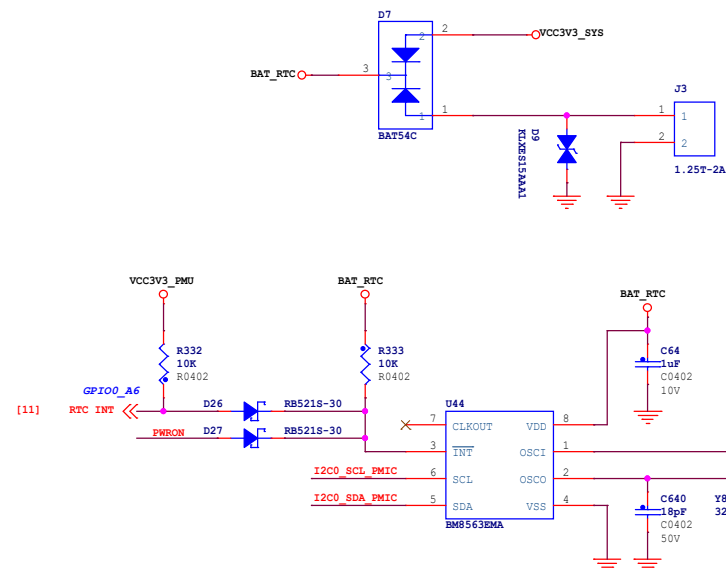


PMIC RK809 LDO

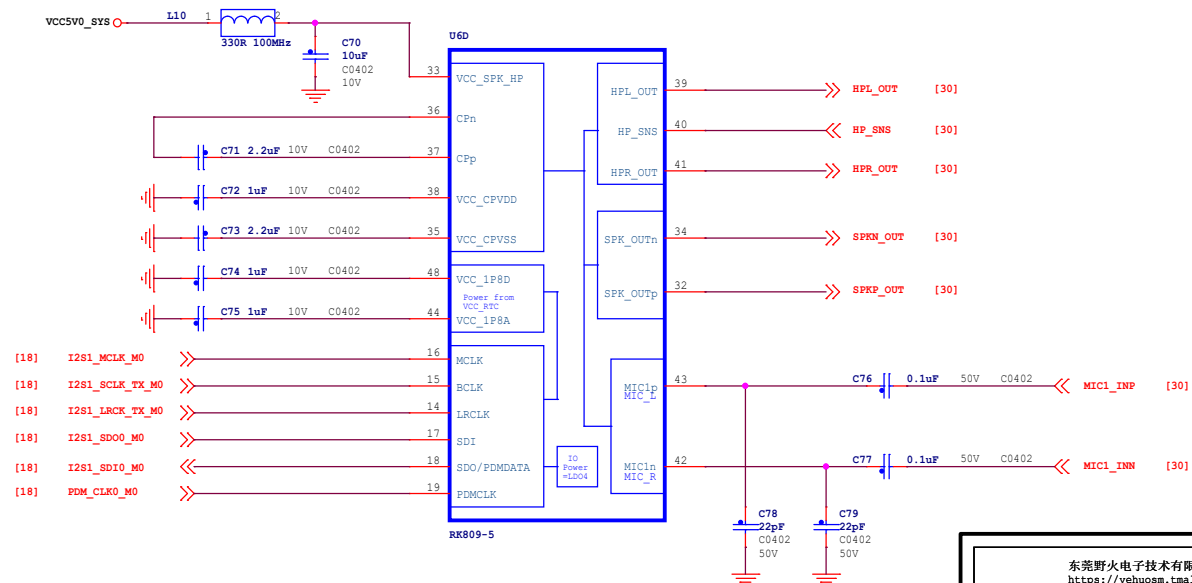


东莞野火电子技术有限公司 https://yehuosm.tmall.com		
Title	野火_RK3568 LubanCat 2_N_原理图	
Size A3	Document Number PMIC_DCDC/LDO	Rev V3R0
Date: Friday, March 22, 2024	Sheet 5	of 29

PWR LED

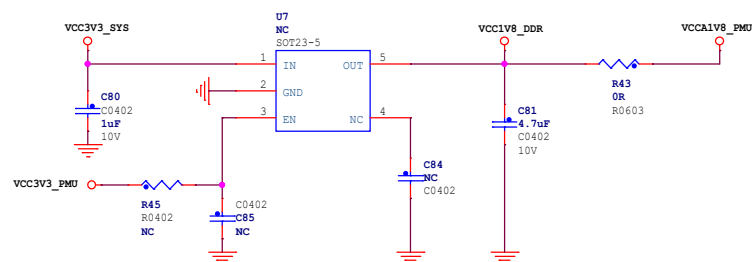


PWR LED



Date: Friday, March 22, 2024 Sheet 6 of 29

LPDDR4_VCC1V8_DDR

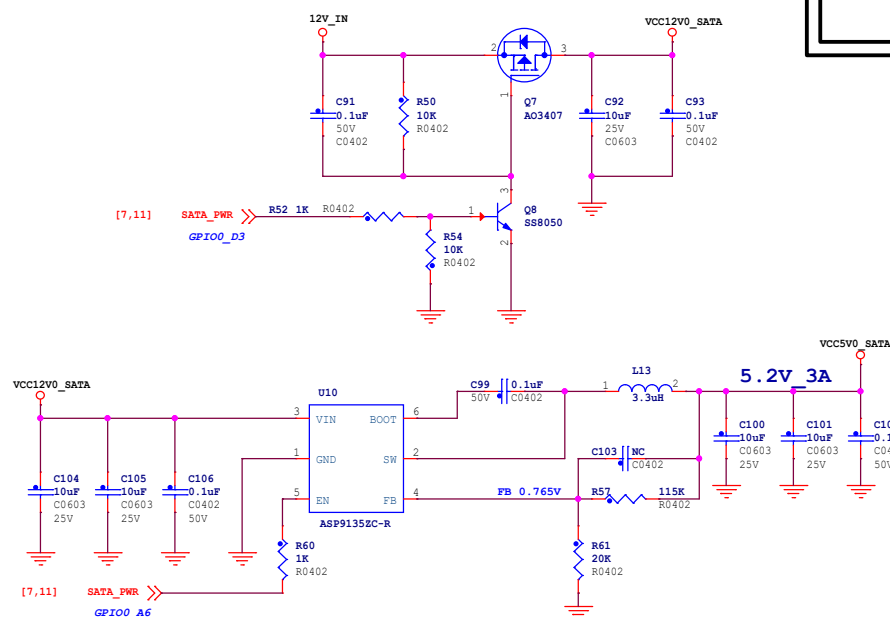


VCC5V0_SATA

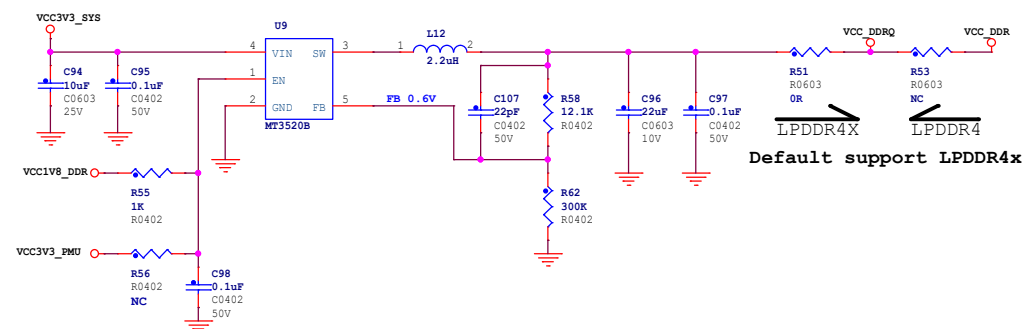
VCC12V0_SATA

J4
XH-4A

1 1
2 2
3 3
4 4

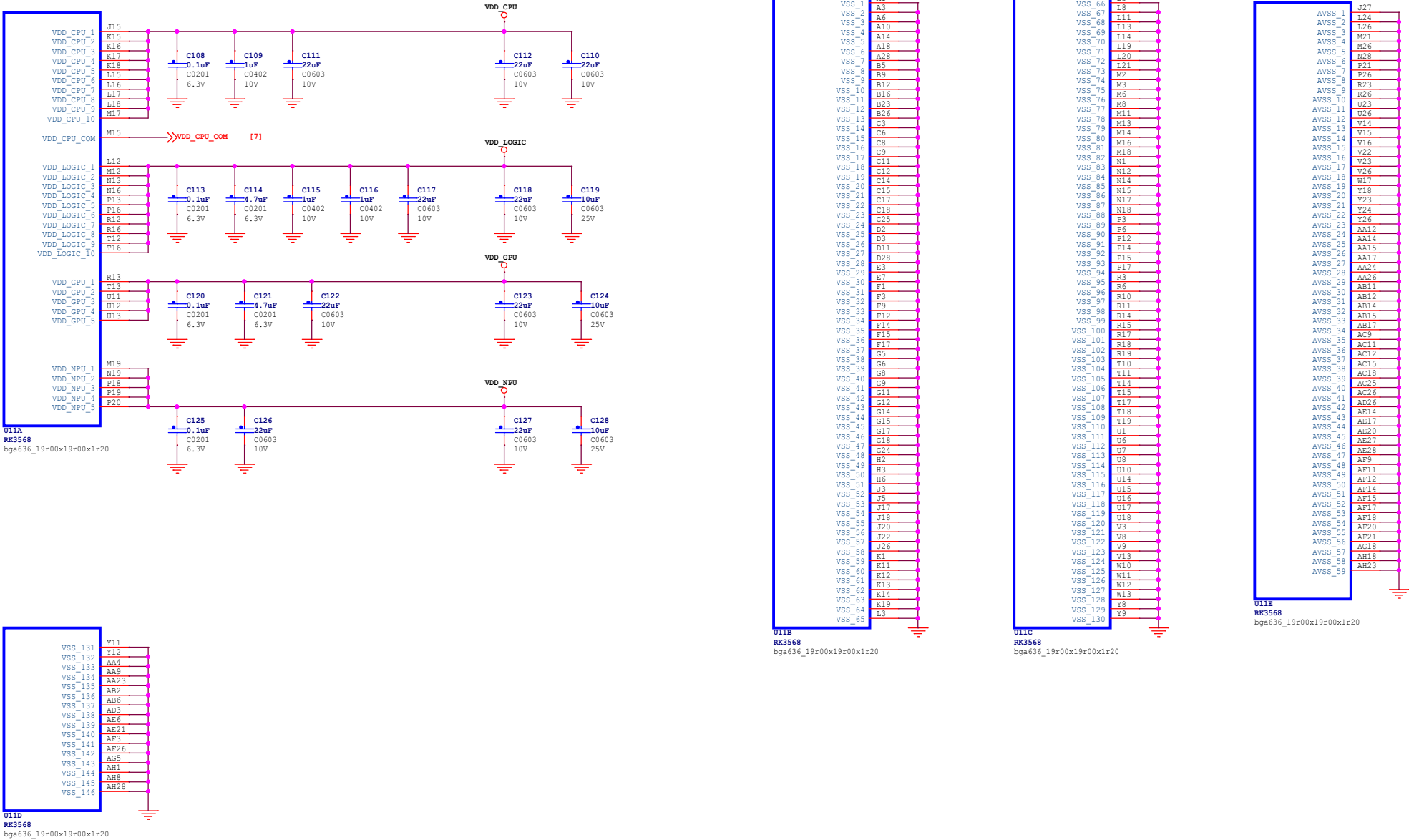
[illegible]

output: 0.6V



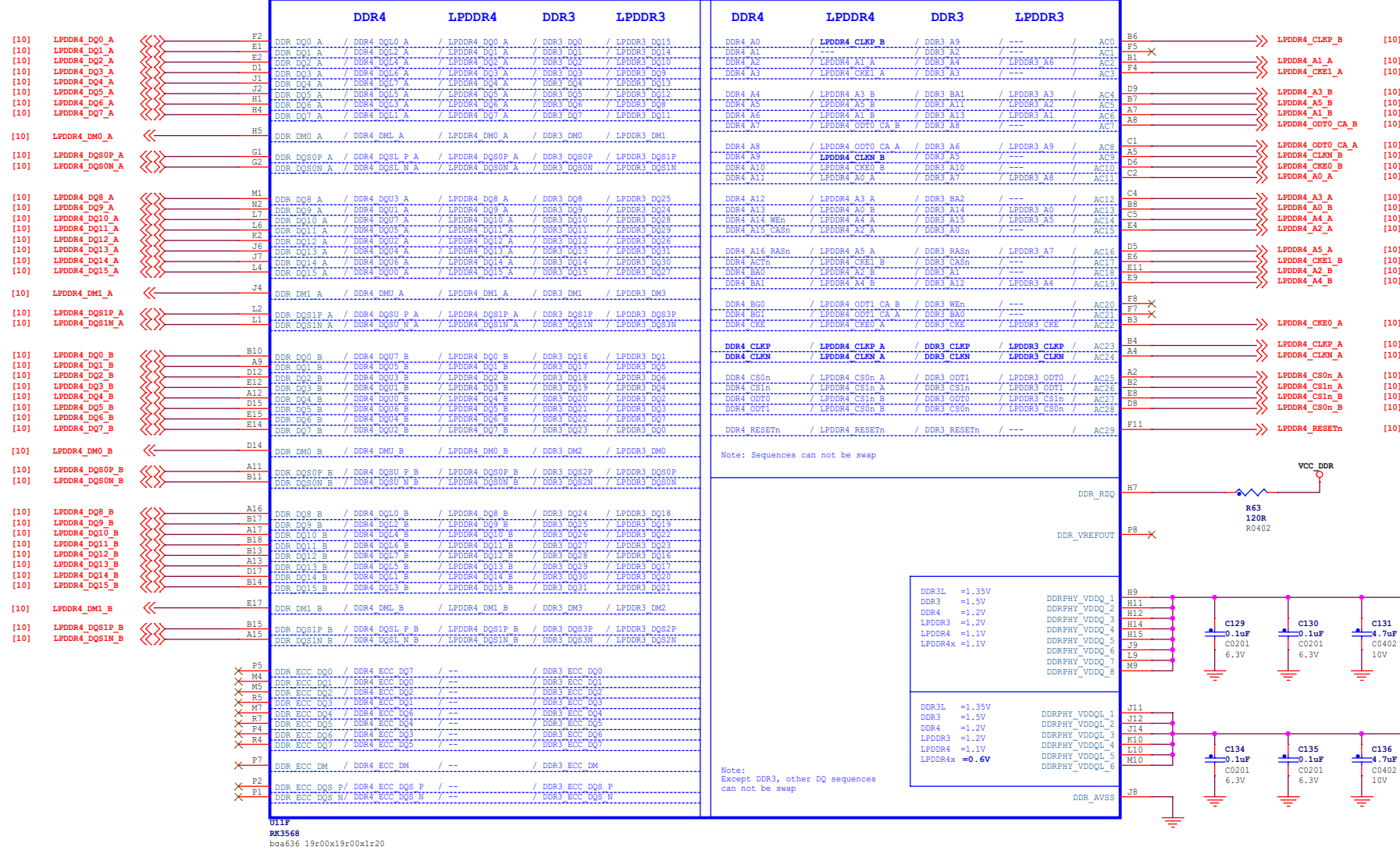
Date: Tuesday, October 22, 2024 Sheet 7 of 29

RK3568 Power/GND

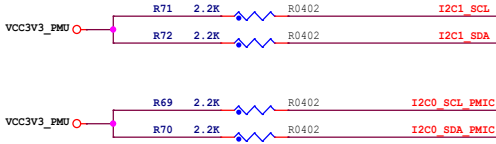
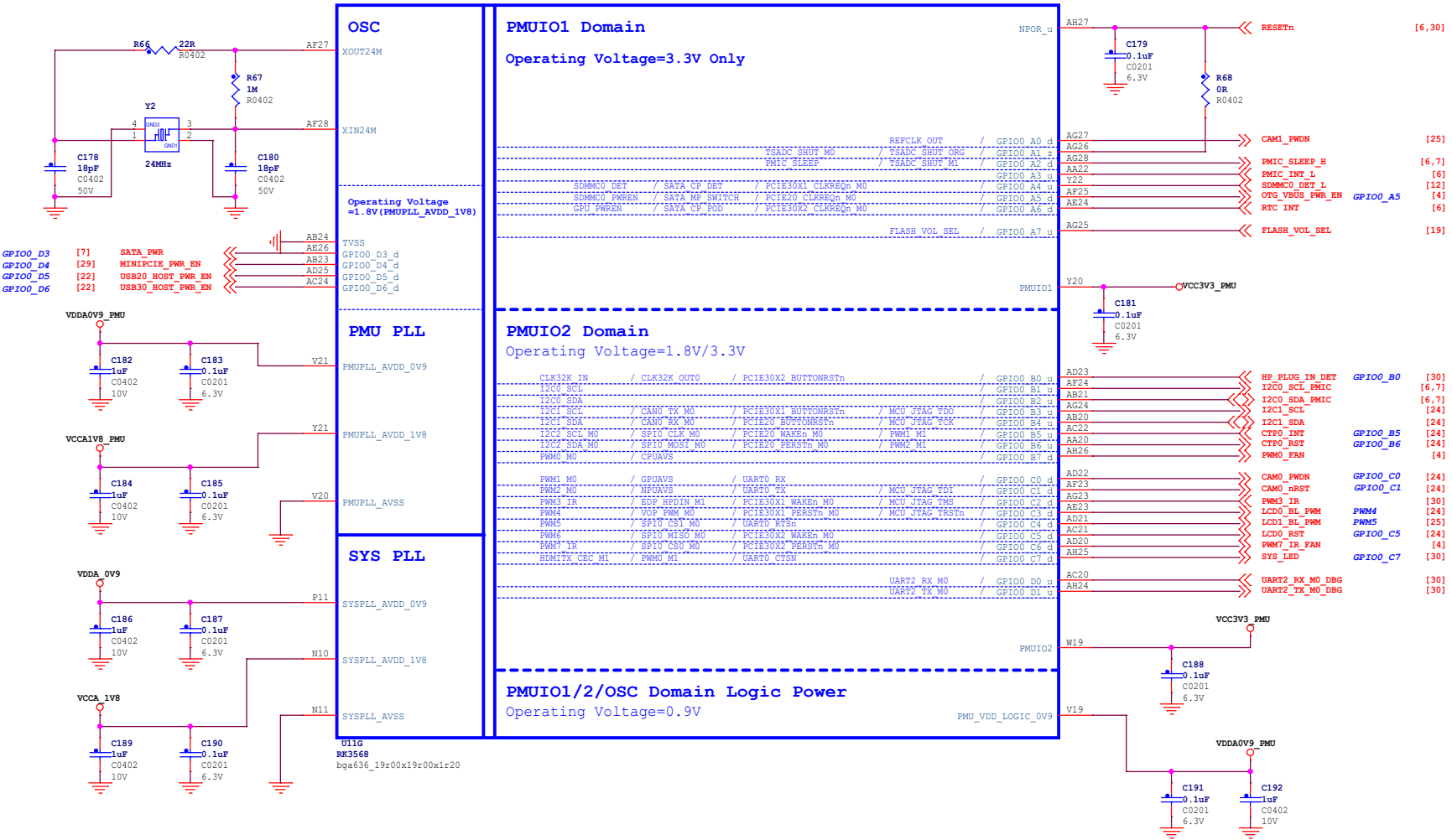


东莞野火电子有限公司 https://yehuosm.tmall.com		
Title 野火_RK3568 LubanCat 2 N_原理图		
Size A3	Document Number RK3568_Power/GND	Rev V3R0
Date: Friday, March 22, 2024	Sheet 8	of 29

RK3568 DDR PHY

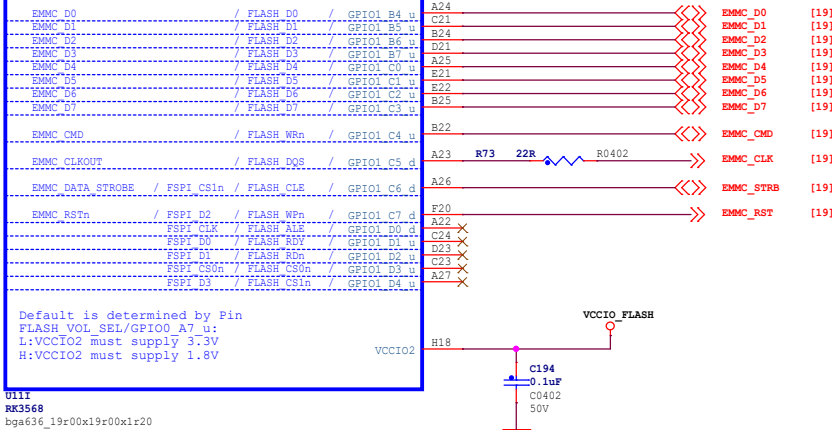


RK3568 OSC/PLL/PMUIO



RK3568 VCCIO2 Domain

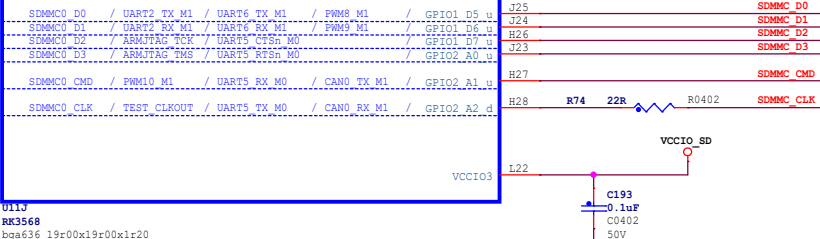
VCCIO2 Domain
Operating Voltage=1.8V/3.3V



Resistor close to SOC
terminal

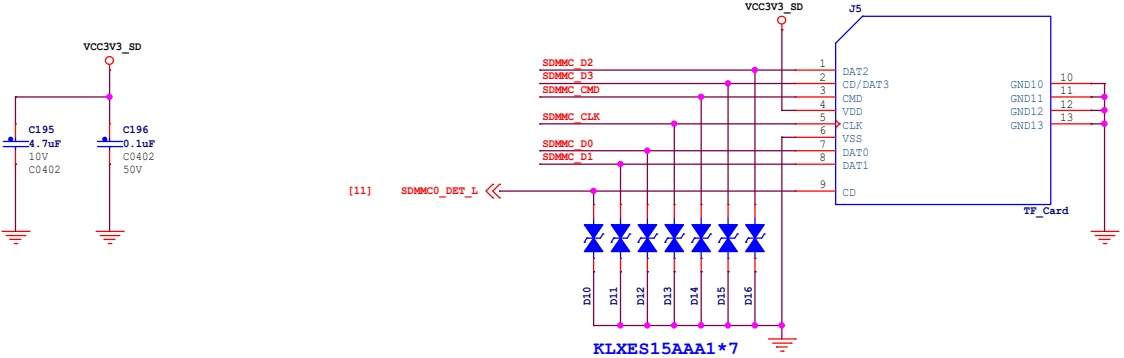
RK3568 VCCIO3 Domain

VCCIO3 Domain
Operating Voltage=1.8V/3.3V

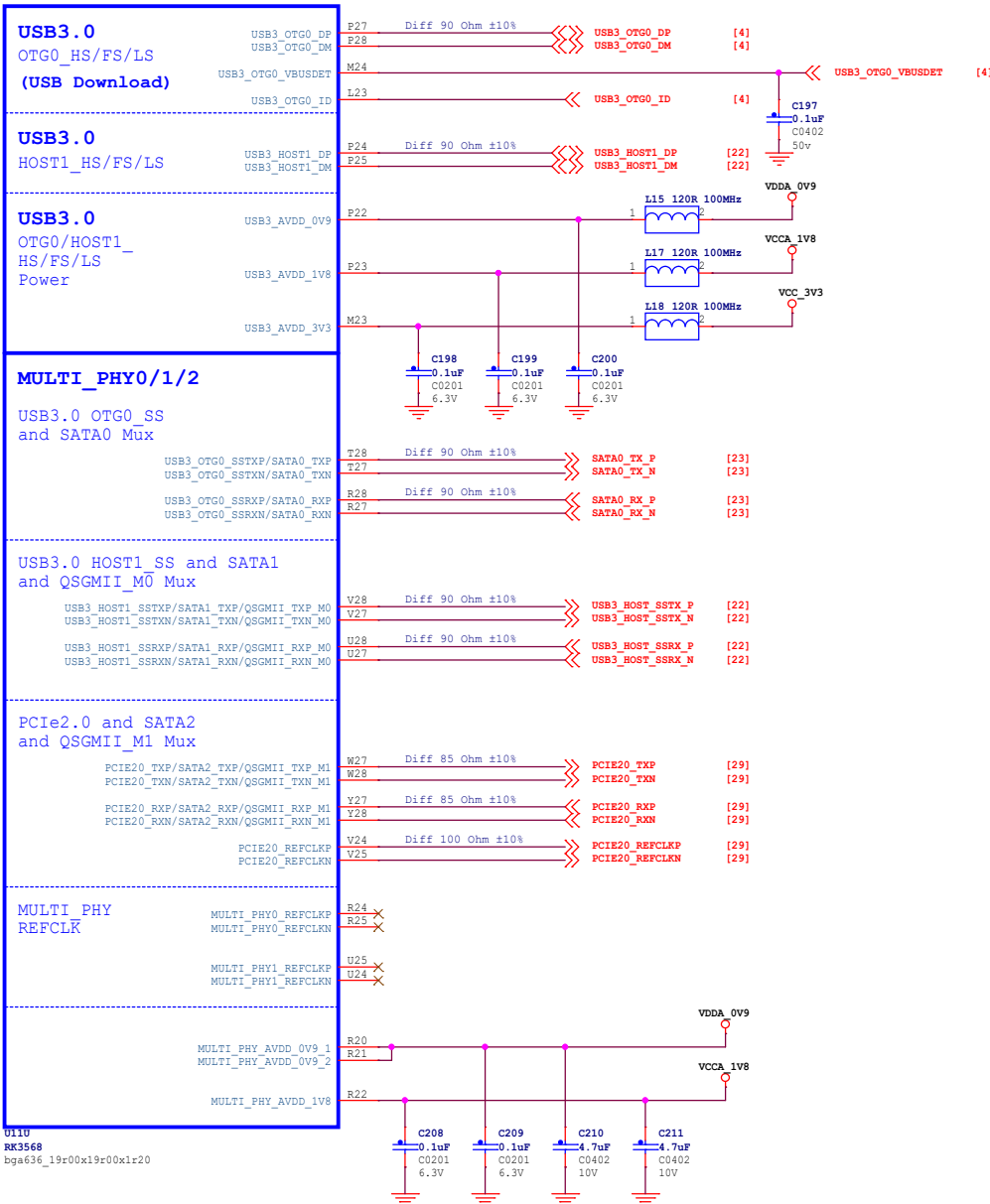


Resistor close to SOC
terminal

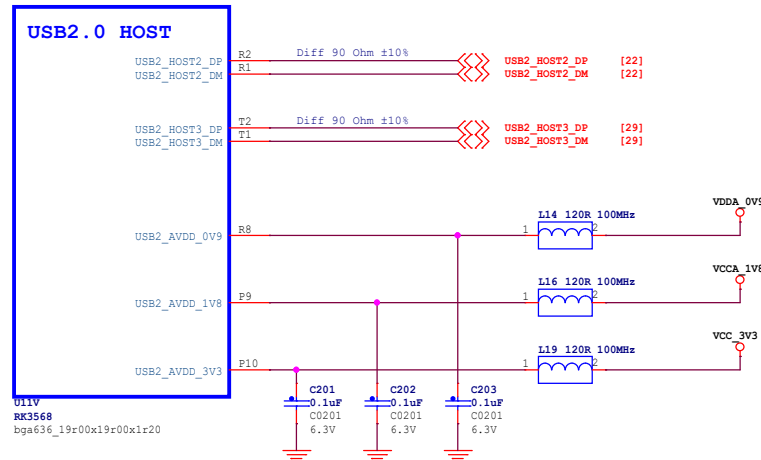
TF_CARD



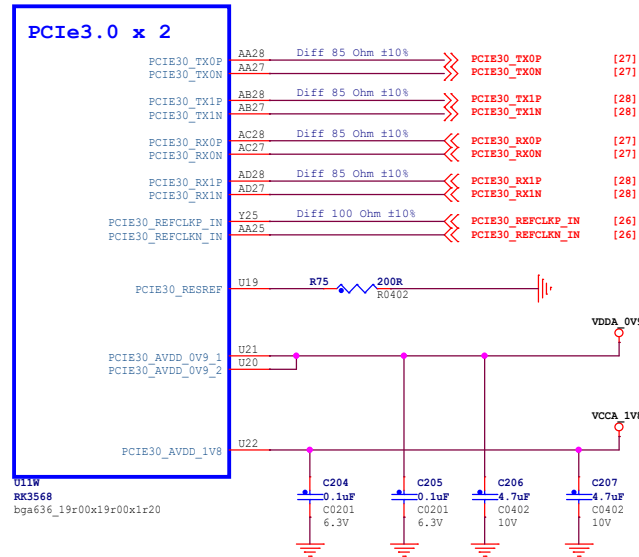
RK3568 USB3.0/SATA/QSGMII/PCIe2.0 x1



RK3568 USB2.0 HOST

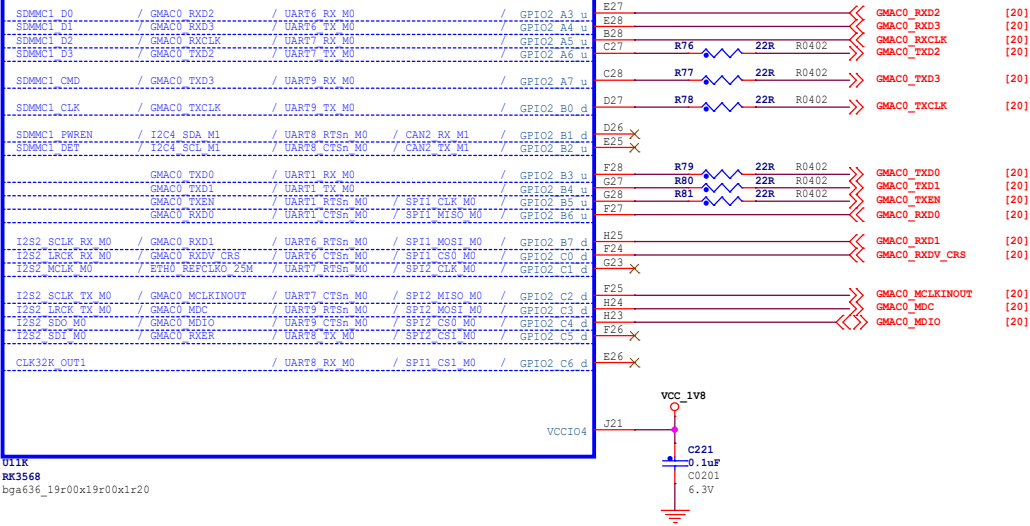


RK3568 PCIe3.0 x2

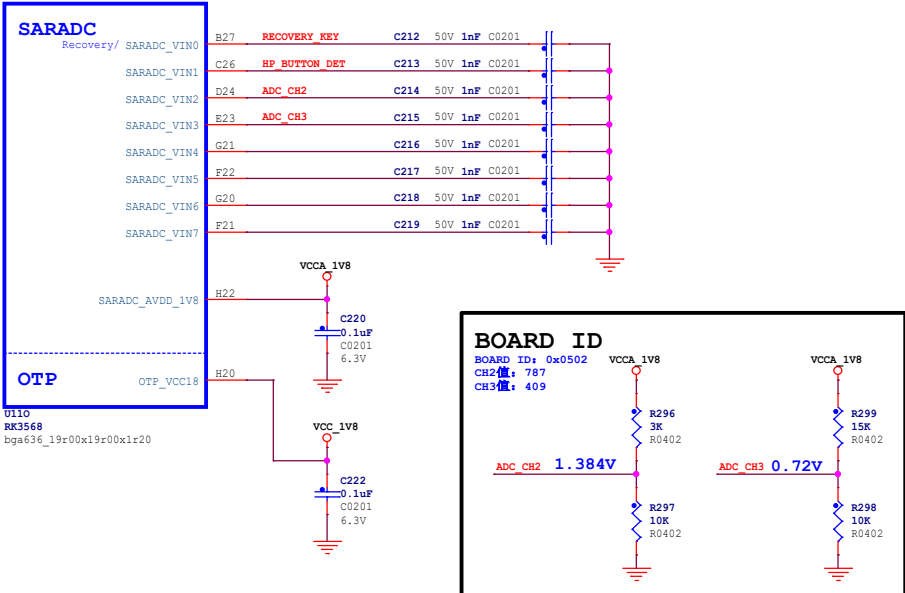


RK3568 VCCIO4 Domain

VCCIO4 Domain
Operating Voltage=1.8V/3.3V

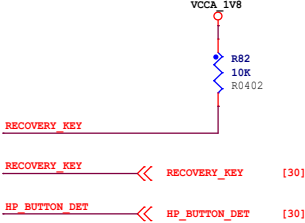
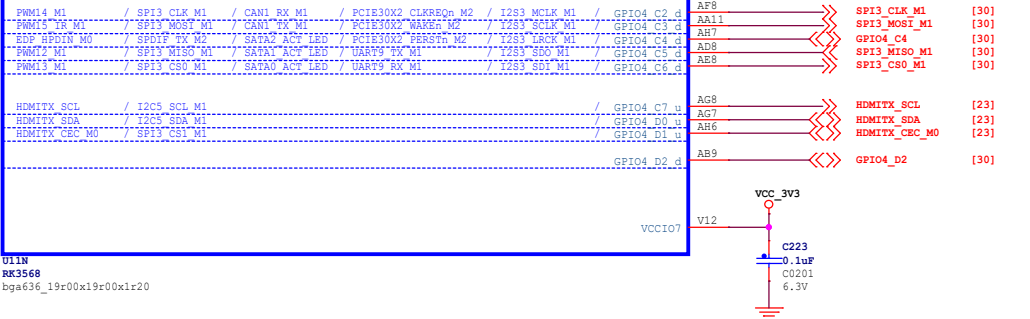


RK3568 SARADC/OTP

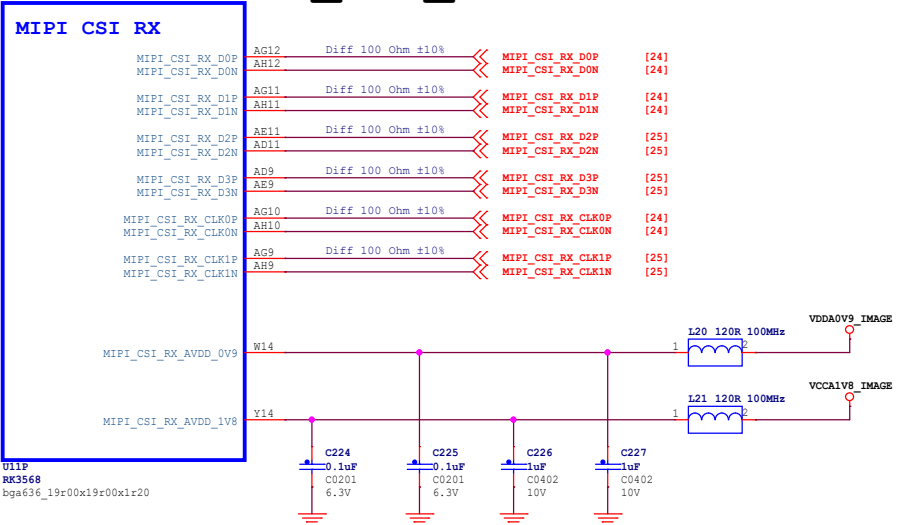


RK3568 VCCIO7 Domain

VCCIO7 Domain
Operating Voltage=1.8V/3.3V

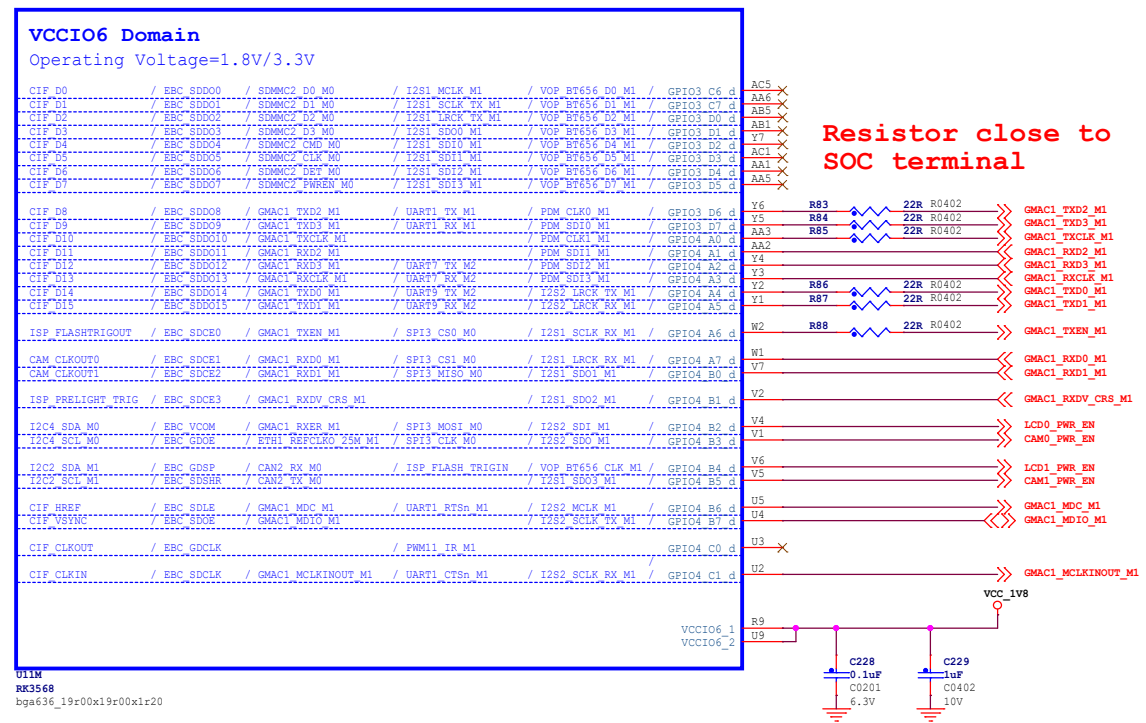


RK3568 MIPI_CSI_RX



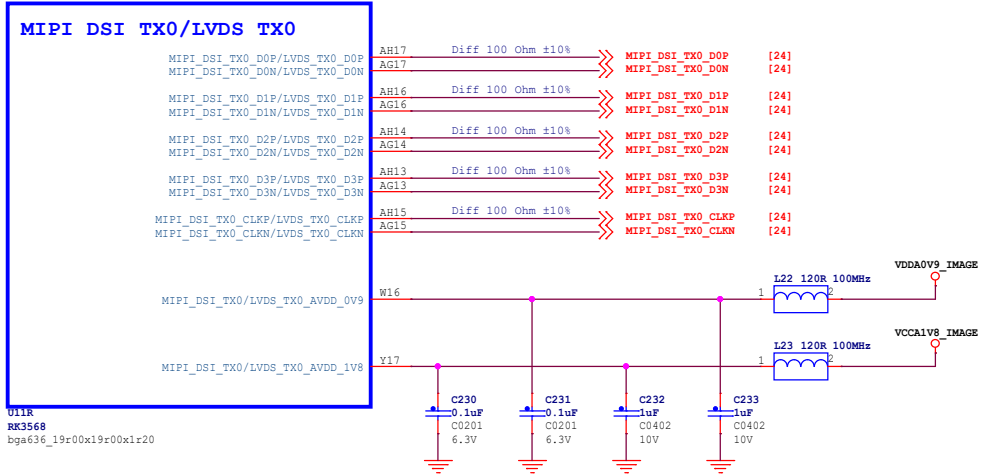
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568 VCCIO6 Domain

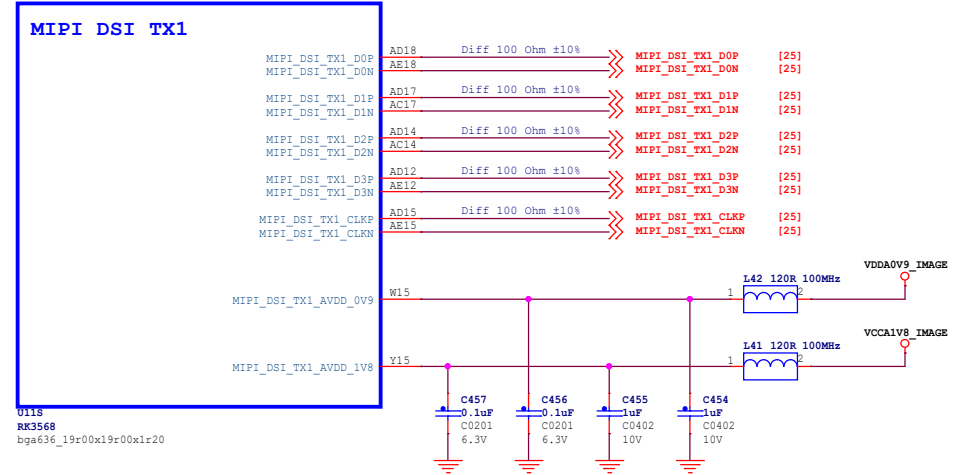


Title		
野火_RK3568 Iubancat 2 N_原理图		
Size A3	Document Number VI Interface	Rev V3R0
Date: Friday, March 22, 2024 Sheet 15 of 29		

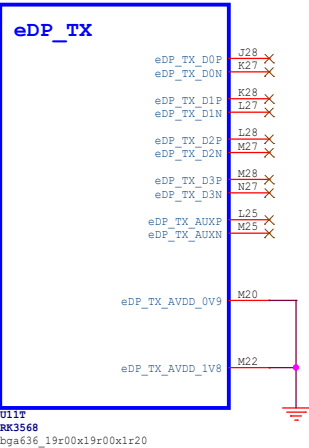
RK3568 MIPI_DSI_TX0/LVDS_TX0



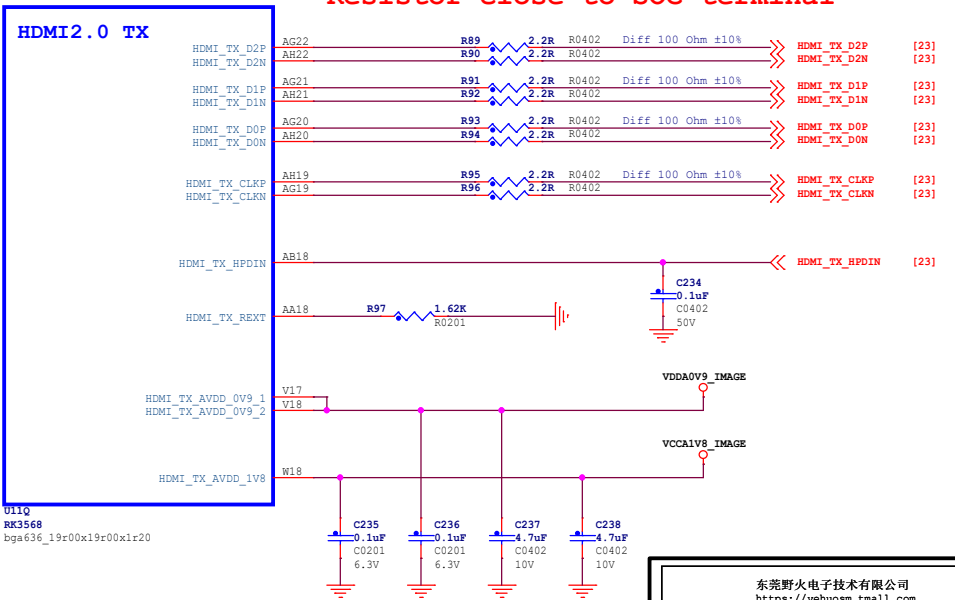
RK3568 MIPI_DSI_TX1



RK3568 eDP TX



RK3568 HDMI2.0 TX

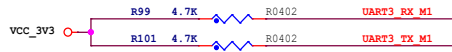
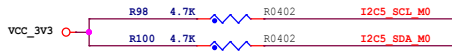
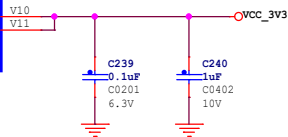


RK3568 VCCIO5 Domain

VCCIO5 Domain					
Operating Voltage=1.8V/3.3V					
LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQn M1	/ I2S1 MCLK M2	/ GPIO2 D0 D
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 D
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREQn M1	/ I2S1 LCLK TX M2	/ GPIO2 D2 D
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDIO M2	/ GPIO2 D3 D
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CSY M1	/ PCIE30X1 CLKREQn M1	/ I2S1 SDI1 M2	/ GPIO2 D4 D
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X1 WAKEn M1	/ I2S1 SDI2 M2	/ GPIO2 D5 D
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 D
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART9 TX M1	/ I2S1 SDIO M2	/ GPIO2 D7 D
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART9 RX M1	/ I2S1 SD01 M2	/ GPIO3 A0 D
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 D
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 D
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 D
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 LCLK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 D
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 SD0 M1	/ SDMMC2 CLK M1	/ GPIO3 A5 D
LCDC D13	/ VOP BT1120 D5	/ GMAC1 RXD4 M0	/ I2S3 SDI M1	/ SDMMC2 DEN M1	/ GPIO3 A6 D
LCDC D14	/ VOP BT1120 D6	/ GMAC1 RXD5 M0	/ I2S3 SDI M1	/ SDMMC2 PWREN M1	/ GPIO3 A7 D
LCDC D15	/ VOP BT1120 D6	/ ETH1 REPC10 Z5M M0	/ SDMMC2 PWREN M1	/ SDMMC2 PWREN M1	/ GPIO3 B0 D
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 D
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 D
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXD0 CHS M0	/ I2C5 SCL M2	/ PWM SDI0 M2	/ GPIO3 B3 D
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXD6 M0	/ I2C5 SDA M2	/ PWM SDI1 M2	/ GPIO3 B4 D
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 D
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 D
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SDI2 M2	/ GPIO3 B7 D
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SDI3 M2	/ GPIO3 C0 D
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SD02 M2	/ GPIO3 C1 D
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SD03 M2	/ GPIO3 C2 D
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 D
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 D
PWM15 TX M0	/ SPDIF TX M1	/ GMAC1 MDIO M0	/ UART7 RX M1	/ I2S1 LCLK RX M2	/ GPIO3 C5 D

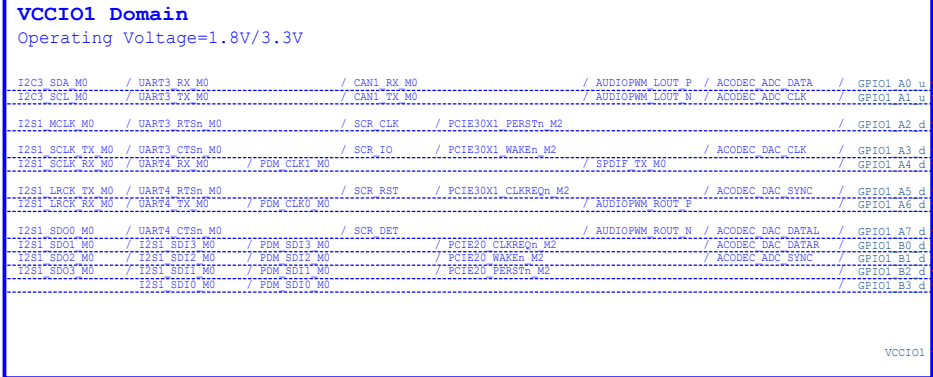
U11L
RK3568
bga636_19r00x19r00x1r20

AG6	PCIE20_CLKREQn_M1	[29]
AD7	PCIE20_WAKEn_M1	[29]
AC8	GMAC0_INT	GPIO2_D2
AC7	GMAC0_RSTn	GPIO2_D3
AF5	ZG5_PHY1_RST	GPIO2_D4
AD6	ZG5_PHY2_RST	GPIO2_D5
AD6	GPIO2_D6	[30]
AH5	GPIO2_D7	[30]
AH4	GPIO3_A0	[30]
AB8	GMAC1_INT	GPIO3_A1
AB5	GMAC1_RSTn	GPIO3_A2
AG4	CTP1_INT	GPIO3_A3
AF4	CTP1_RST	GPIO3_A4
AH3	GPIO3_A5	[30]
AG3	GPIO3_A6	[30]
AH2	GPIO3_A7	[30]
AG2	GPIO3_B0	[30]
AG1	PWM8_M0	[30]
AF2	PWM9_M0	[30]
AF1	I2C5_SCL_M0	[25, 30]
AE1	I2C5_SDA_M0	[25, 30]
AE2	PWM10_M0	[30]
AB3	GPIO3_B6	[30]
AD4	UART3_TX_M1	[30]
AD2	UART3_RX_M1	[30]
AD1	PCIE20_PERSTn_M1	[29]
AA7	MINIPCI0_nWDSISABLE	GPIO3_C2
AC4	LC01_RST	GPIO3_C3
AC3	PWM14_M0	[30]
AC2	GPIO3_C5	[30]

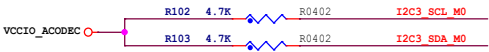
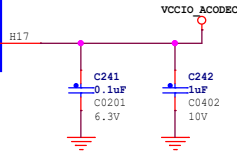
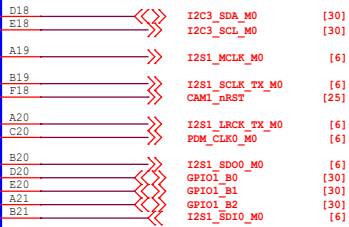


东莞野火电子技术有限公司 https://yehuoem.taobao.com		
Title 野火_RK3568 LubanCat 2 N_原理图		
Size A3	Document Number V0 Interface_2	Rev V3R0
Date: Friday, March 22, 2024	Sheet 17 of 29	

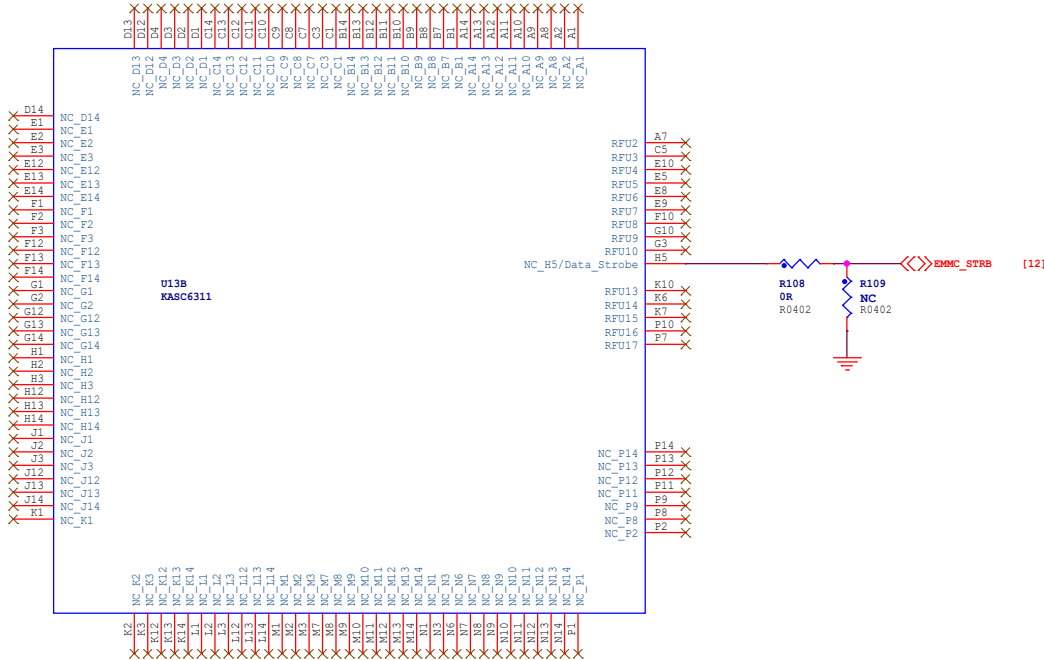
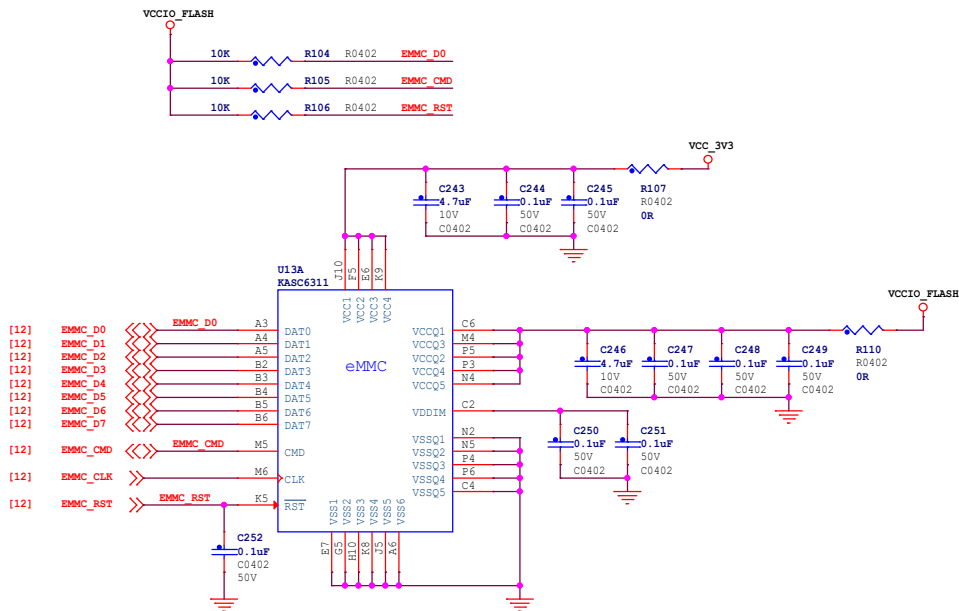
RK3568 VCCIO1 Domain



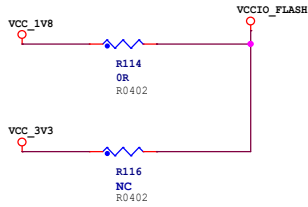
U11H
RK3568
bga636_19r00x19r00x1r20



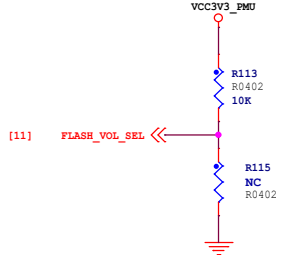
EMMC FLASH



EMMC_IO_Toggle



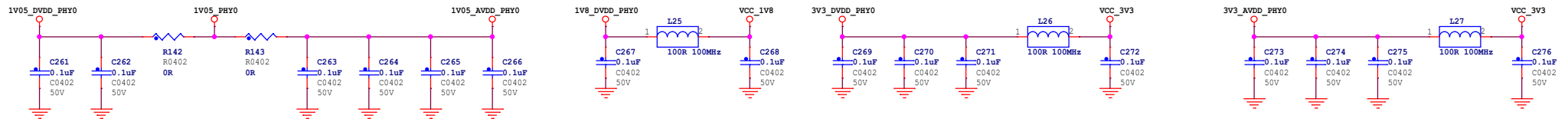
FLASH_VOL_SEL



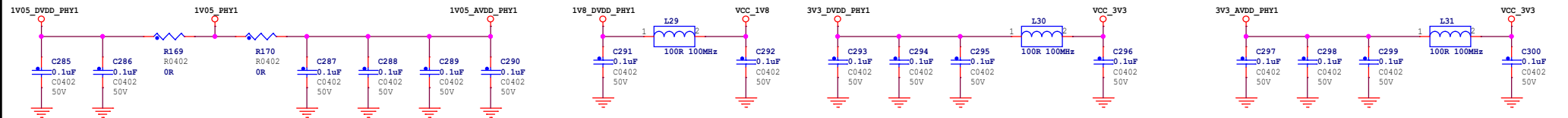
Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

Title		
野火_RK3568 IubanCat 2 N_原理图		
Size	Document Number	Rev
A3	EMMC_FLASH	V3R0
Date:	Friday, March 22, 2024	Sheet 19 of 29

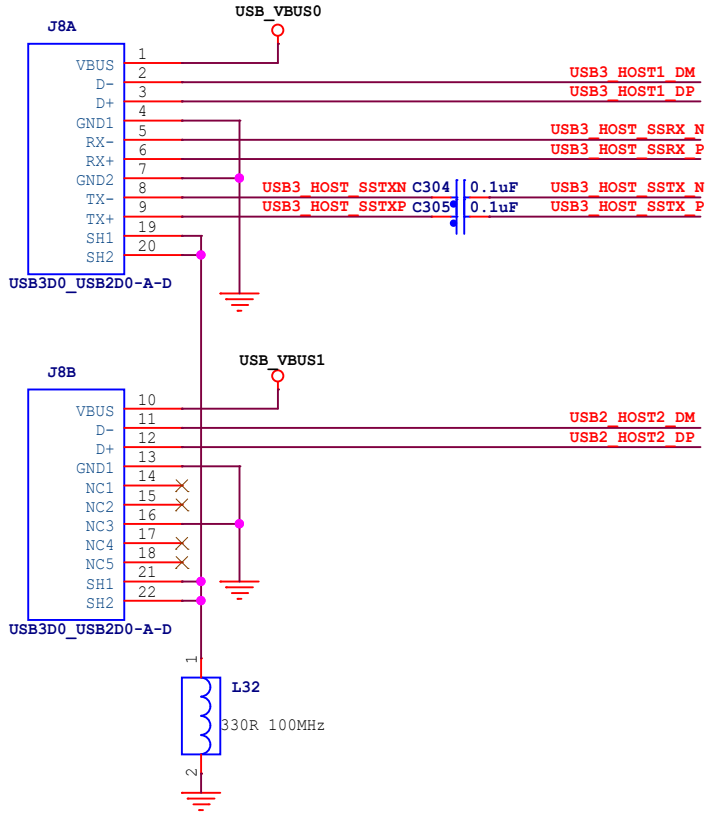
PHY Address : 001



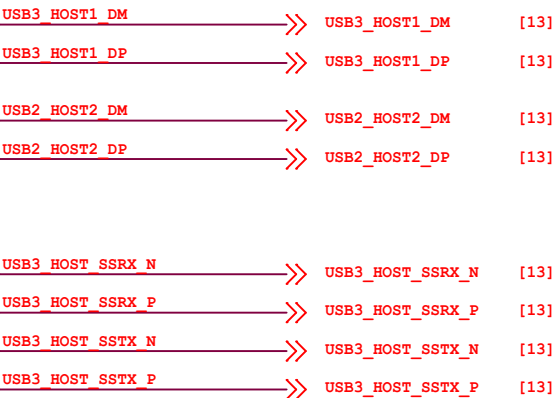
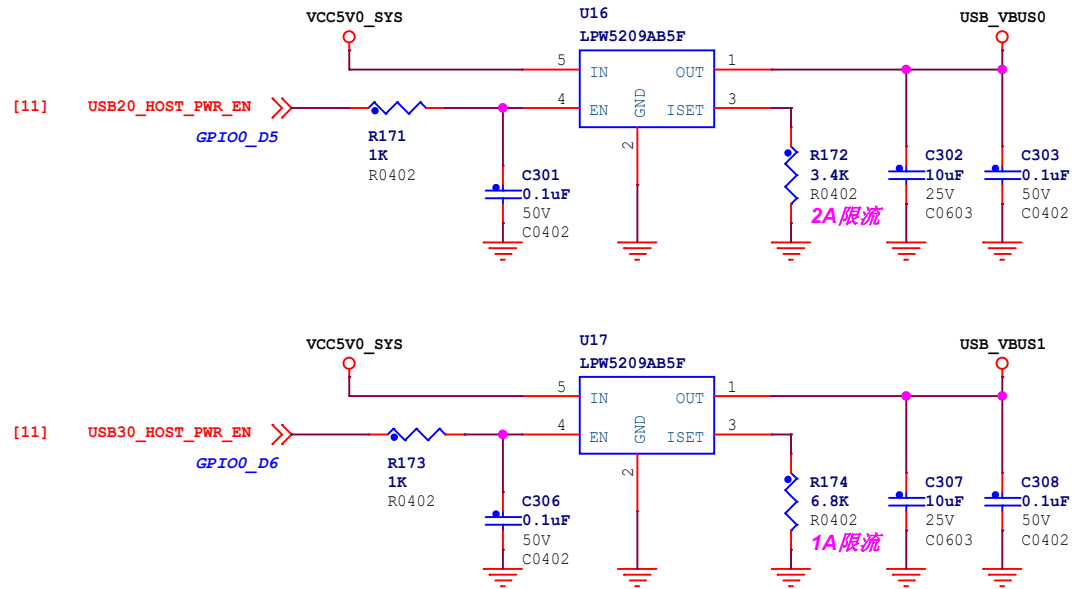
PHY Address : 010



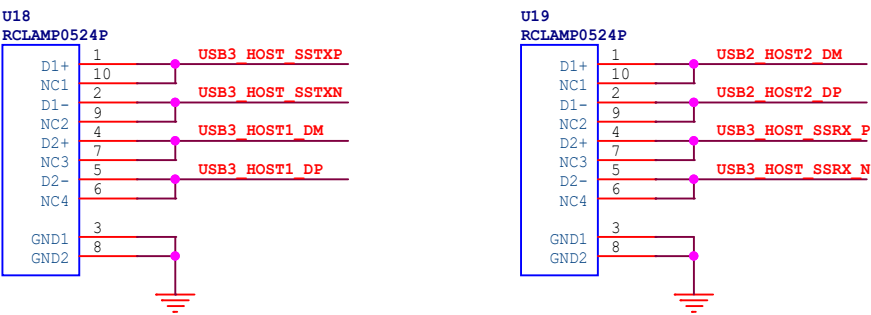
USB 3.0 HOST x1
USB 2.0 HOST x1



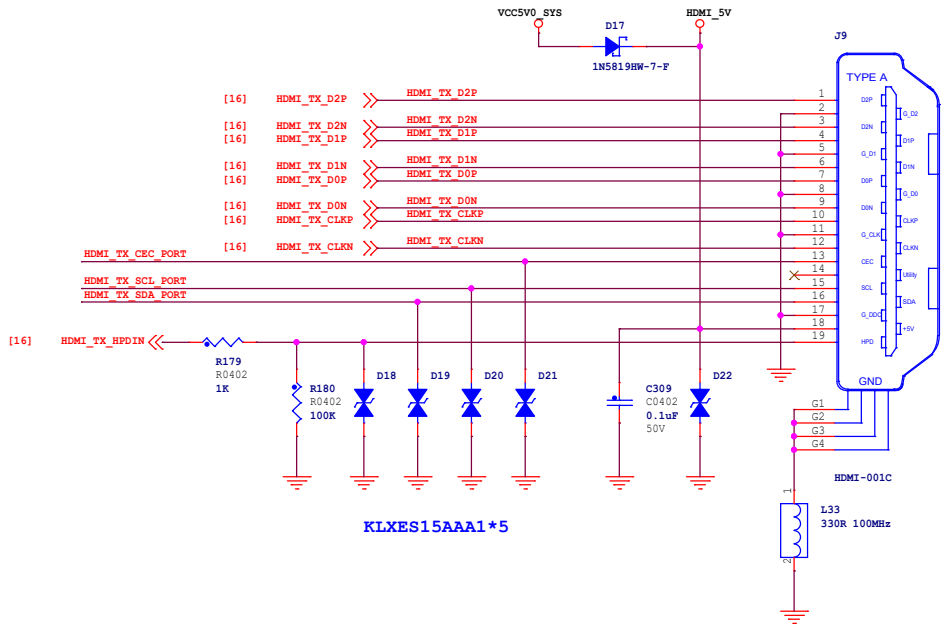
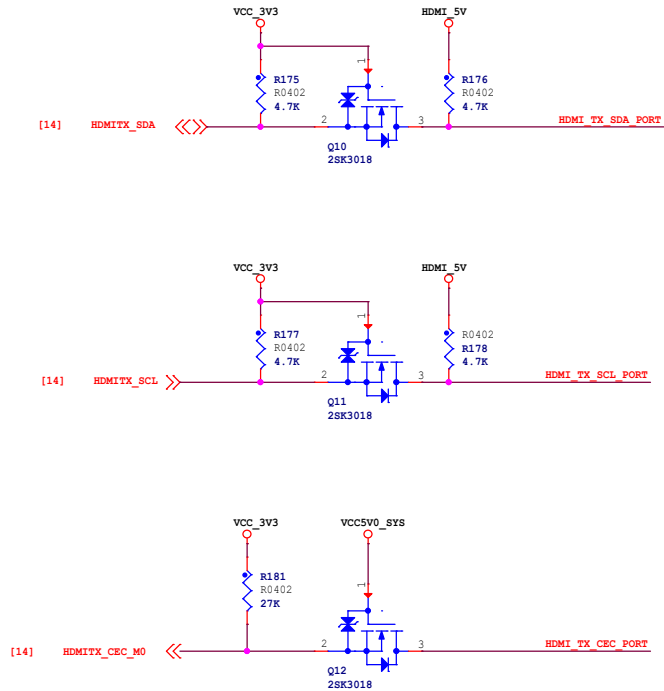
USB POWER



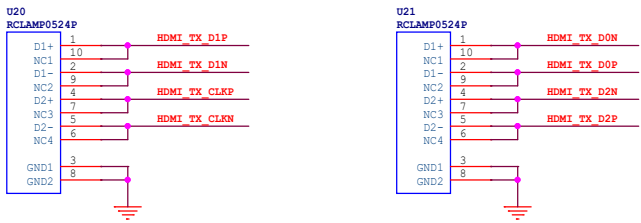
ESD



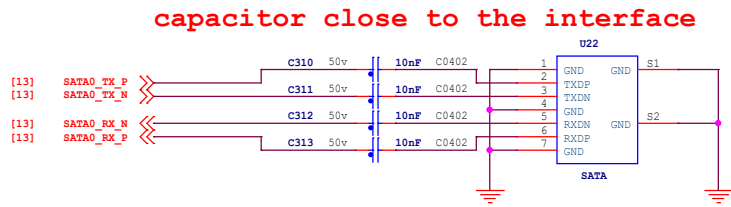
HDMI_PORT



HDMI_ESD

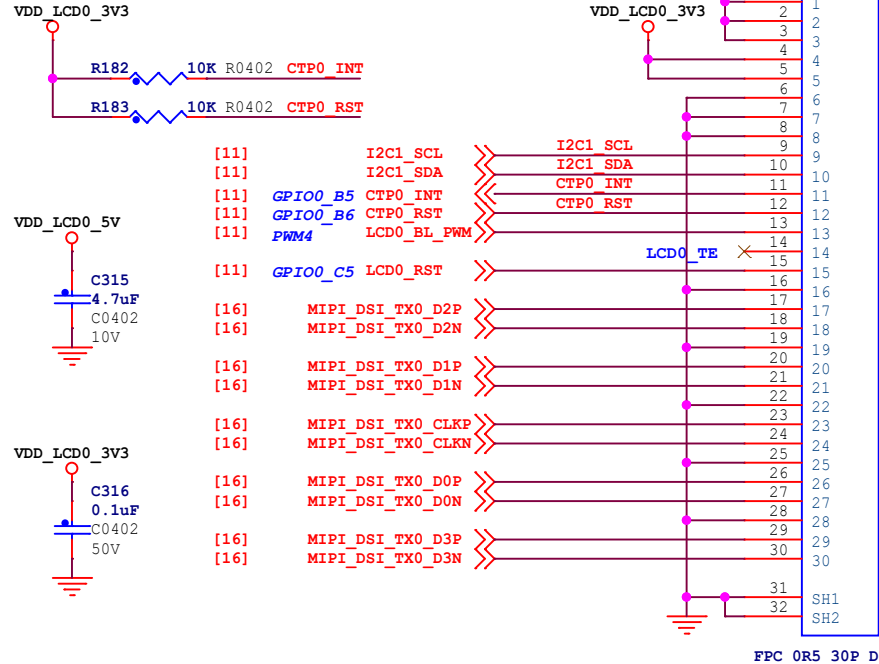


SATA_PORT

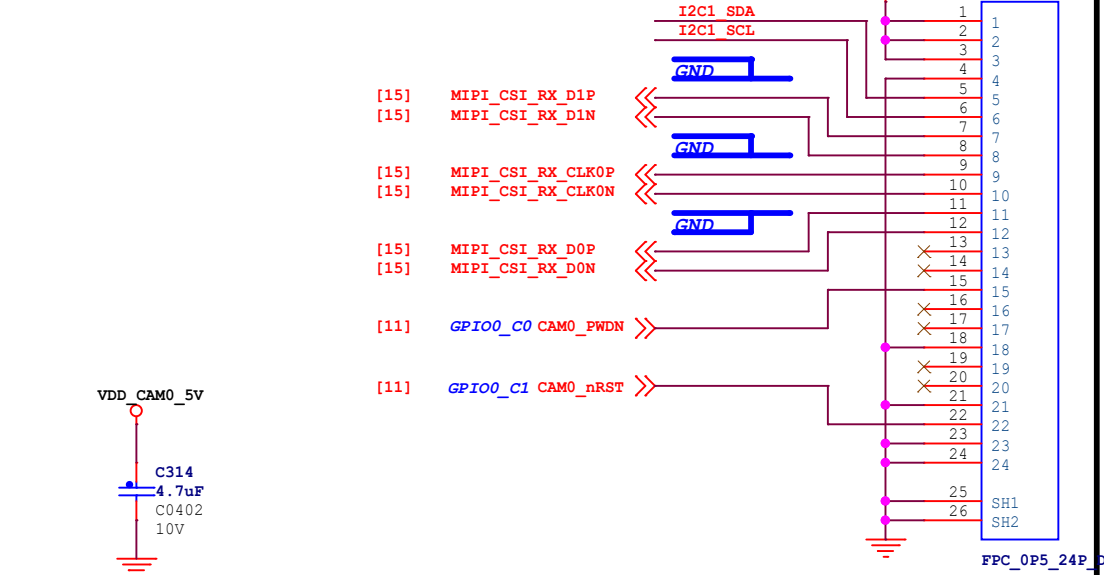


东莞野火电子有限公司 https://yehuosm.tmall.com		
Title 野火_RK3568 LubanCat 2 N_原理图		
Size A3	Document Number HDMI_PORT/SATA_PORT	Rev V3R0
Date: Friday, March 22, 2024	Sheet 23	of 29

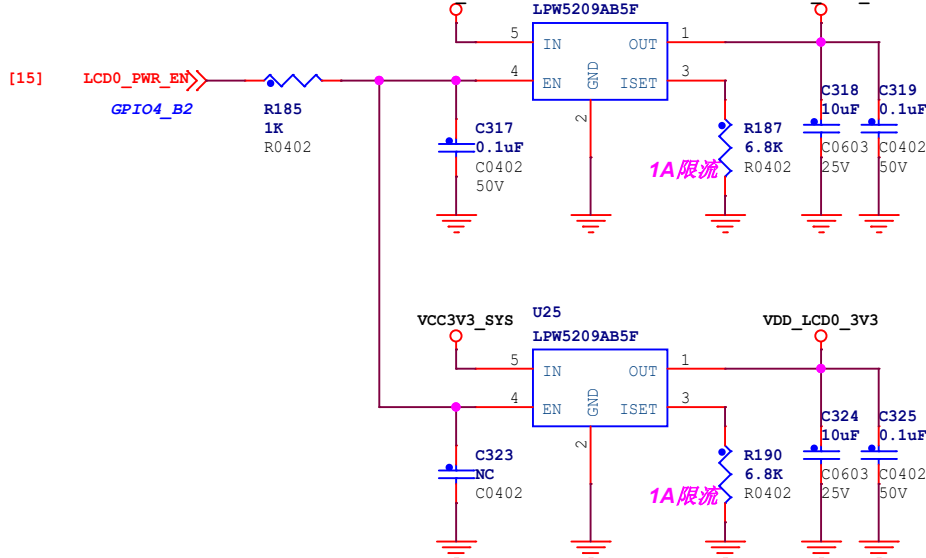
MIPI DSI LCD PORT 0



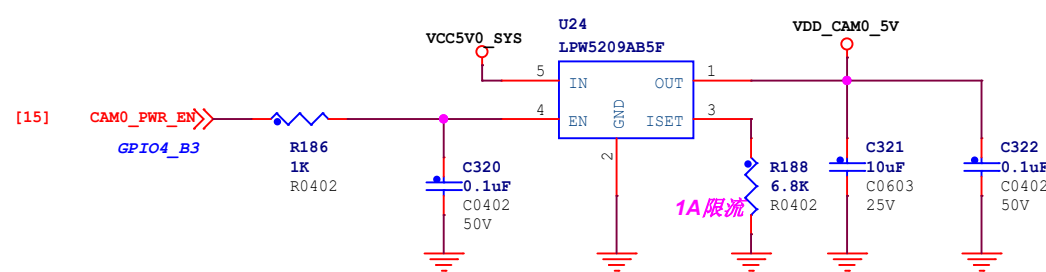
MIPI CSI PORT 0



LCD Power



MIPI CSI Power



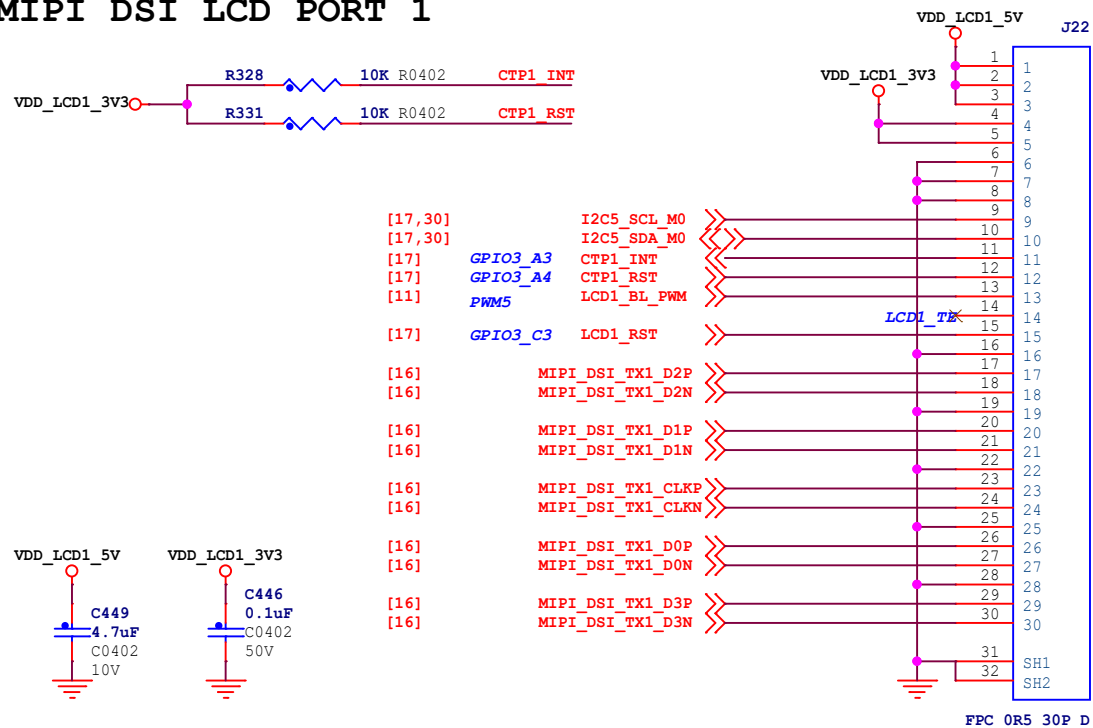
东莞野火电子技术有限公司
https://yehuosm.tmall.com

Title 野火_RK3568 LubanCat 2 N_原理图

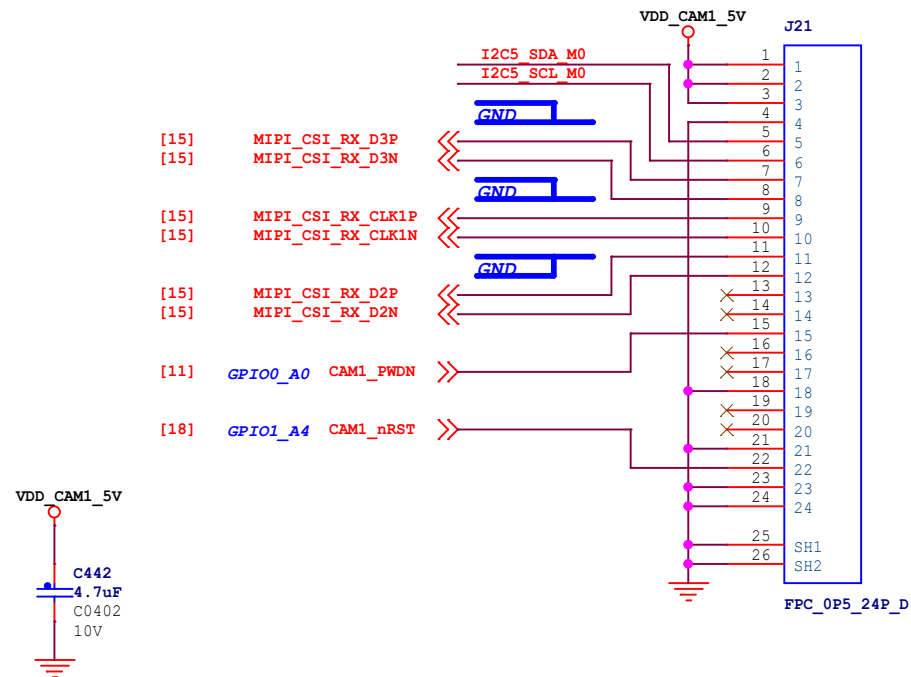
Size A4 Document Number MIPI DSI/MIPI CSI_PORT Rev V3R0

Date: Friday, March 22, 2024 Sheet 24 of 29

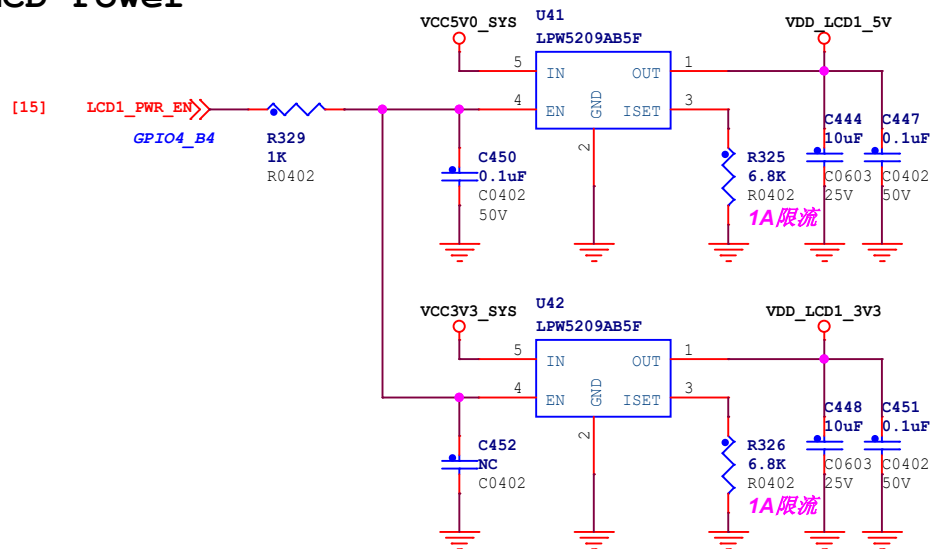
MIPI DSI LCD PORT 1



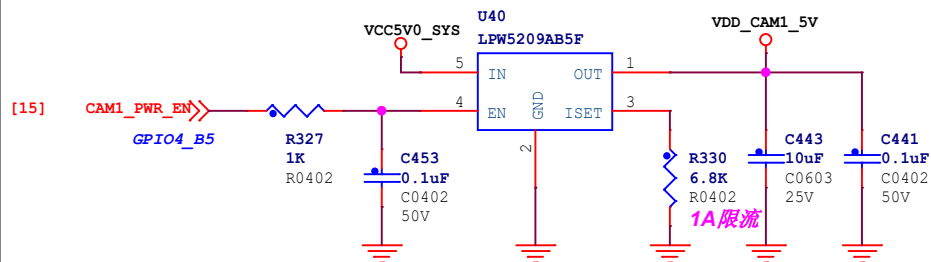
MIPI CSI PORT 1



LCD Power



MIPI CSI Power



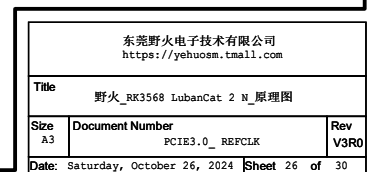
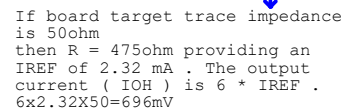
东莞野火电子技术有限公司
https://yehuosm.tmall.com

Title 野火_RK3568 LubanCat 2 N_原理图

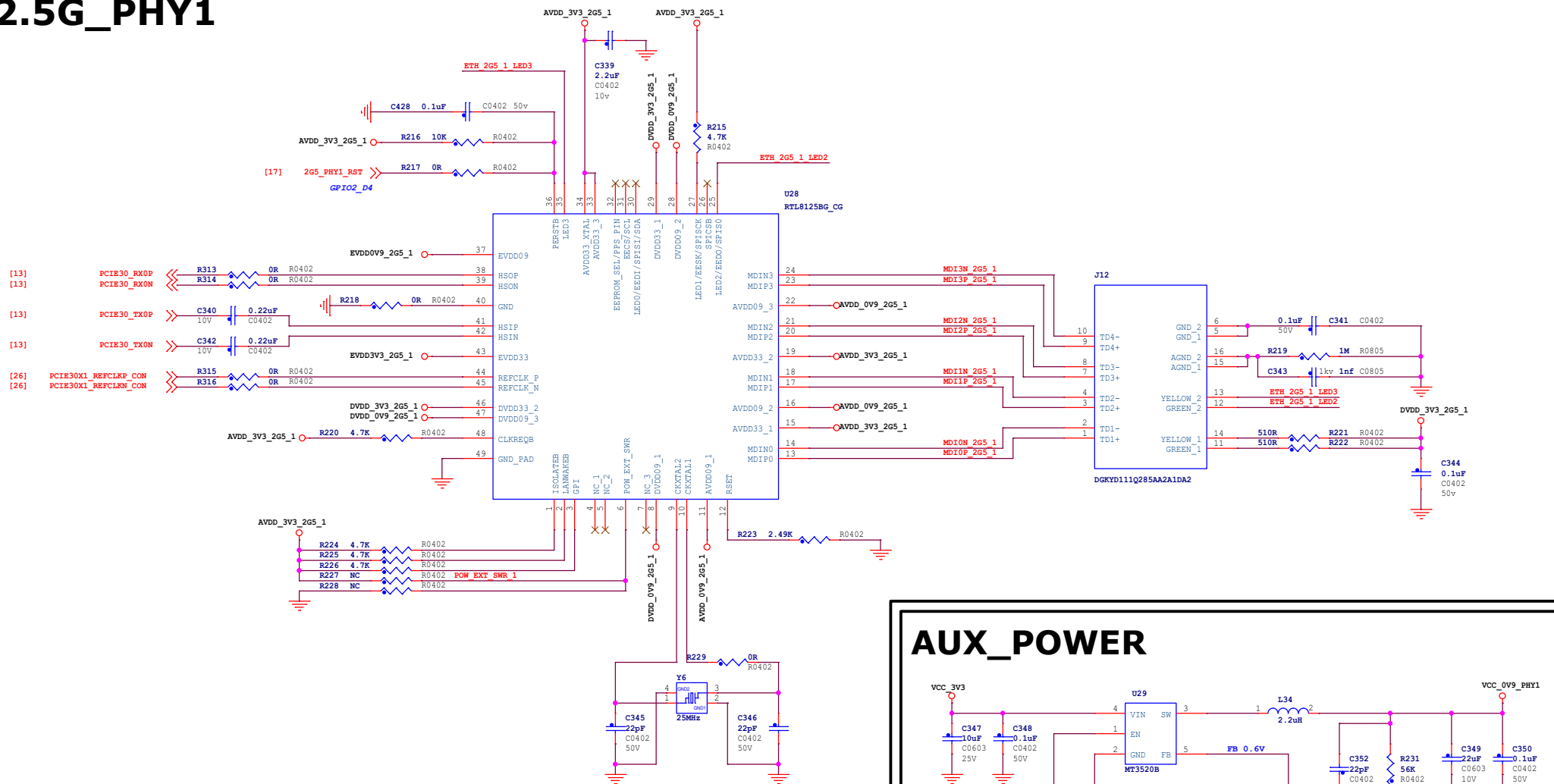
Size A4 Document Number MIPI DSI/MIPI CSI_PORT Rev V3R0

Date: Friday, March 22, 2024 Sheet 25 of 30

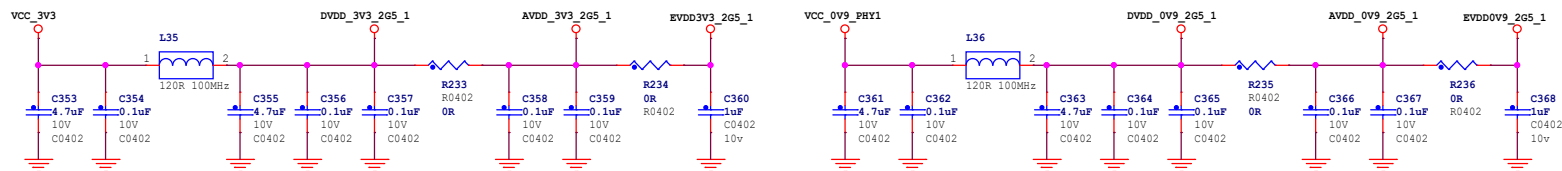
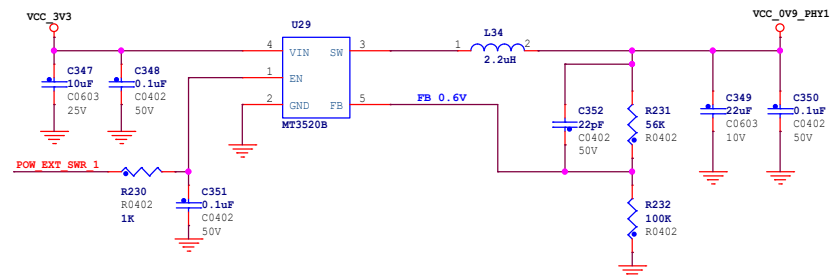
CLK*3 @100MHz



2.5G_PHY1



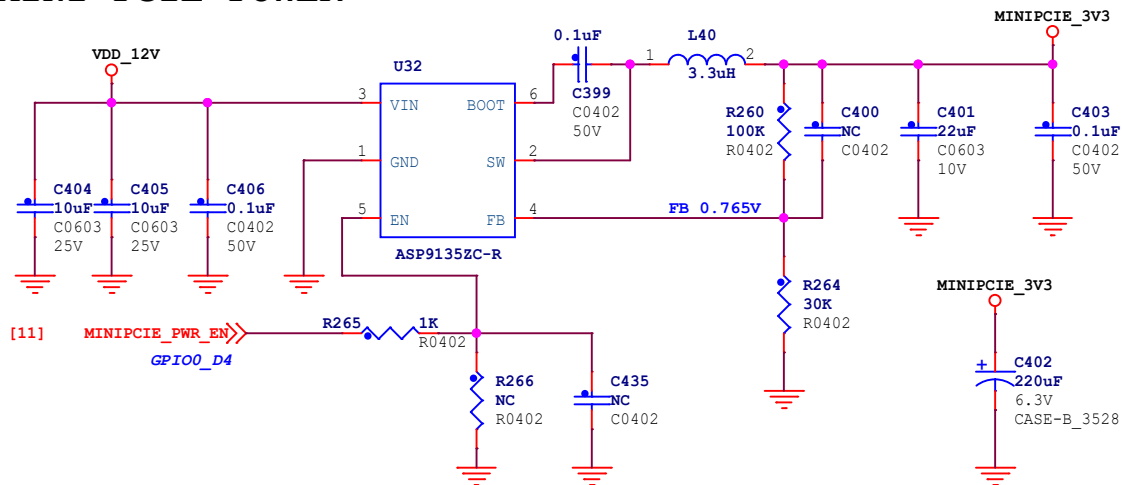
AUX_POWER



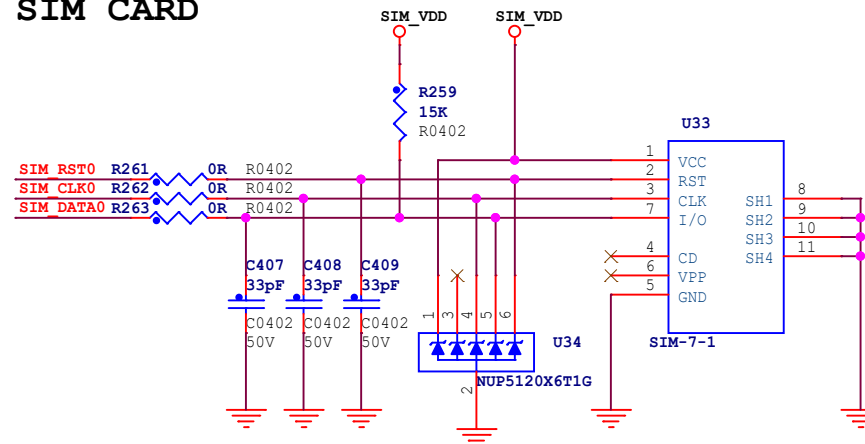
东莞野火电子科技有限公司
https://yehuosm.tmall.com

Title		
野火_RK3568 LubanCat 2 N_原理图		
Size A3	Document Number 2.5G_PHY1	Rev V3R0
Date: Friday, March 22, 2024	Sheet 27 of 30	

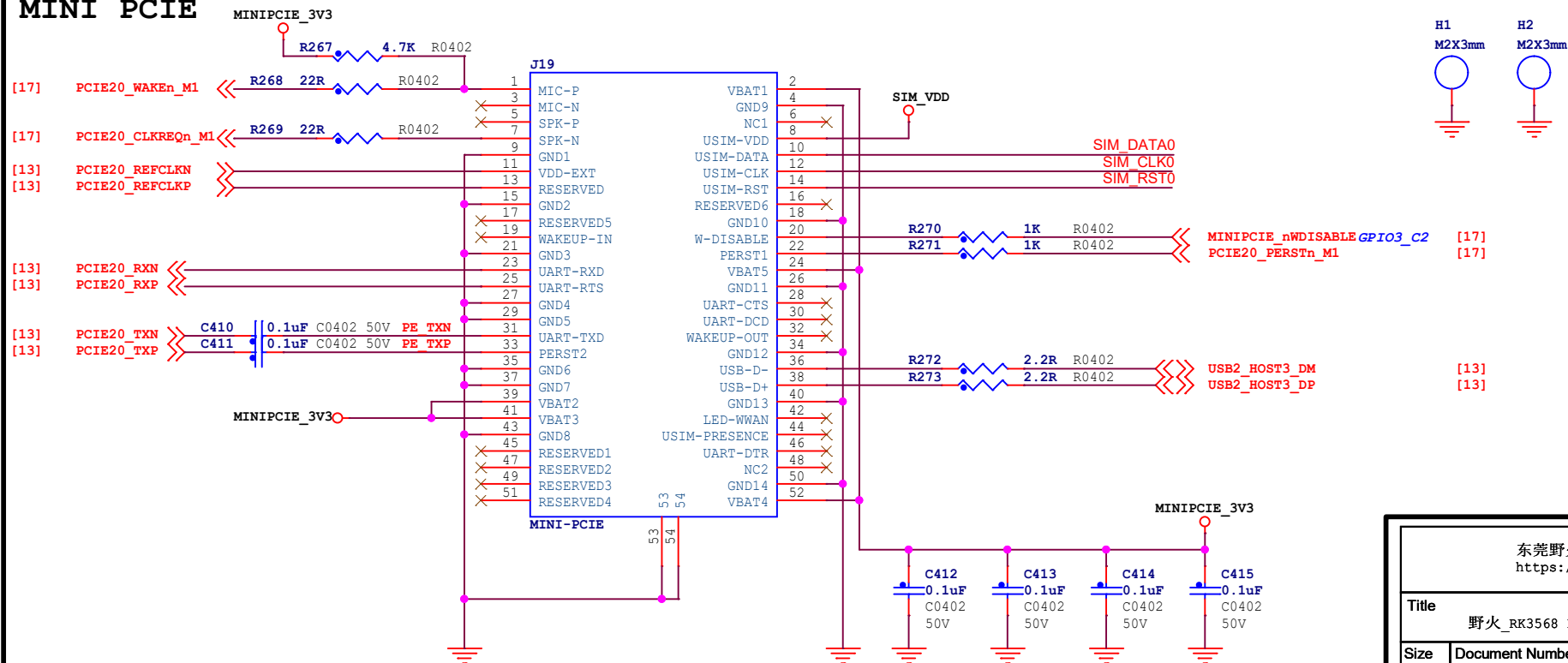
MINI PCIE POWER



SIM CARD

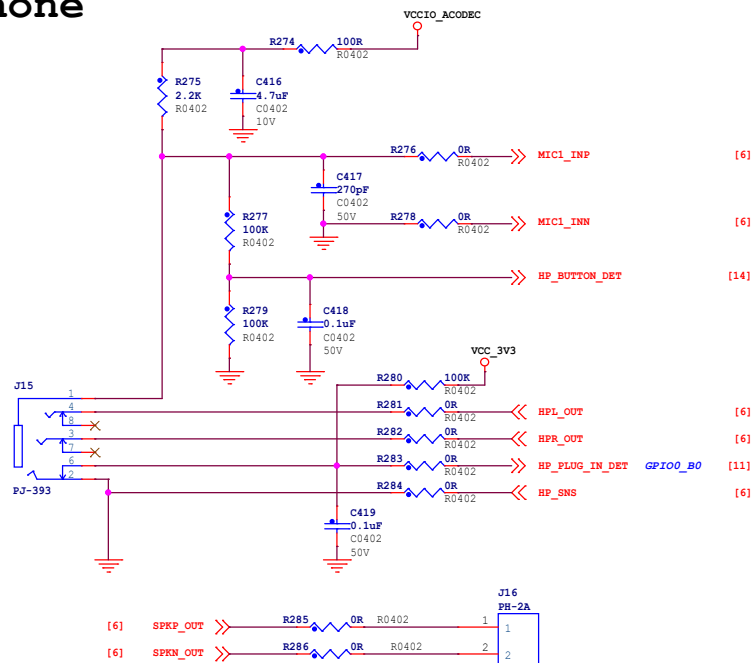


MINI PCIE

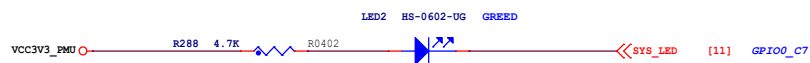


东莞野火电子技术有限公司 https://yehuosm.tmall.com		
Title 野火_RK3568 LubanCat 2 N_原理图		
Size A4	Document Number MINI PCIE_PORT	Rev V3R0
Date: Tuesday, October 22, 2024	Sheet 29	of 30

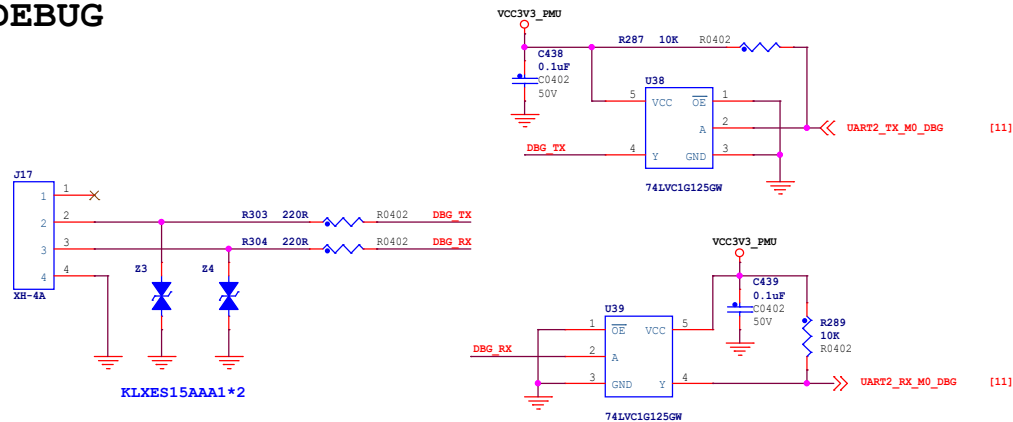
Earphone



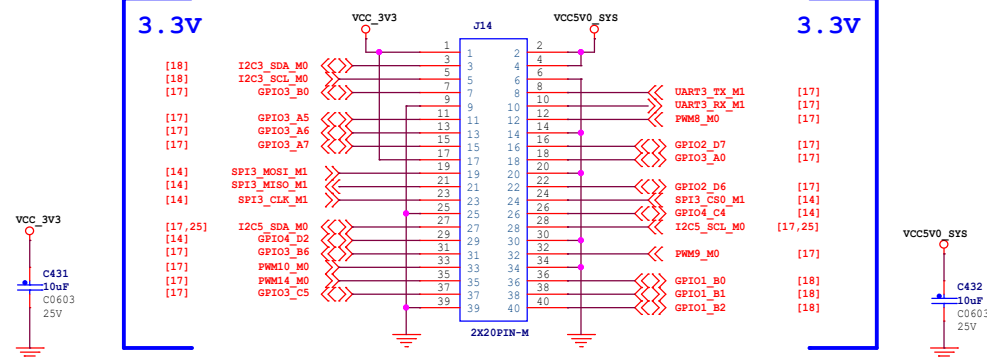
LED



DEBUG

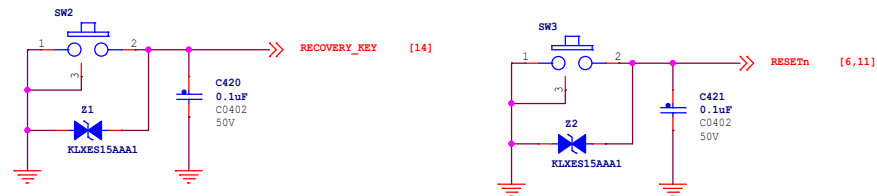


IO PORT

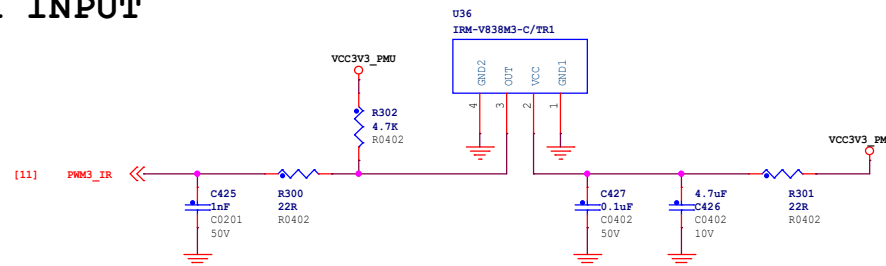


RECOVERY KEY

RESET KEY



IR INPUT



东莞野火电子技术有限公司
https://yehuosm.tmall.com

Title		
野火_RK3568 LubanCat 2 N_原理图		
Size	Document Number	Rev
A3	Earphone/DEBUG/IO_PORT/LED	V3R0
Date:	Friday, March 22, 2024	Sheet 30 of 30