



# 历史版本

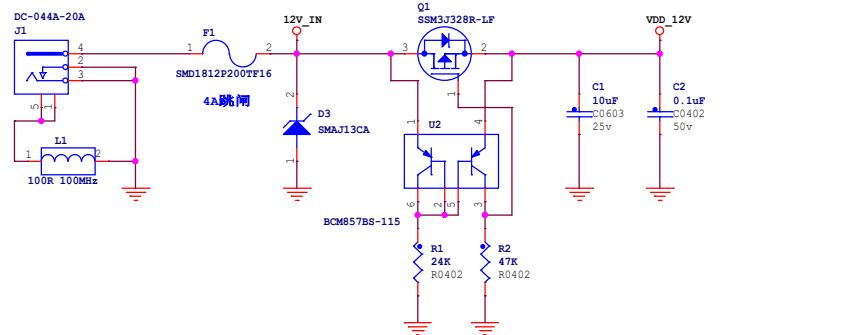
版本号	日期	设计	描述
V0.1	2022-05-05	ghs	初始版本
V1.0	2022-09-09	ghs	修正U27开启信号接反的问题，解决调试接口漏电的问题
V1.1	2022-09-09	ghs	修正BOARD ID的ID识别电阻的电源域，修正PHY芯片的复位引脚电压不匹配问题
V1.2	2022-12-13	ghs	增加网卡上拉电阻，更新mini pcie的固定螺丝柱

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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
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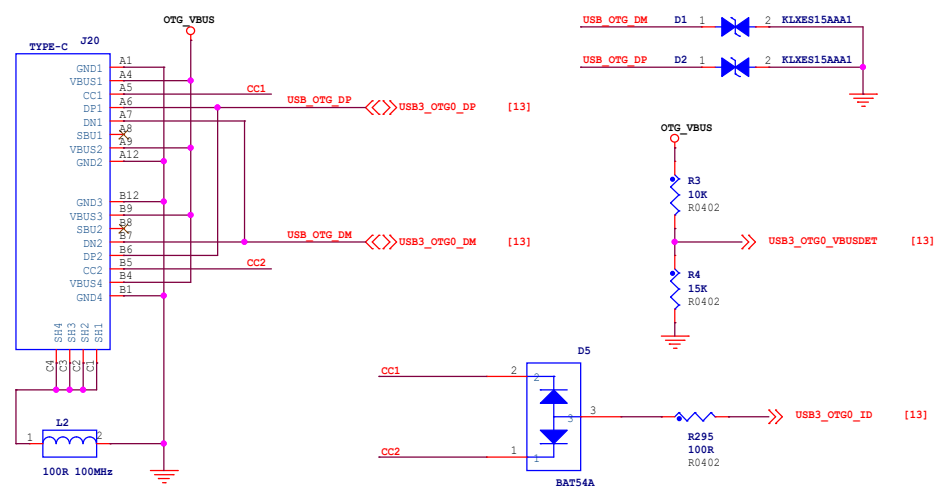


# DC 12V 3A POWER IN

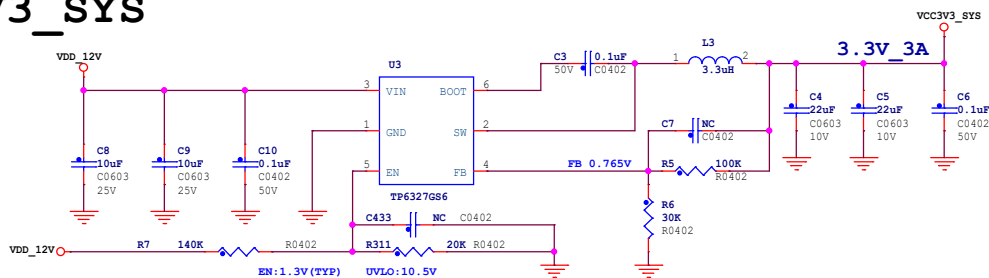
12V/3A



# OTG/Download

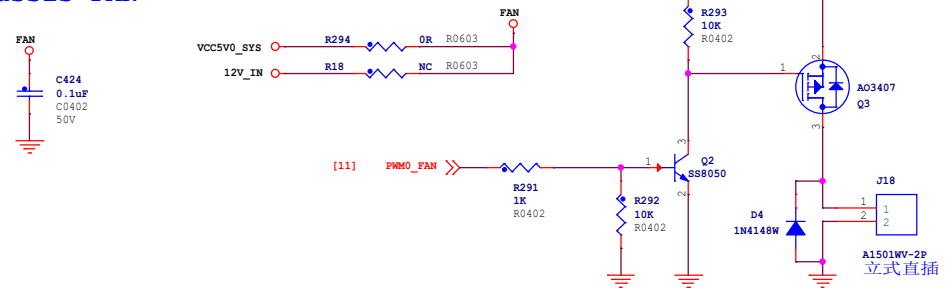


# 3V3\_SYS

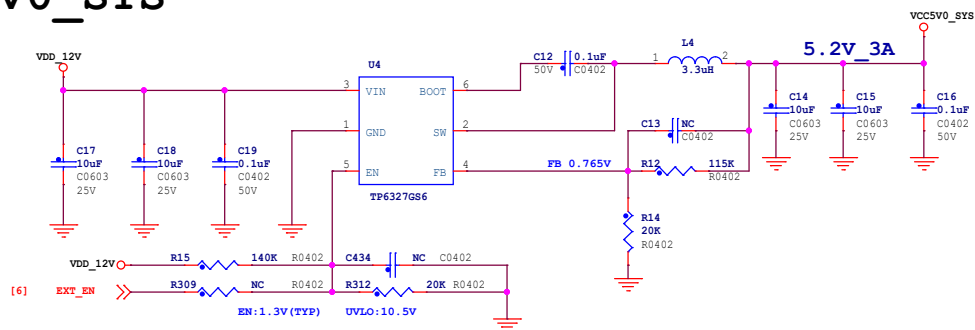


# Active Cooling

Chassis FAN

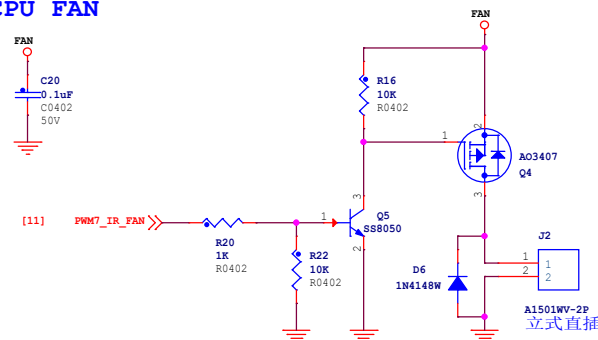


# 5V0\_SYS



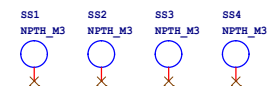
# Active Cooling

CPU FAN

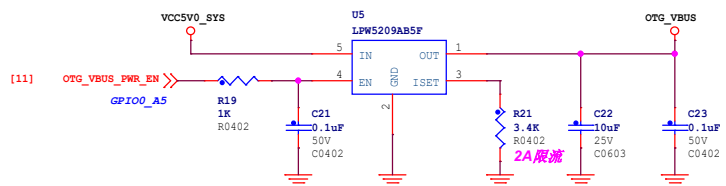


# Fix Hole

4\*M3



# OTG POWER



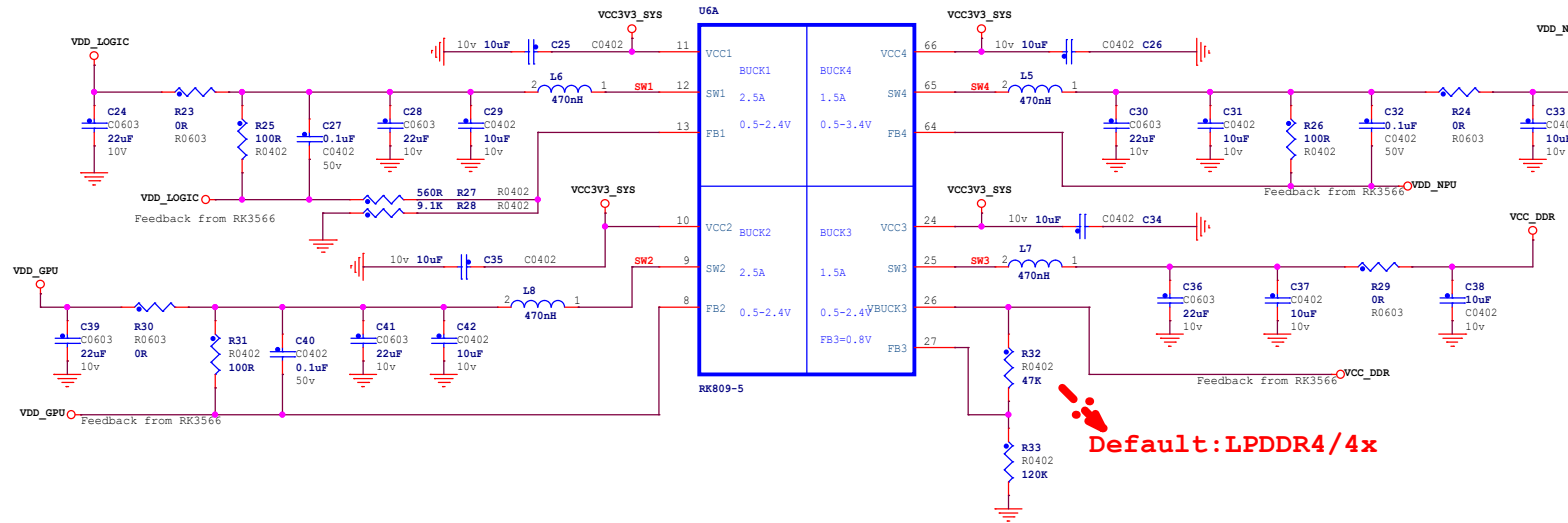
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Title 野火\_RK3568 LubanCat 2 N\_原理图\_V1.2

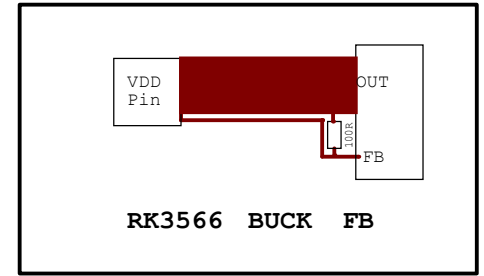
Size A3 Document Number DC\_IN/OTG\_Download Rev V1.2

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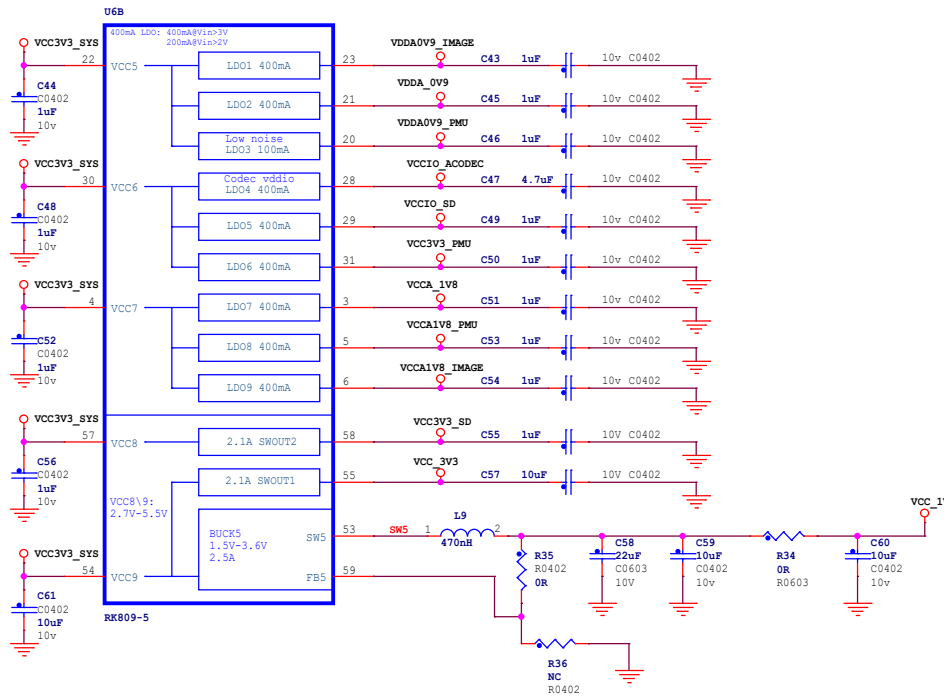
# PMIC RK809 DCDC



Default: LPDDR4/4x

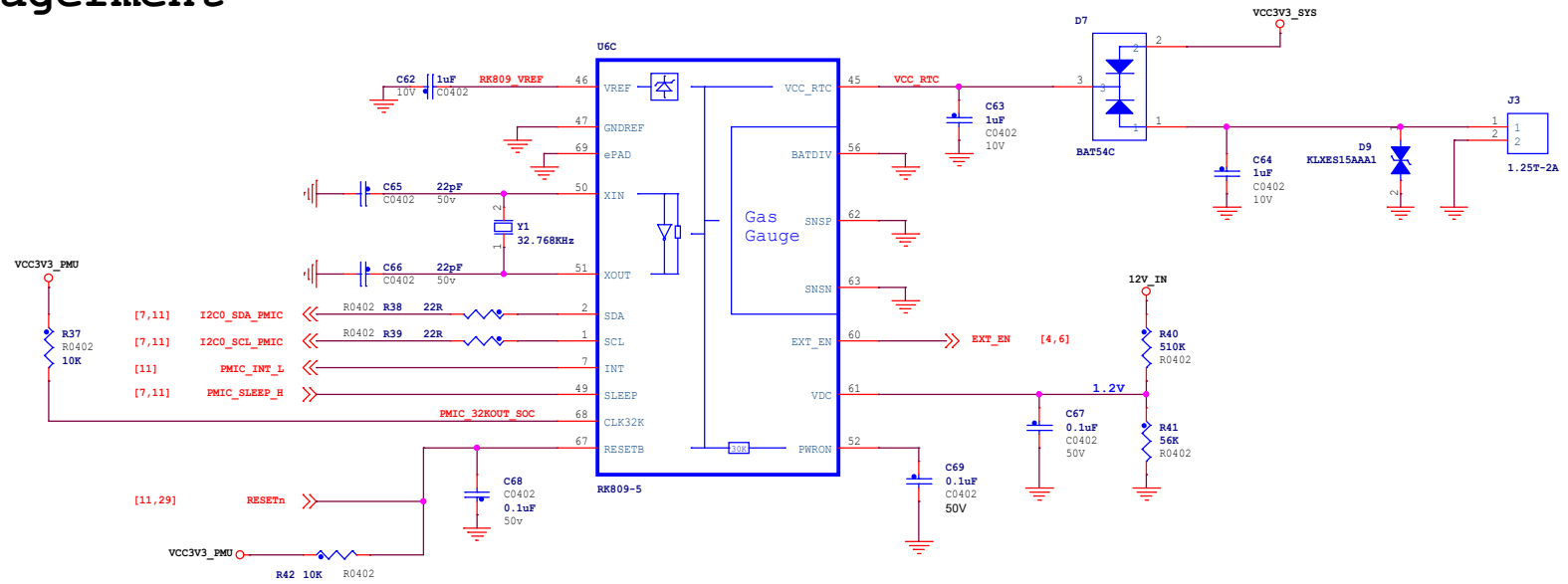


# PMIC RK809 LDO

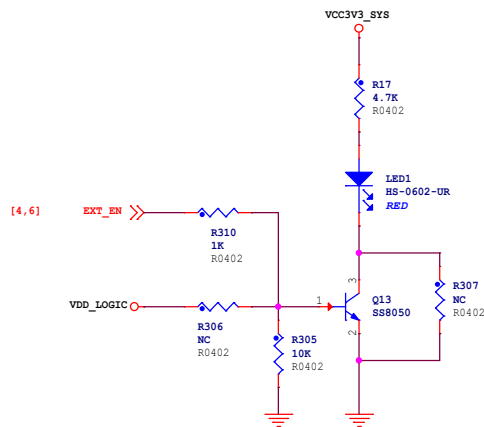


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Title 野火_RK3568 LuBanCat 2 N_原理图_V1.2		
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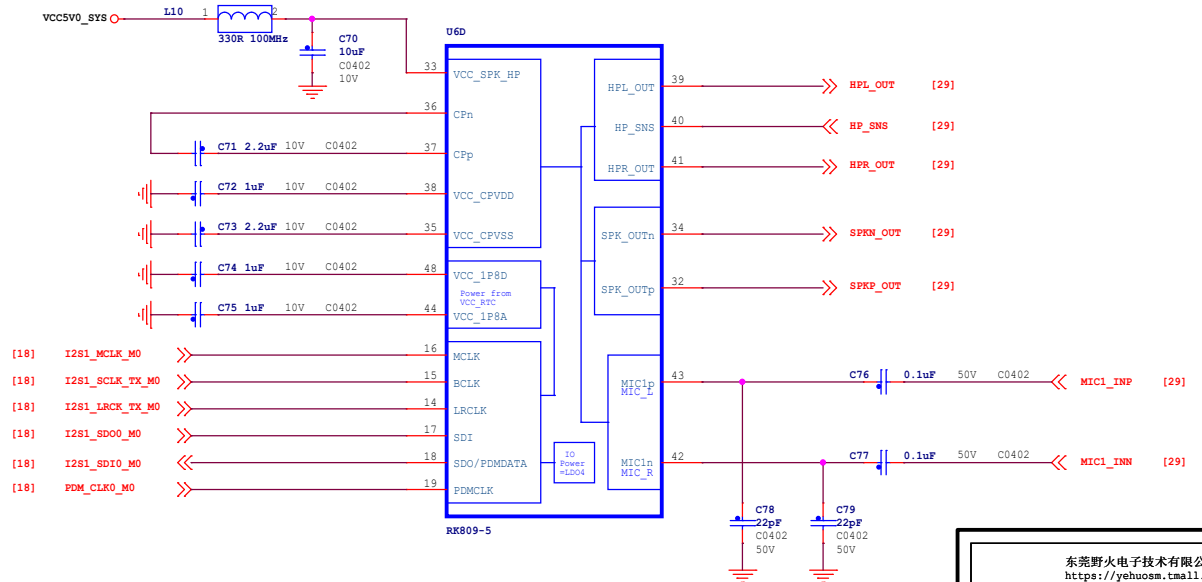
# PMIC RK809 Management



# PWR\_LED



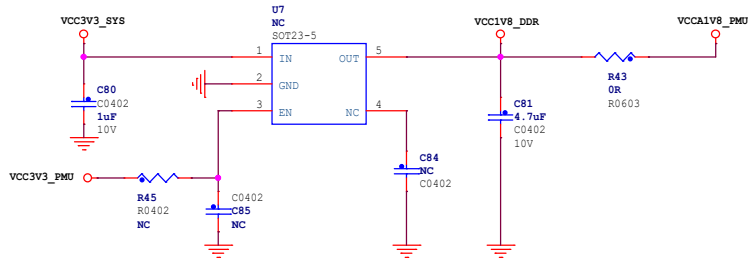
# PMIC RK809 CODEC



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Title	野火_RK3568 LubanCat 2 N_原理图_V1.2	
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A3	PMIC_Management/CODE	V1.2
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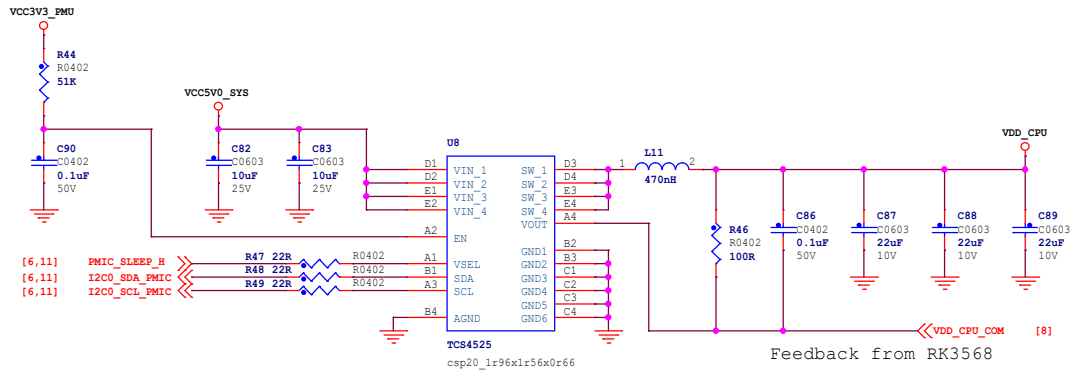
# Auxiliary power supply

LPDDR4\_VCC1V8\_DDR



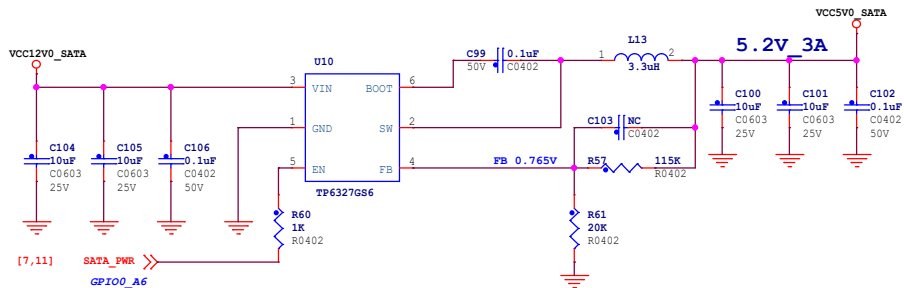
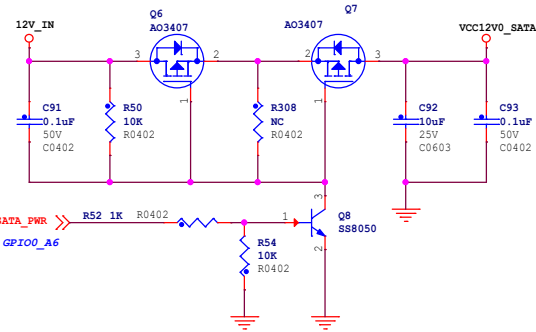
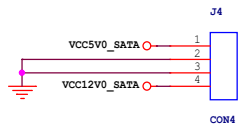
# RK3568 CPU Power

VDD\_CPU\_EXT



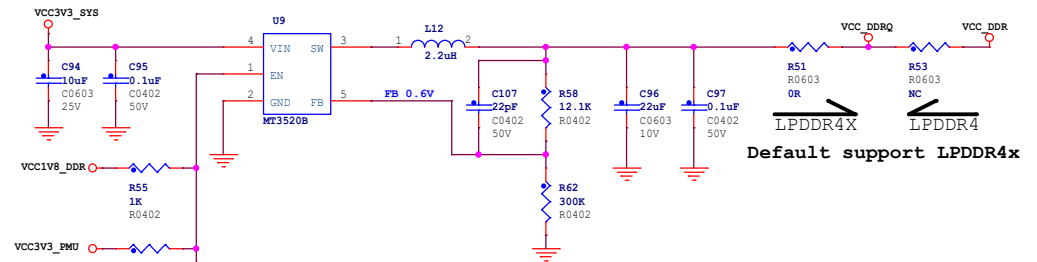
# SATA\_POWER

SATA\_5V0\_12V0\_POWER



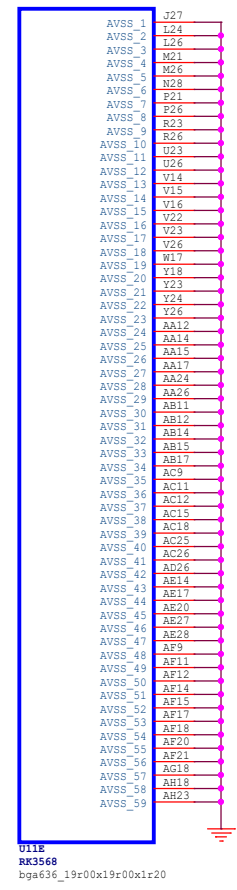
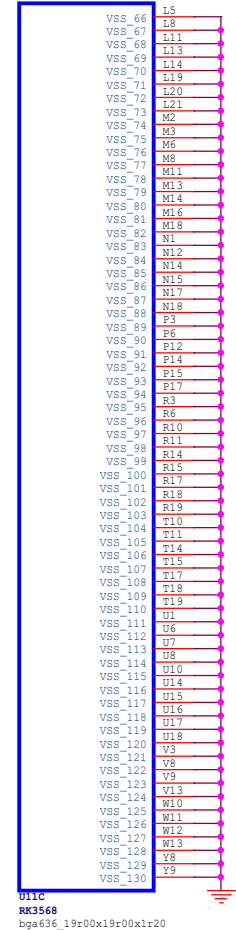
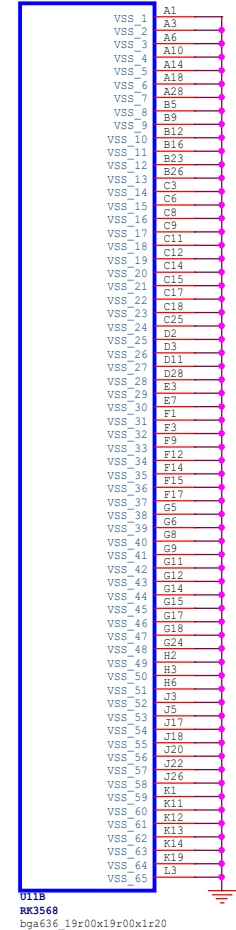
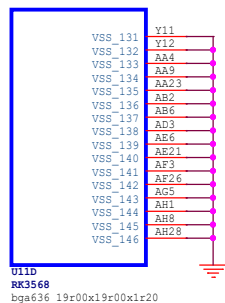
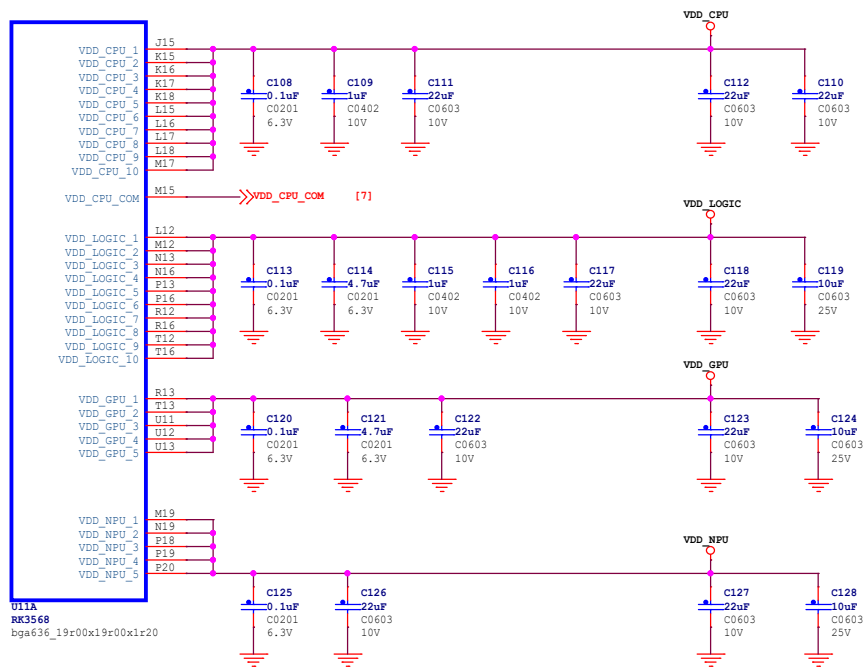
# LPDDR4x Power

output: 0.6V



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# RK3568 Power/GND

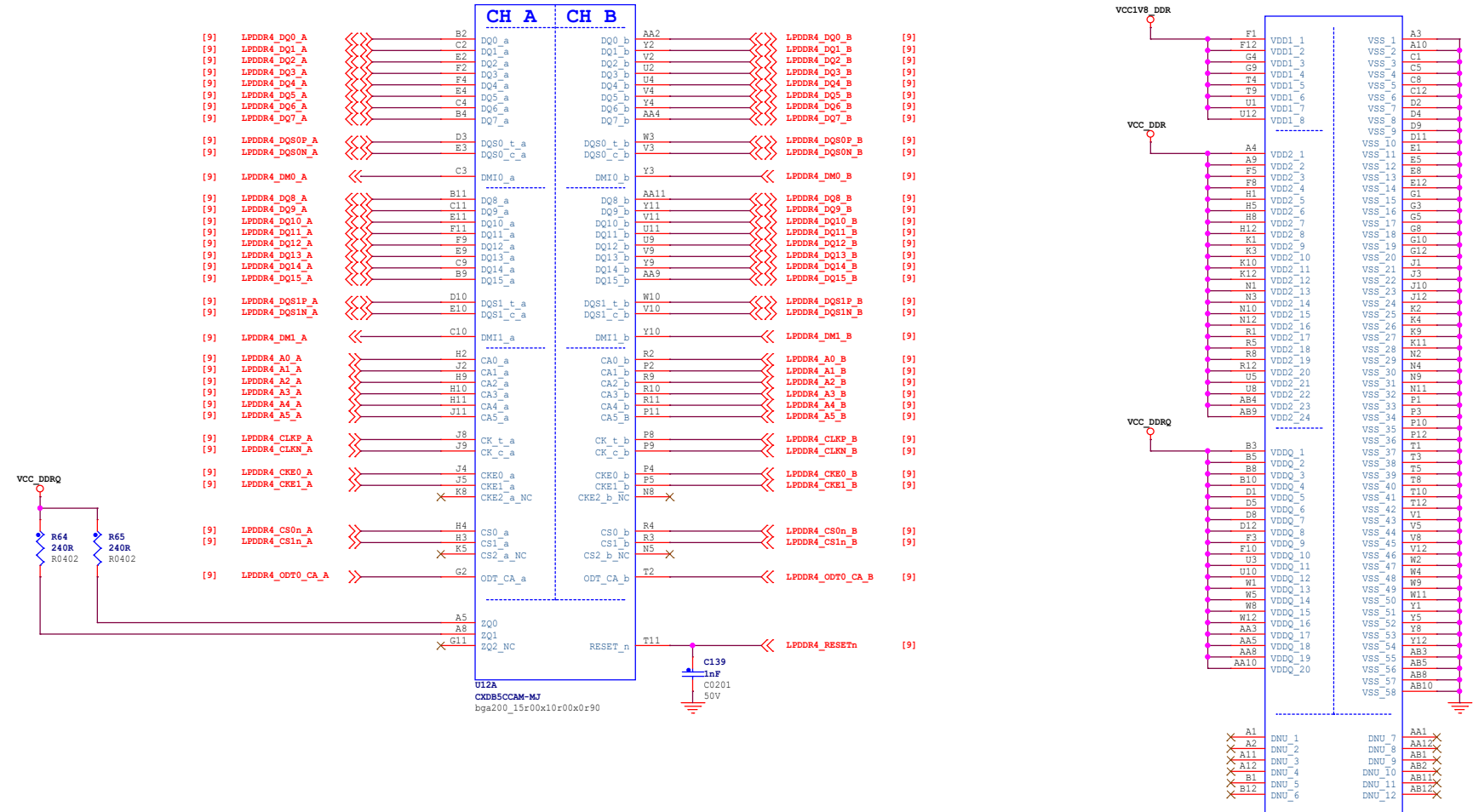


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Title	野火_RK3568 LubanCat 2 N_原理图_V1.2	
Size	Document Number	Rev
A3	RK3568_Power/GND	V1.2
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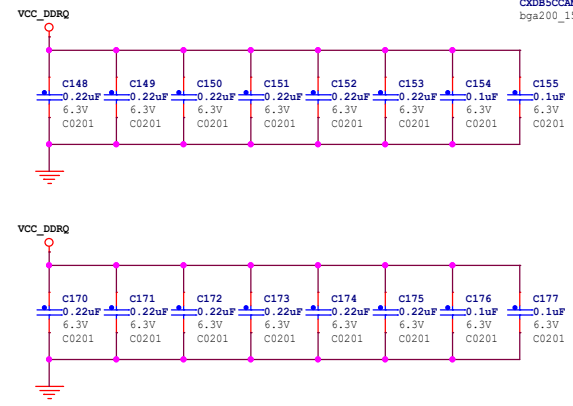
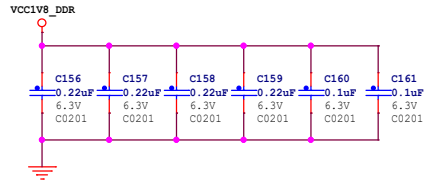
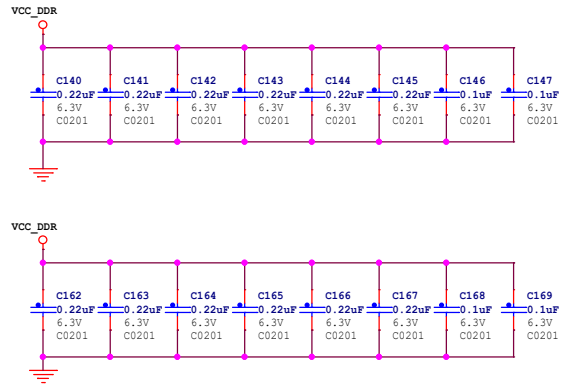
# LPDDR4/4x



U12A  
CXDB5CCAM-MJ  
bga200\_15x00x10r00x0r90

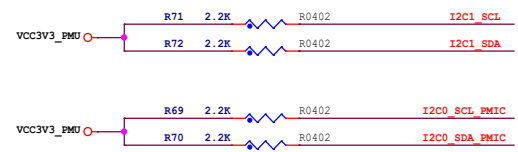
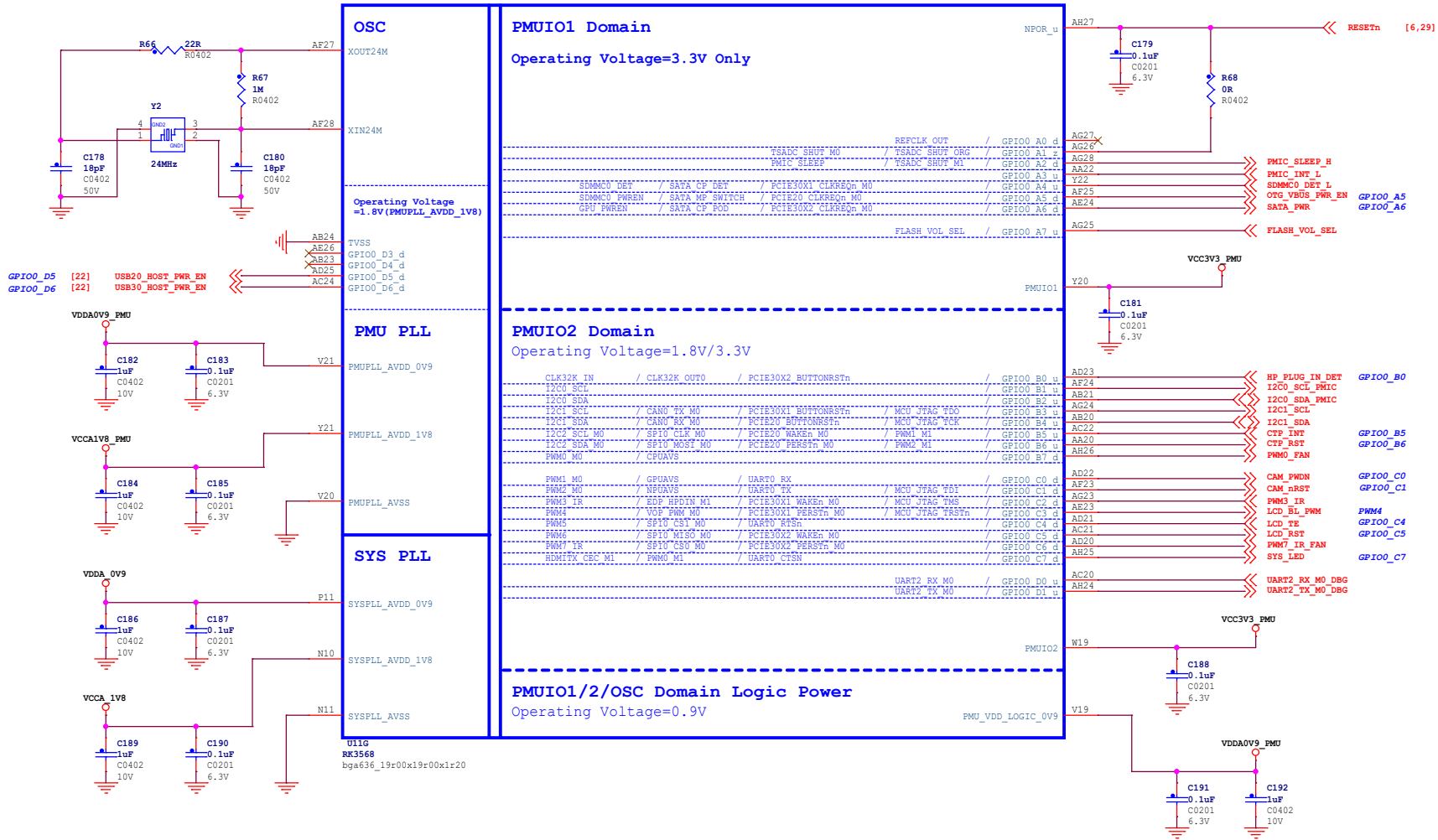
C139  
1nF  
50V

U12B  
CXDB5CCAM-MJ  
bga200\_15x00x10r00x0r90



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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number LPDDR4/4x	Rev V1.2
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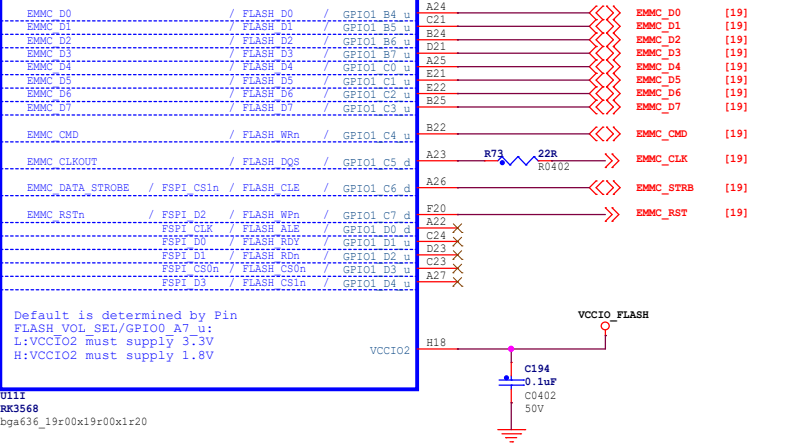
# RK3568 OSC/PLL/PMUIO



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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number OSC/PLL/PMUIO	Rev V1.2
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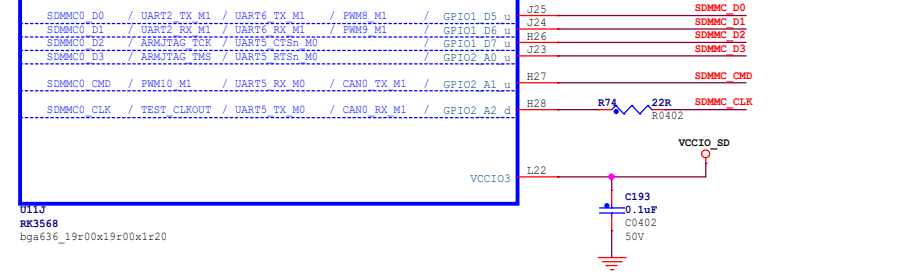
# RK3568 VCCIO2 Domain

VCCIO2 Domain  
Operating Voltage=1.8V/3.3V

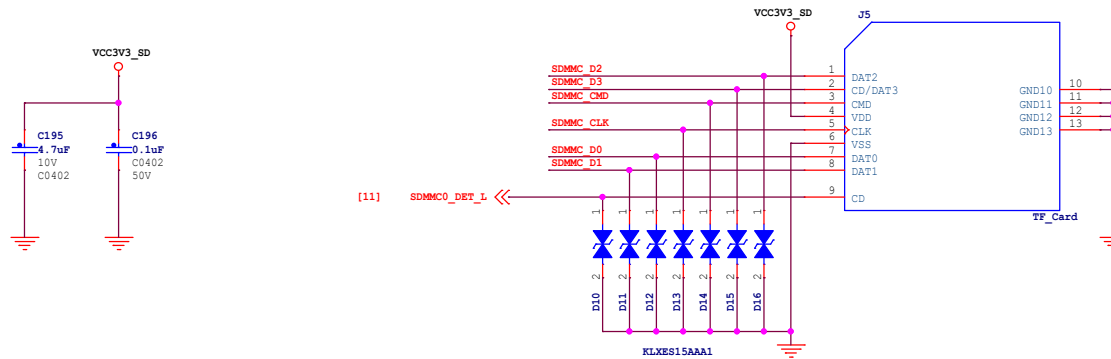


# RK3568 VCCIO3 Domain

VCCIO3 Domain  
Operating Voltage=1.8V/3.3V



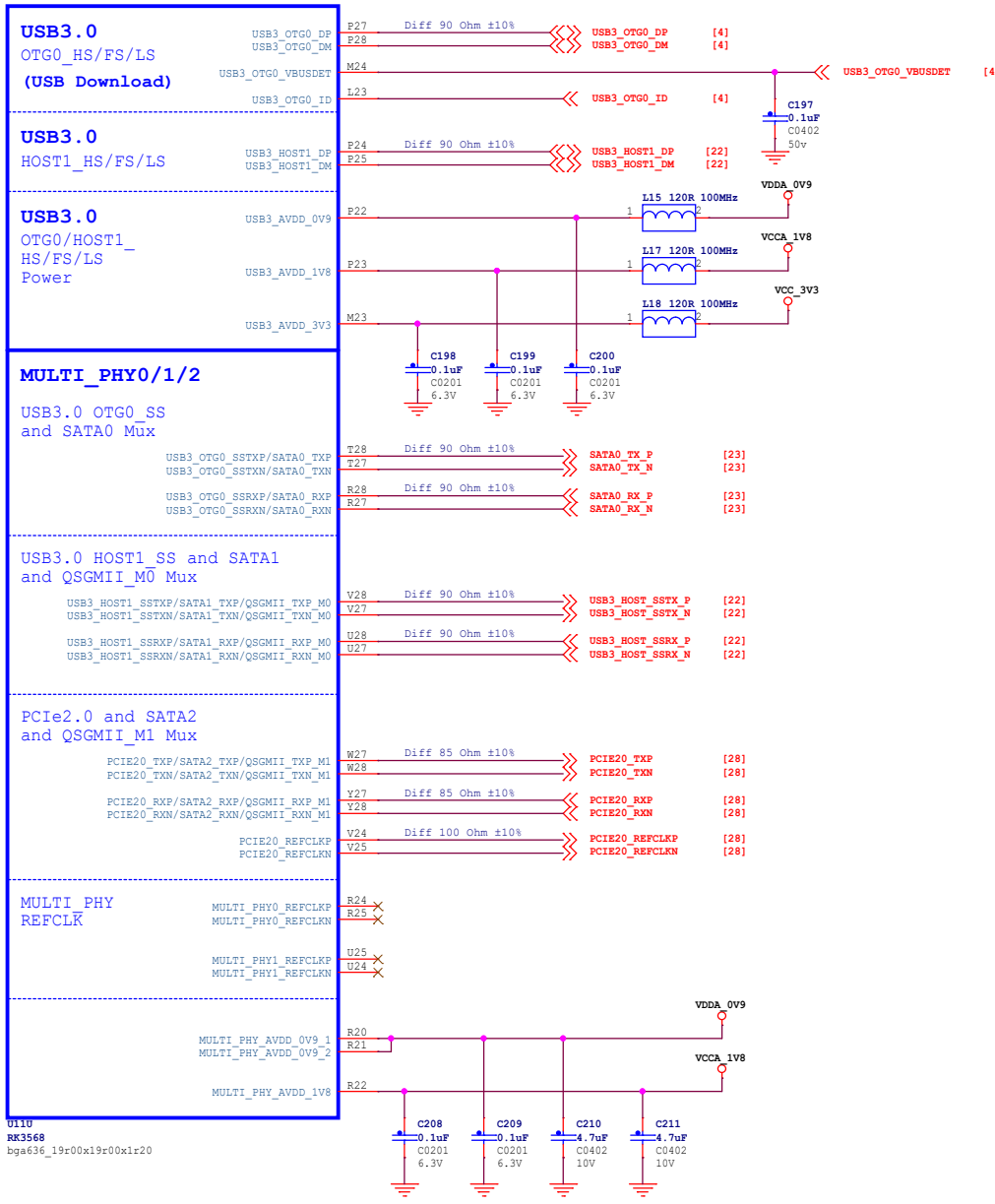
# TF\_CARD



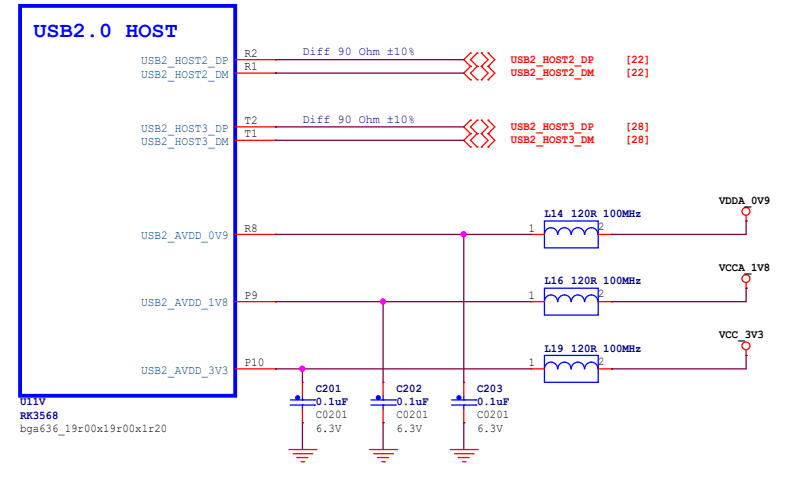
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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number Flash/SD Controller	Rev V1.2
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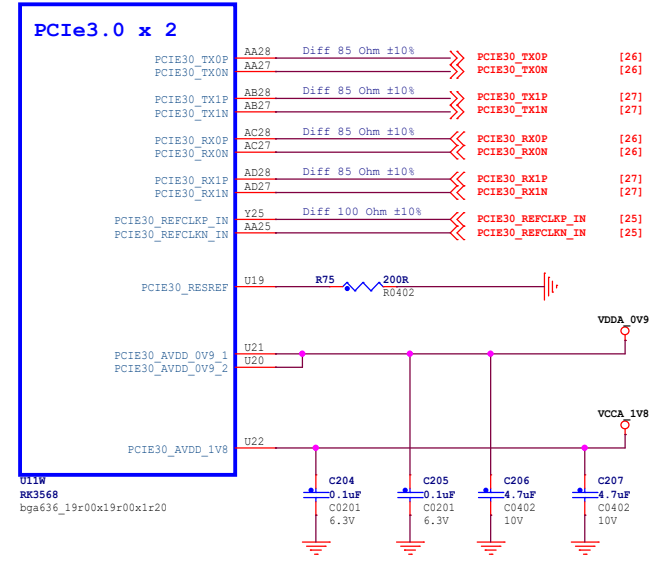
# RK3568 USB3.0/SATA/QSGMII/PCIe2.0 x1



# RK3568 USB2.0 HOST

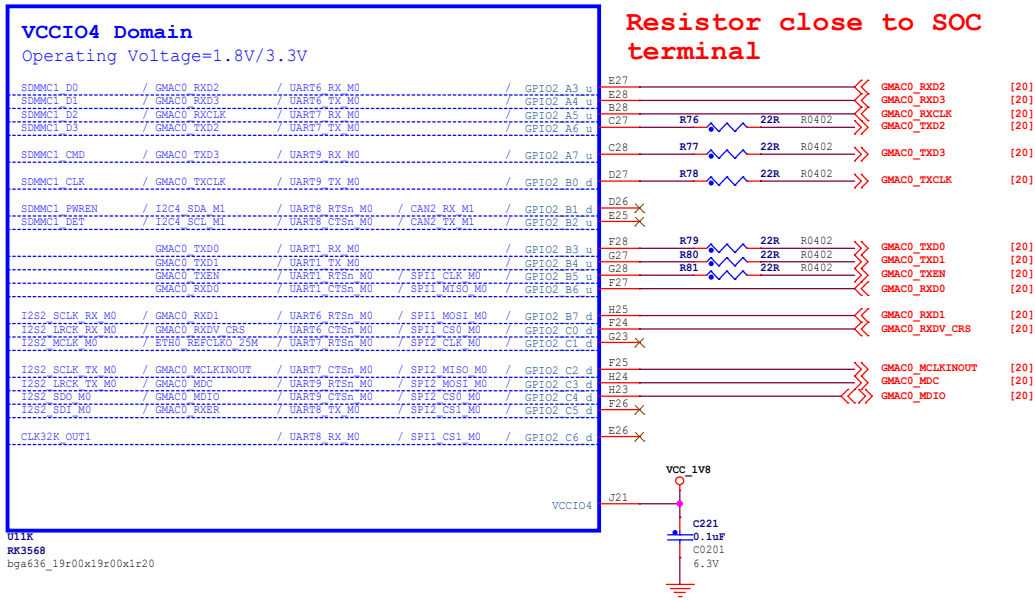


# RK3568 PCIe3.0 x2



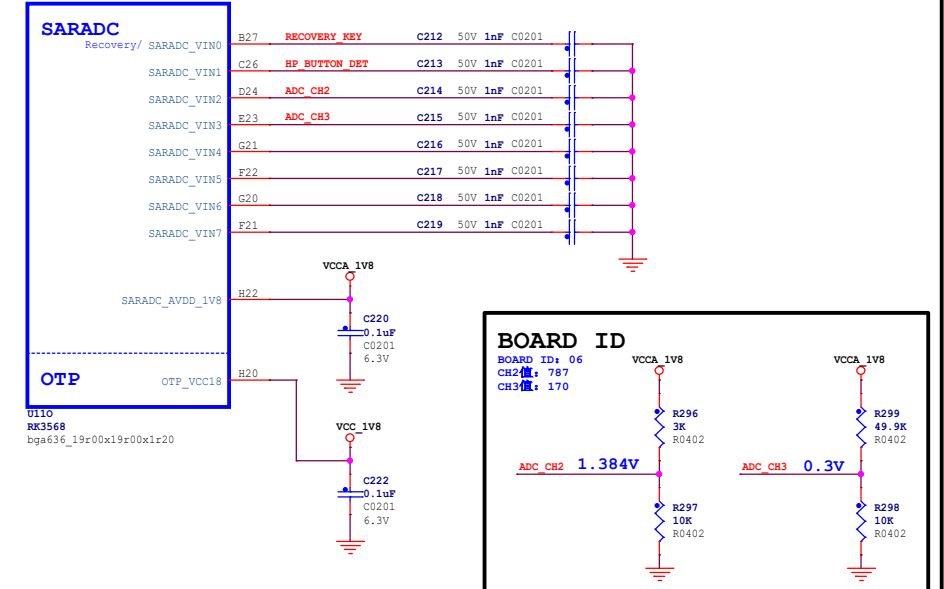
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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number USB/PCIe/STAT PHY	Rev V1.2
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# RK3568 VCCIO4 Domain



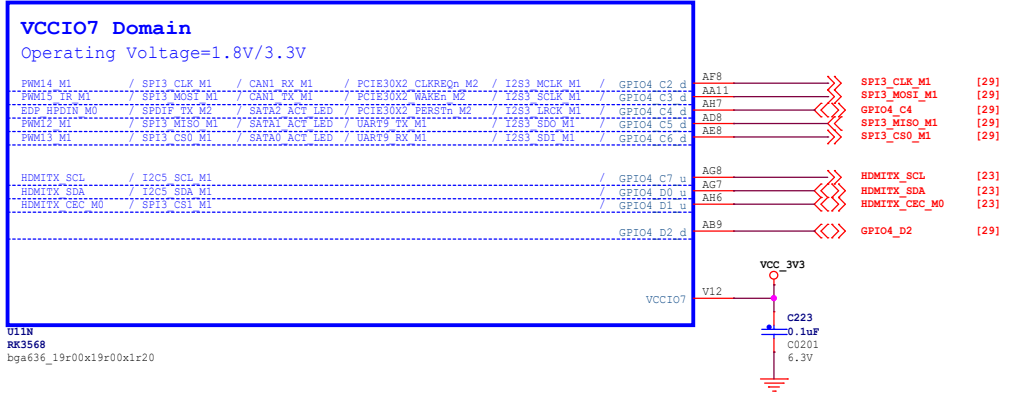
U11K  
RK3568  
bga636\_19r00x19r00x1r20

# RK3568 SARADC/OTP

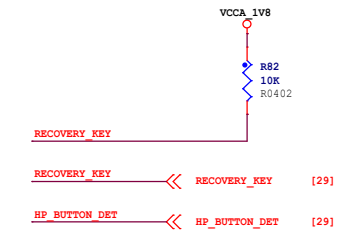


U11o  
RK3568  
bga636\_19r00x19r00x1r20

# RK3568 VCCIO7 Domain



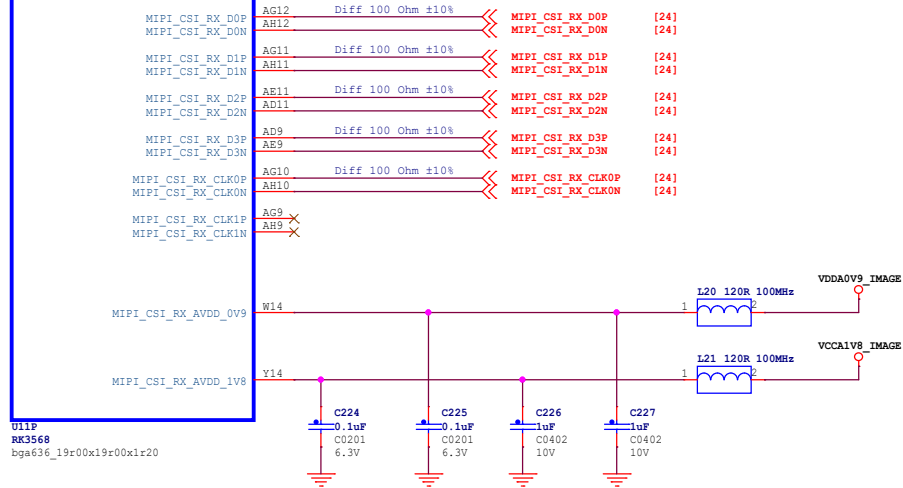
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RK3568  
bga636\_19r00x19r00x1r20



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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number SARADC/GPIO	Rev V1.2
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# RK3568 MIPI\_CSI\_RX

## MIPI CSI RX

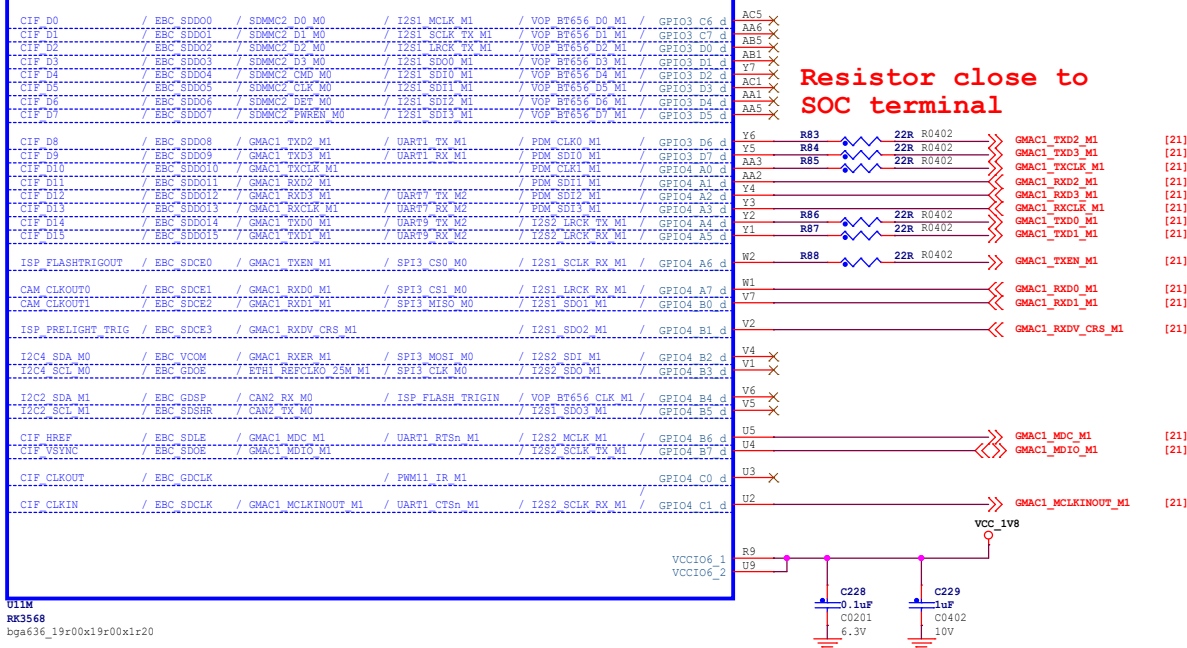


Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

# RK3568 VCCIO6 Domain

## VCCIO6 Domain

Operating Voltage=1.8V/3.3V

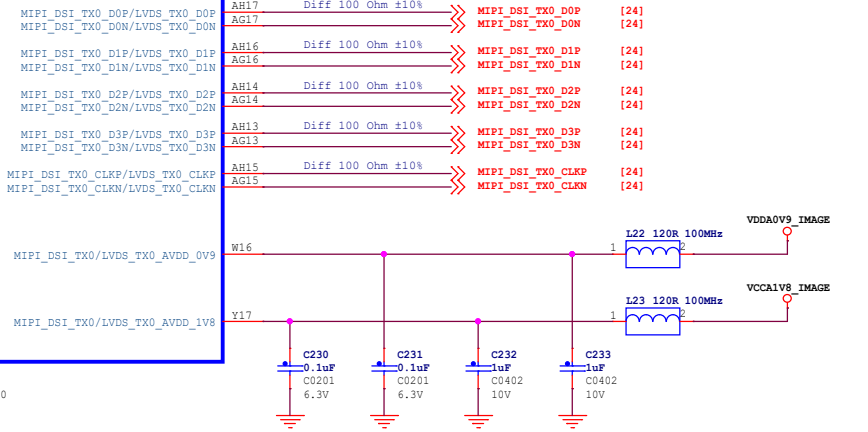


Resistor close to SOC terminal

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# RK3568 MIPI\_DSI\_TX0/LVDS\_TX0

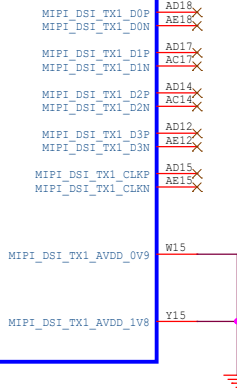
## MIPI DSI TX0/LVDS TX0



U11R  
RK3568  
bga636\_19r00x19r00x1r20

# RK3568 MIPI\_DSI\_TX1

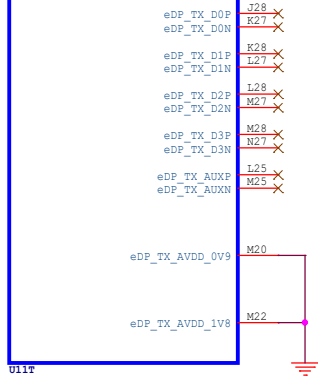
## MIPI DSI TX1



U11S  
RK3568  
bga636\_19r00x19r00x1r20

# RK3568 eDP TX

## eDP\_TX

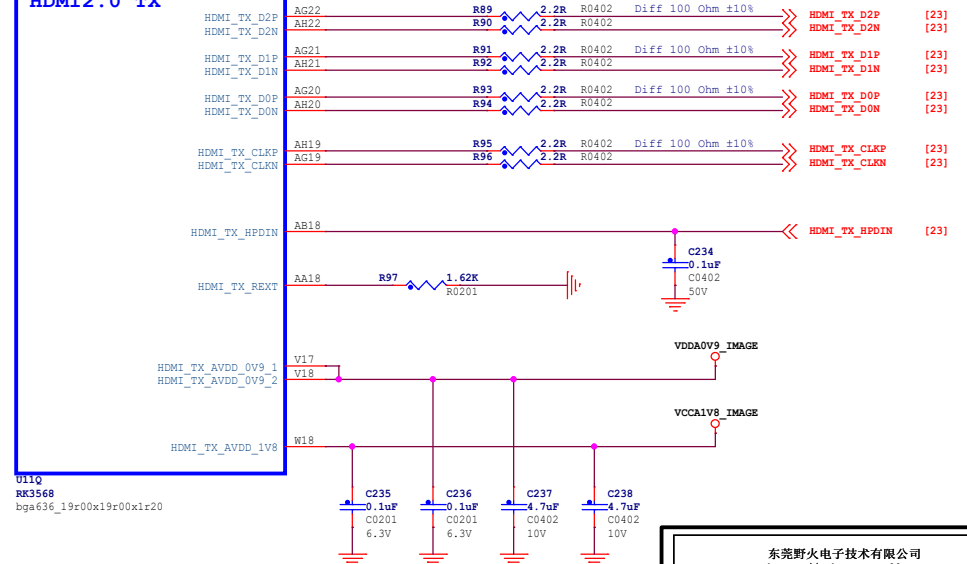


U11Q  
RK3568  
bga636\_19r00x19r00x1r20

# RK3568 HDMI2.0 TX

Resistor close to SOC terminal

## HDMI2.0 TX



U11Q  
RK3568  
bga636\_19r00x19r00x1r20

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Title		
野火_RK3568 LubanCat 2 N_原理图_V1.2		
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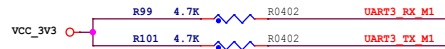
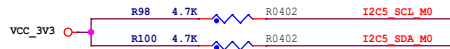
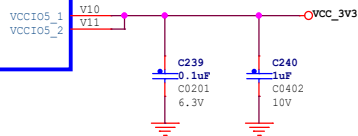


# RK3568 VCCIO5 Domain

## VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQ0n M1	/ I2S1 MCLK M2	/ GPIO2 D0 H	AG6				
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEN M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 H	AD7		PCIE20_WAKEn_M1		[28]
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE20X1 CLKREQ0n M1	/ I2S1 LRCLK TX M2	/ GPIO2 D2 H	AC8		GMAC0_INT	GPIO2_D2	[20]
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE20X1 WAKEN M1	/ I2S1 SCLK M2	/ GPIO2 D3 H	AC7		GMAC0_RSTn	GPIO2_D3	[20]
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 SSI M1	/ PCIE20X2 CLKREQ0n M1	/ I2S1 SDI1 M2	/ GPIO2 D4 H	AF5		2G5_PHY1_RST	GPIO2_D4	[26]
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE20X2 WAKEN M1	/ I2S1 SDI2 M2	/ GPIO2 D5 H	AP6		2G5_PHY2_RST	GPIO2_D5	[27]
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE20X2 PERSTn M1	/ I2S1 SDI3 M2	/ GPIO2 D6 H	AD6		GPIO2_D6		[29]
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART9 TX M1	/ I2S1 SDO0 M2	/ GPIO2 D7 H	AH5		GPIO2_D7		[29]
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART9 RX M1	/ I2S1 SDO1 M2	/ GPIO3 A0 H	AH4		GPIO3_A0		[29]
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 H	AB8		GMAC1_INT	GPIO3_A1	[21]
LCDC D9	/ VOP BT1120 D1	/ GMAC1 TXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 H	AE5		GMAC1_RSTn	GPIO3_A2	[21]
LCDC D10	/ VOP BT1120 D2	/ GMAC1 TXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 H	AG4		LCD_PWR_EN	GPIO3_A3	[24]
LCDC D11	/ VOP BT1120 D3	/ GMAC1 TXD0 M0	/ I2S3 LRCLK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 H	AF4		CM1_PWR_EN	GPIO3_A4	[24]
LCDC D12	/ VOP BT1120 D4	/ GMAC1 TXD1 M0	/ I2S3 SSI M0	/ SDMMC2 CLK M1	/ GPIO3 A5 H	AH3		GPIO3_A5		[29]
LCDC D13	/ VOP BT1120 D5	/ GMAC1 RXCLK M0	/ I2S3 SSI M0	/ SDMMC2 CLK M1	/ GPIO3 A6 H	AG3		GPIO3_A6		[29]
LCDC D14	/ VOP BT1120 D6	/ GMAC1 RXCLK M0	/ I2S3 SSI M0	/ SDMMC2 DEN M1	/ GPIO3 A7 H	AH2		GPIO3_A7		[29]
LCDC D15	/ VOP BT1120 D6	/ ETH1 BEPC10_25M M0		/ SDMMC2 PWREN M1	/ GPIO3 B0 H	AG2		GPIO3_B0		[29]
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 H	AG1		PWM8_M0		[29]
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 H	AF2		PWM9_M0		[29]
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXD0_CRS M0	/ I2C3 SCL M0	/ PWM SD10 M2	/ GPIO3 B3 H	AF1		I2C5_SCL_M0		[29]
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXD1_CRS M0	/ I2C3 SDA M0	/ PWM SD11 M2	/ GPIO3 B4 H	AE1		I2C5_SDA_M0		[29]
LCDC D20	/ VOP BT1120 D11	/ GMAC1 TXD0 M0	/ I2C3 SCL M1	/ PWM10 M0	/ GPIO3 B5 H	AE2		PWM10_M0		[29]
LCDC D21	/ VOP BT1120 D12	/ GMAC1 TXD1 M0	/ I2C3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 H	AD4		GPIO3_B6		[29]
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SD12 M2	/ GPIO3 B7 H	AD2		UART3_TX_M1		[29]
LCDC D23	/ PWM13 M0	/ GMAC1 MCLINKOUT M0	/ UART3 RX M1	/ PDM SD13 M2	/ GPIO3 C0 H	AD2		UART3_RX_M1		[29]
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SDO2 M2	/ GPIO3 C1 H	AD1		PCIE20_PERSTn_M1		[28]
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SDO3 M2	/ GPIO3 C2 H	AA7		MINIPICIE_PWDISABLE	GPIO3_C2	[28]
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 H	AC4		MINIPICIE_PWR_EN	GPIO3_C3	[28]
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 H	AC3		PWM14_M0		[29]
PWM13 TX M0	/ SP017 TX M1	/ GMAC1 MDC M0	/ UART7 RX M1	/ I2S1 LRCLK RX M2	/ GPIO3 C5 H	AC2		GPIO3_C5		[29]



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Title 野火\_RK3568 LubanCat 2 N\_原理图\_V1.2

Size A3 Document Number VO Interface\_2 Rev V1.2

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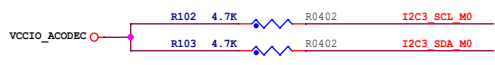
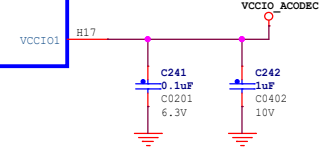
# RK3568 VCCIO1 Domain

**VCCIO1 Domain**  
Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOOP_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_H
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOOP_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_H
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERStn_M2		/ GPIO1_A2_H
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_H
I2S1_SCLK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ SPDIF_TX_M0		/ GPIO1_A4_H
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_H
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROOT_P		/ GPIO1_A6_H
I2S1_SD00_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROOT_N	/ ACODEC_DAC_DATA1	/ GPIO1_A7_H
I2S1_SD01_M0	/ I2S1_SDIF_M0	/ PDM_SDI0_M0	/ PCIE20_CLAMPn_M2	/ ACODEC_DAC_DATA2	/ GPIO1_B0_H
I2S1_SD02_M0	/ I2S1_SDIF_M0	/ PDM_SDI1_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_H
I2S1_SD03_M0	/ I2S1_SDIF_M0	/ PDM_SDI2_M0	/ PCIE20_BERRStn_M2		/ GPIO1_B2_H
I2S1_SD04_M0	/ I2S1_SDIF_M0	/ PDM_SDI3_M0			/ GPIO1_B3_H

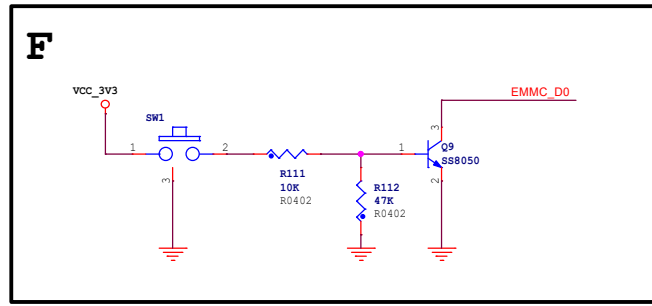
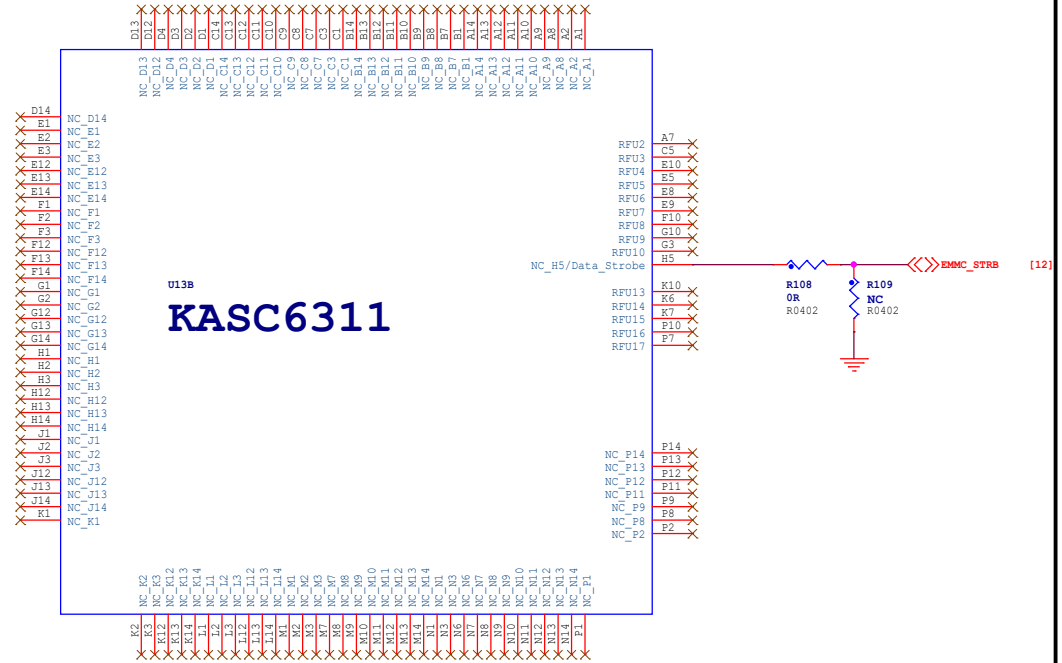
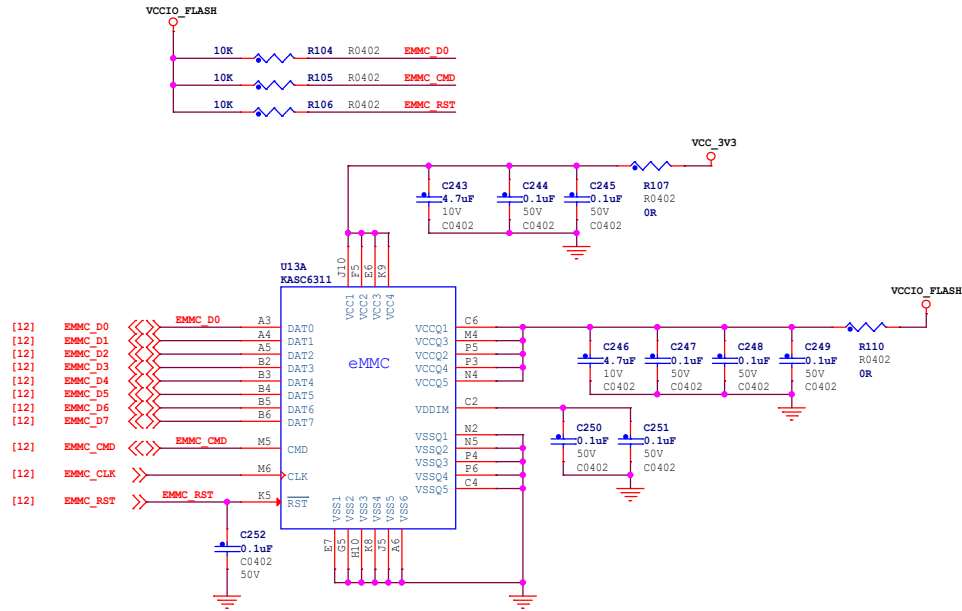


011H  
RK3568  
bga636\_19r00x19r00x1r20

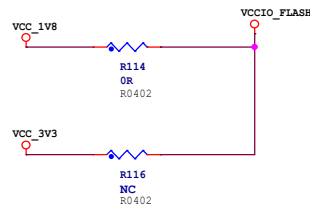


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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number Audio Interface	Rev V1.2
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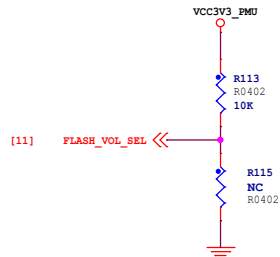
# EMMC FLASH



## EMMC\_IO\_Toggle



## FLASH\_VOL\_SEL



Note:  
FLASH\_VOL\_SEL state decided  
to VCCIO2 domain IO driven by default  
Logic=L: 3.3V IO driven  
Logic=H: 1.8V IO driven

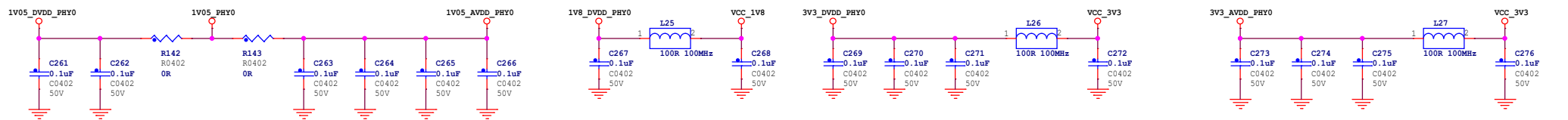
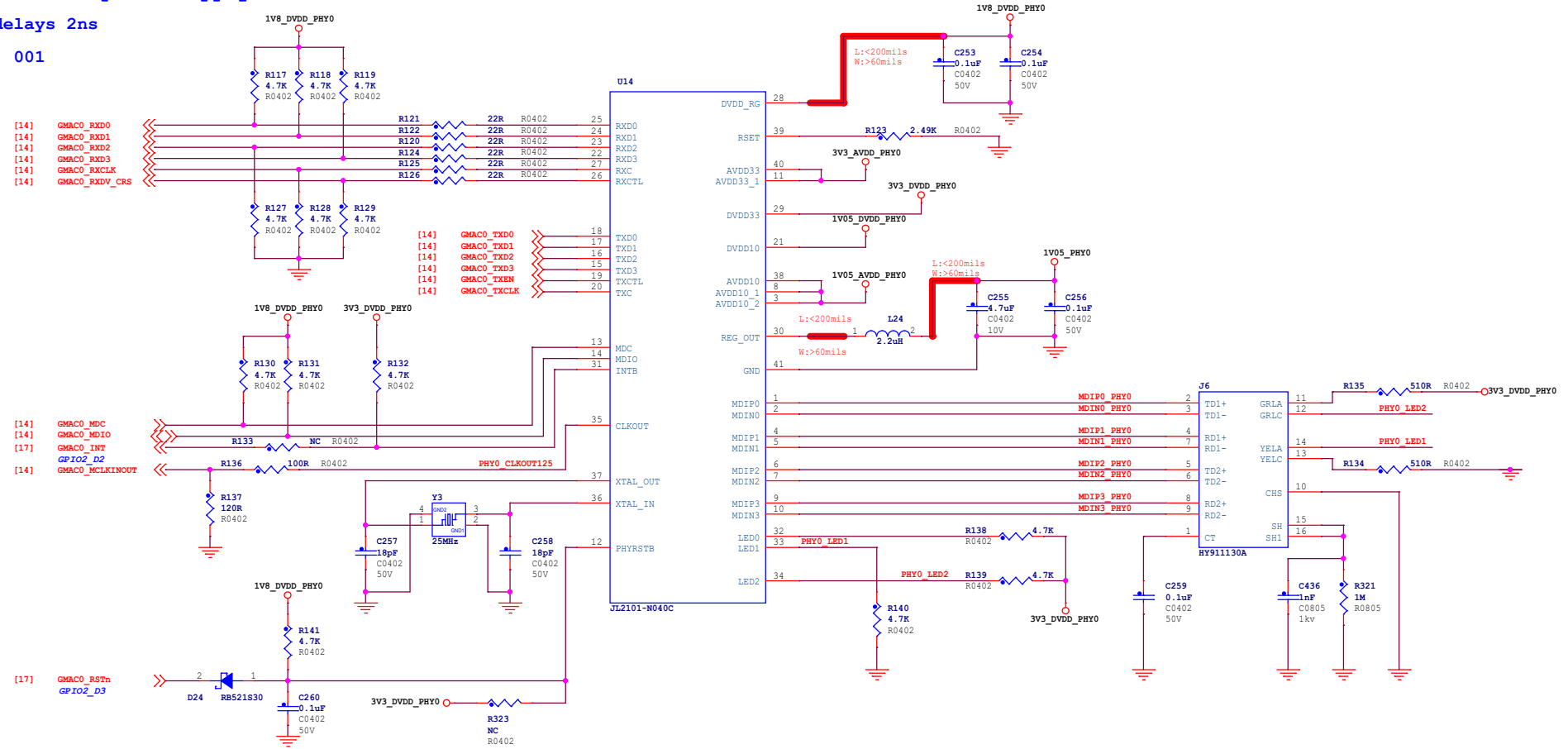
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Title	野火_RK3568 LubanCat 2 N_原理图_V1.2	
Size	Document Number	Rev
A3	EMMC_FLASH	V1.2
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# ETH\_1

IO Use an external power supply: 1.8V

TXC / RXC : delays 2ns

PHY Address : 001



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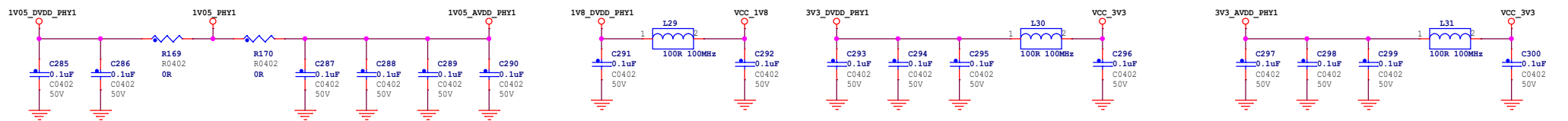
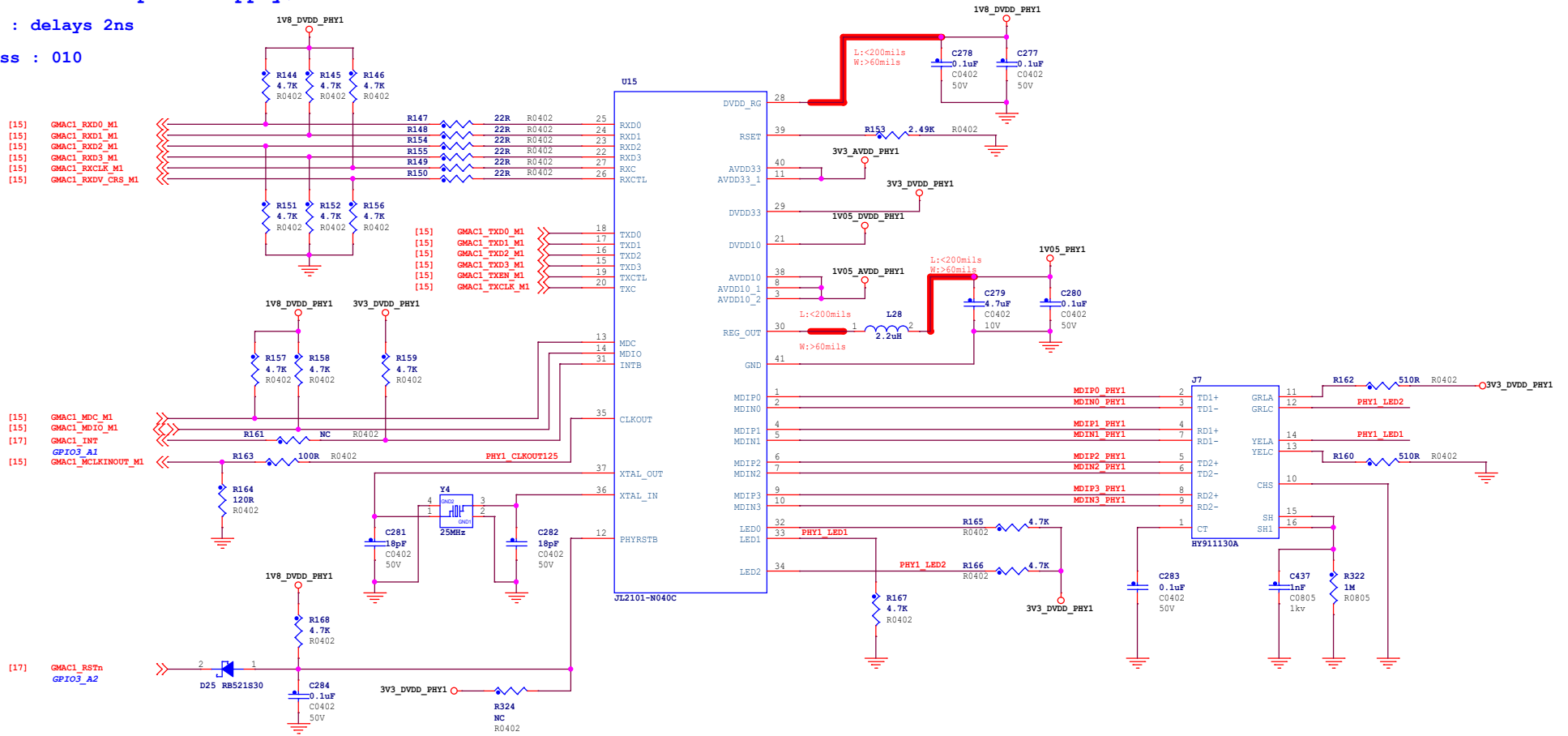
Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number ETH_1	Rev V1.2
Date: Thursday, July 13, 2023 Sheet 20 of 29		

# ETH\_2

IO Use an external power supply: 1.8V

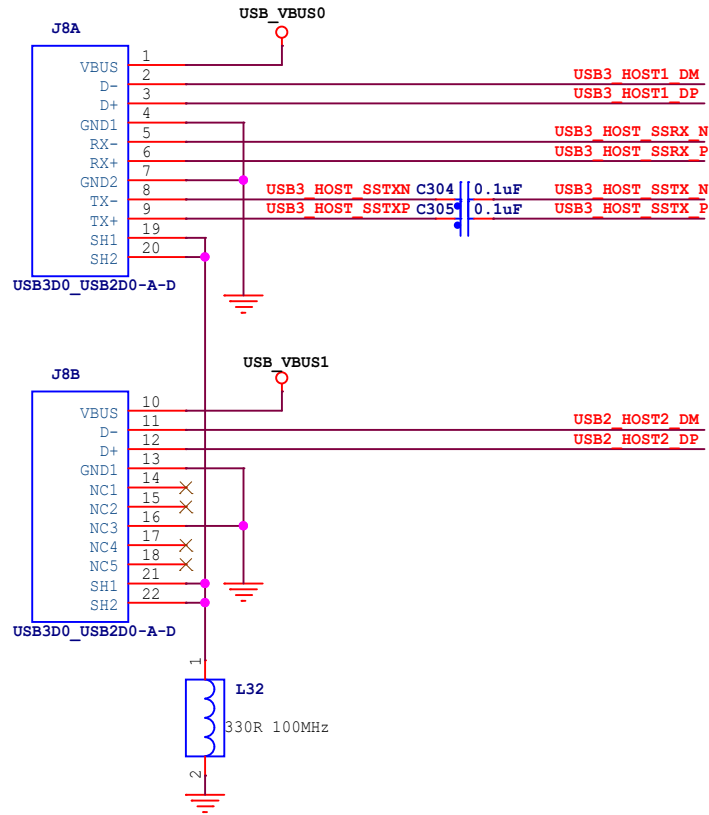
TXC / RXC : delays 2ns

PHY Address : 010

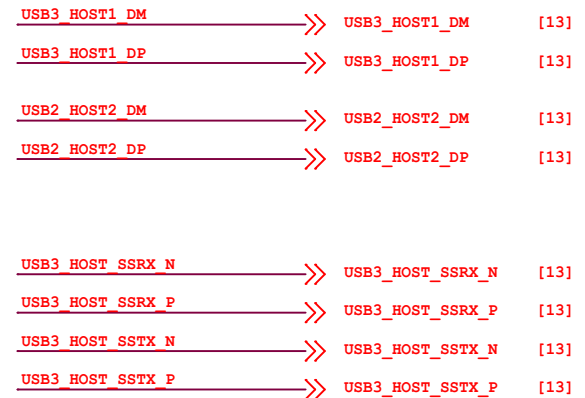
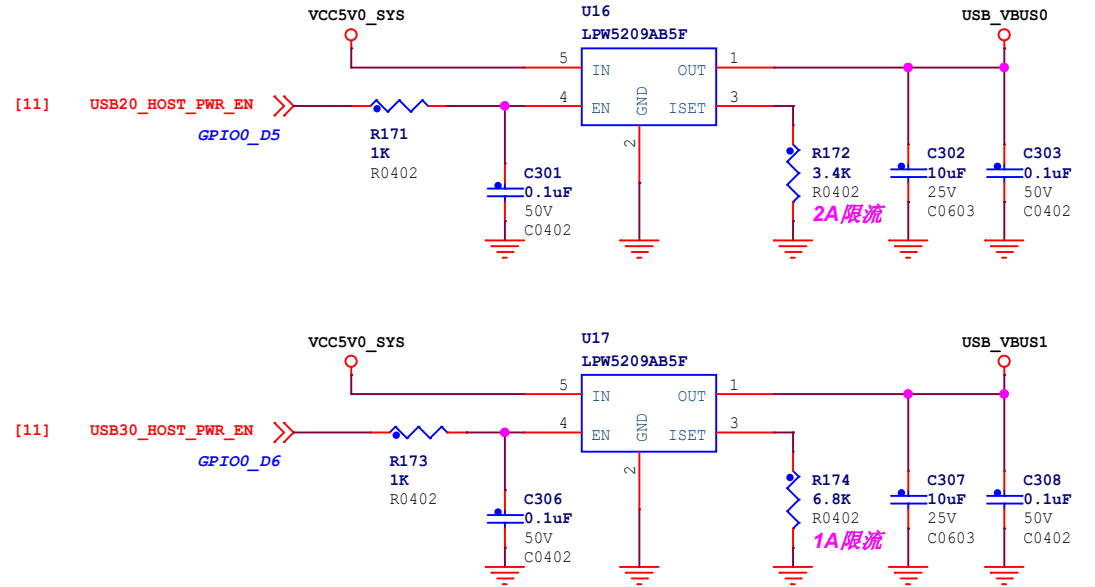


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Title 野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size A3	Document Number ETH_2	Rev V1.2
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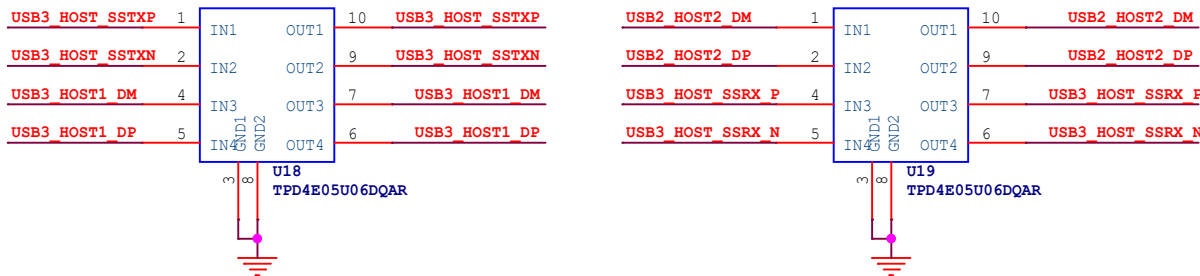
# USB 3.0 HOST x1 USB 2.0 HOST x1



# USB POWER



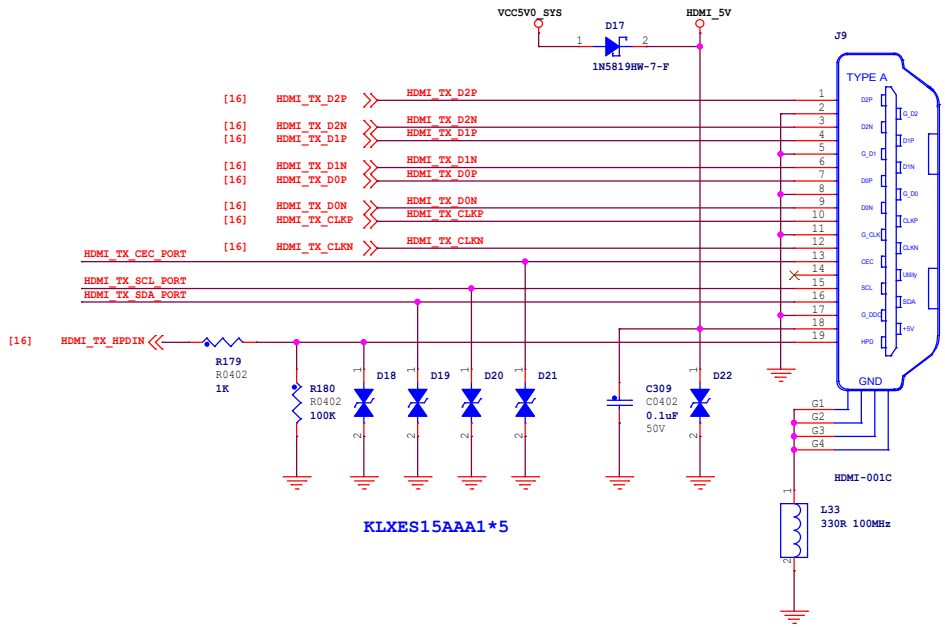
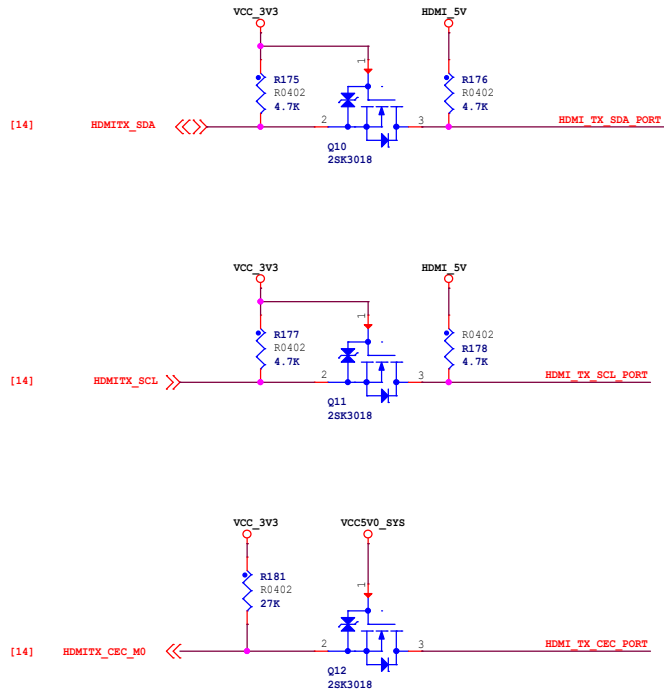
# ESD



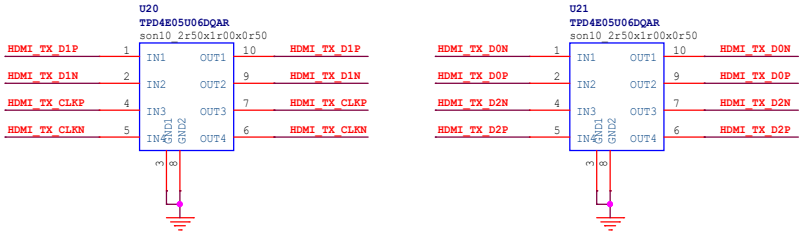
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Title 野火_RK3568 LubanCat 2 N_原理图_v1.2		
Size A4	Document Number USB_PORT	Rev V1.2
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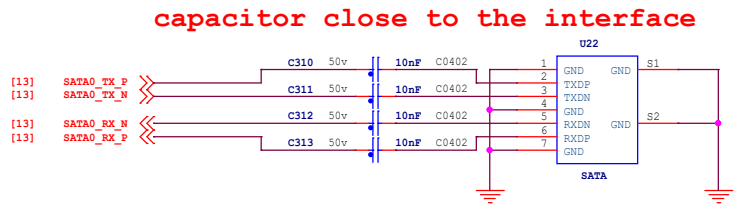
# HDMI\_PORT



# HDMI\_ESD

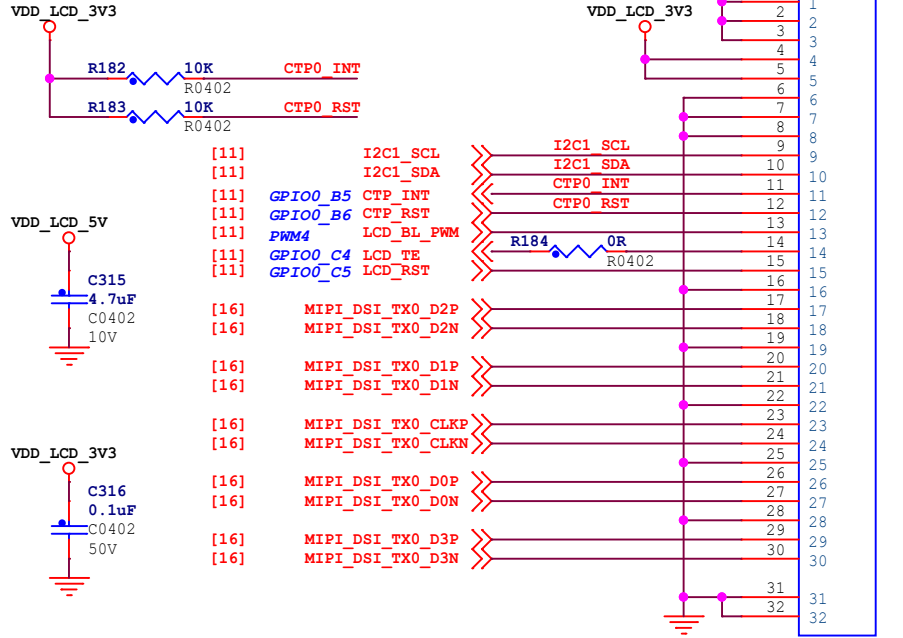


# SATA\_PORT

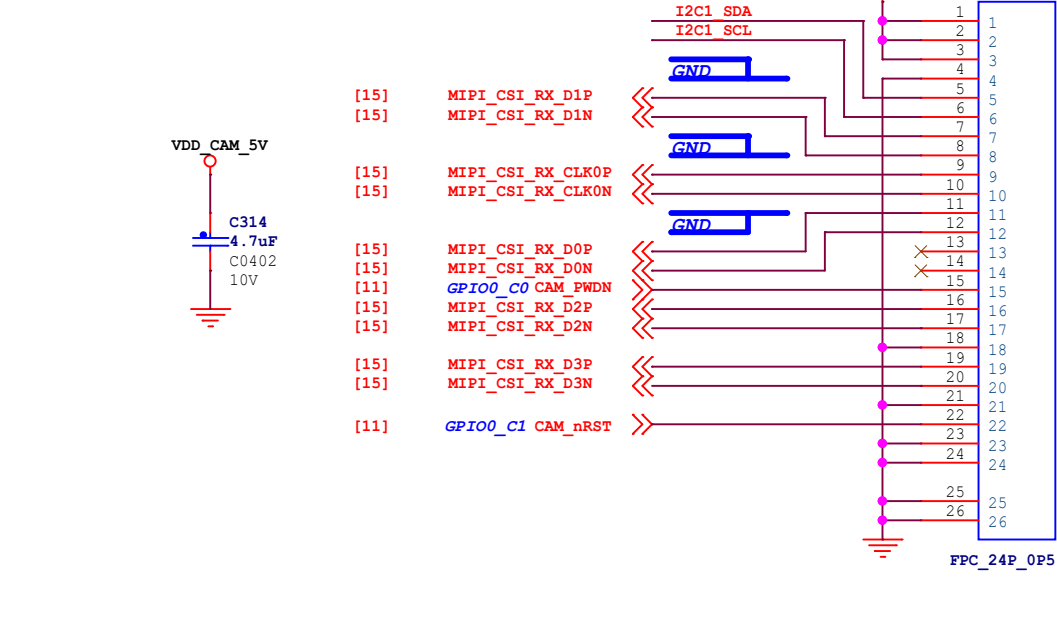


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Title	野火_RK3568 LubanCat 2 N_原理图_V1.2	
Size	Document Number	Rev
A3	HDMI_PORT/SATA_PORT	V1.2
Date:	Thursday, July 13, 2023	Sheet 23 of 29

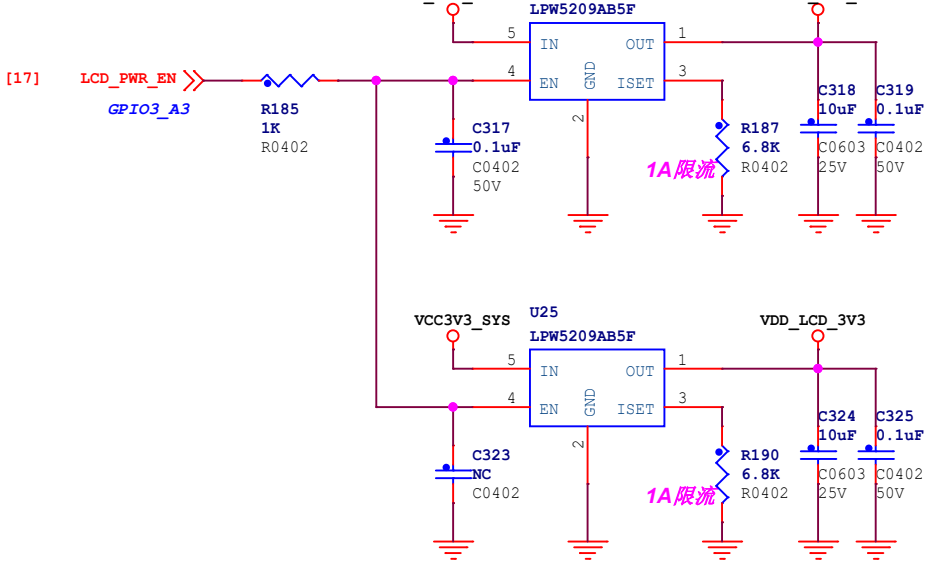
### MIPI DSI LCD PORT



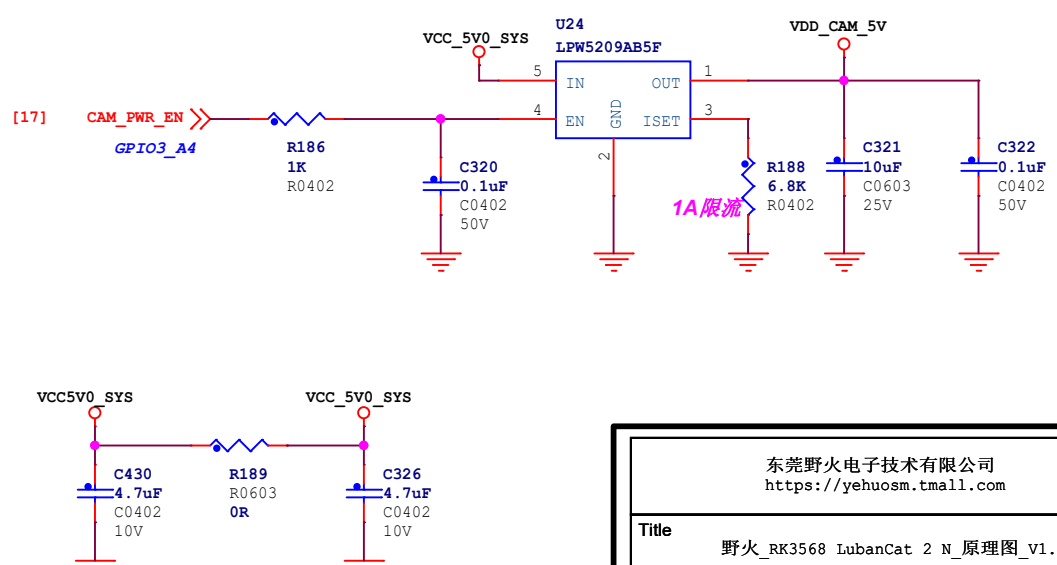
### MIPI CSI PORT



### LCD Power



### MIPI CSI Power



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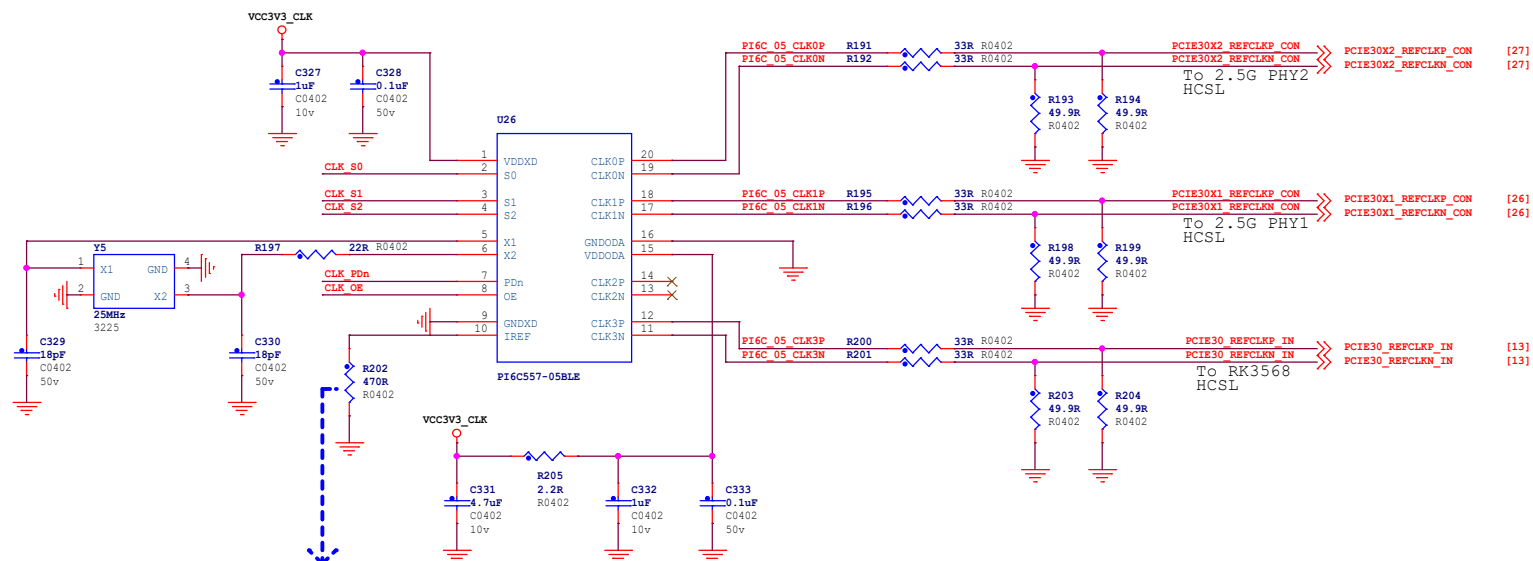
Title: 野火\_RK3568 LubanCat 2 N\_原理图\_V1.2

Size: A4	Document Number: MIPI DSI/MIPI CSI_PORT	Rev: V1.2
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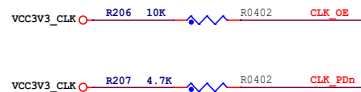


# PCIE3.0\_REFCLK

CLK\*3 @100MHz



If board target trace impedance is 50ohm then  $R = 475\text{ohm}$  providing an IREF of 2.32 mA . The output current ( IOH ) is  $6 * IREF . 6 \times 2.32 \times 50 = 696\text{mA}$

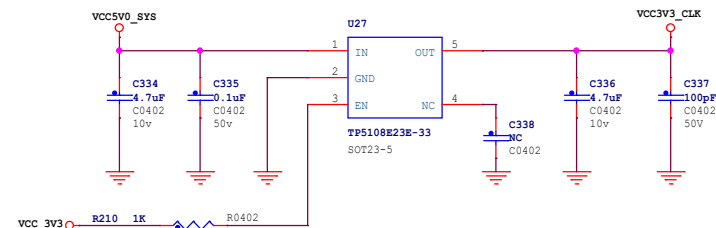


## SPEED\_MODE\_SET

Default: No Spread

CLK_S0	CLK_S1	CLK_S2	Spread %	Out Freq
0	0	0	-0.5	100MHz
1	0	0	-1.0	100MHz
0	1	0	-1.5	100MHz
1	1	0	No Spread	100MHz

## SPLIT\_CLK\_POWER

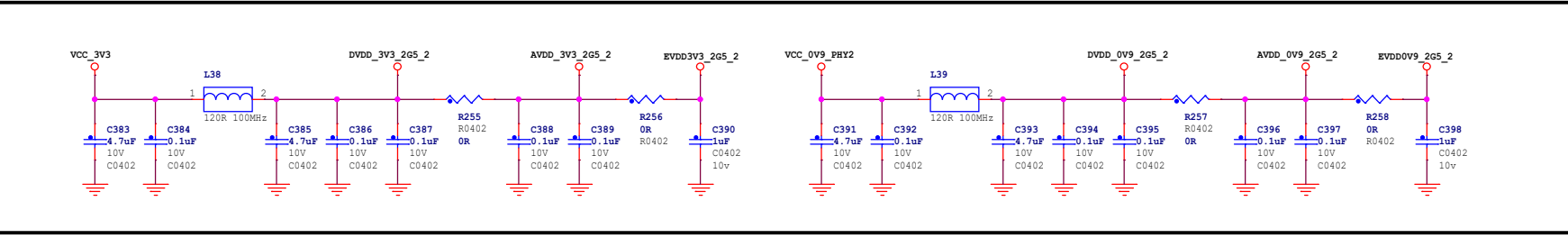
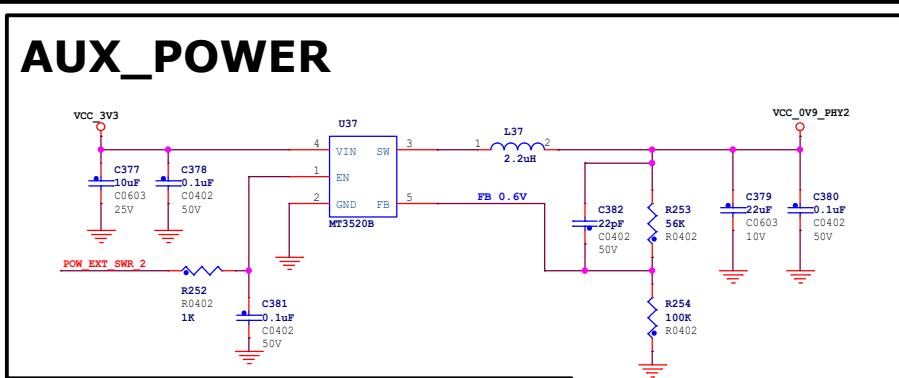
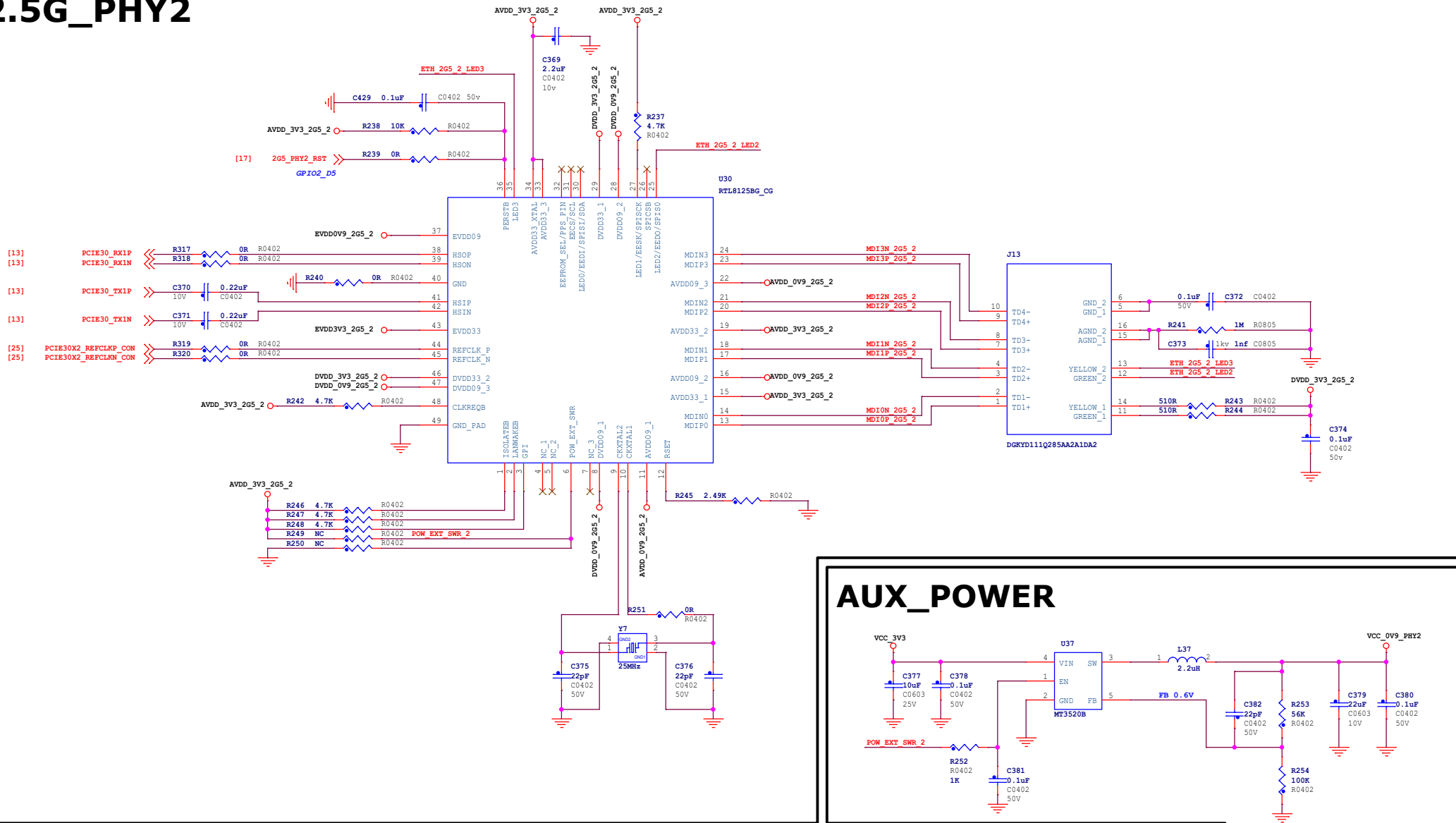


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Size A3	Document Number PCIE3.0_REFCLK	Rev V1.2
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# 2.5G\_PHY2



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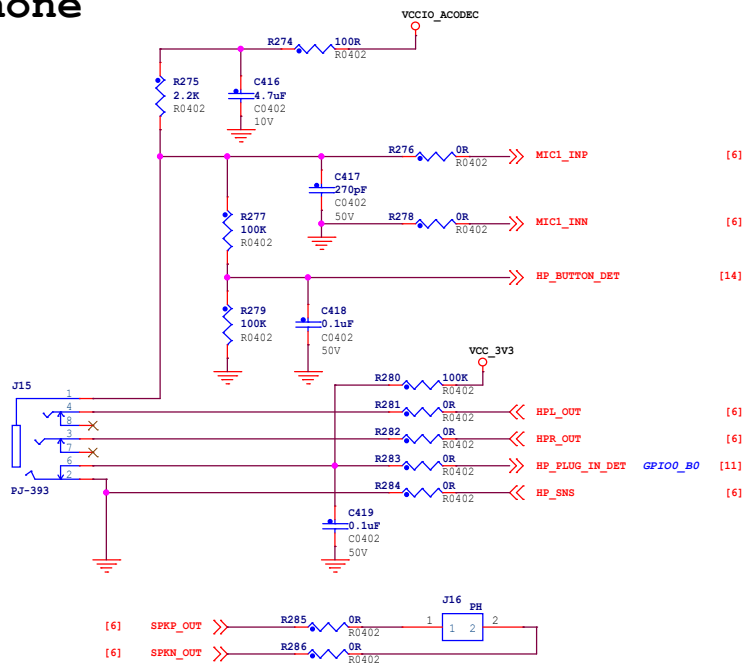
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Size	Document Number	Rev
A3	2.5G_PHY2	V1.2

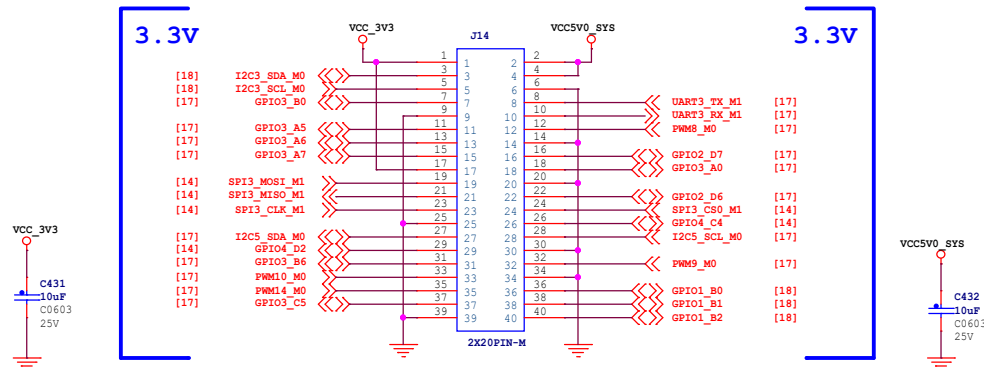
Date: Thursday, July 13, 2023 Sheet 27 of 29



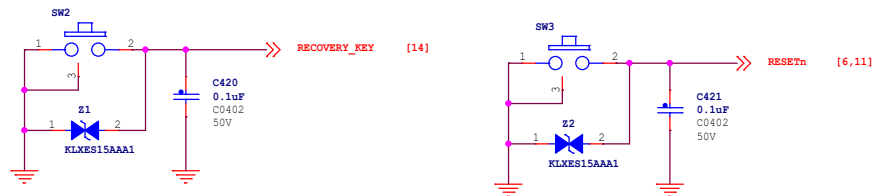
# Earphone



# IO PORT



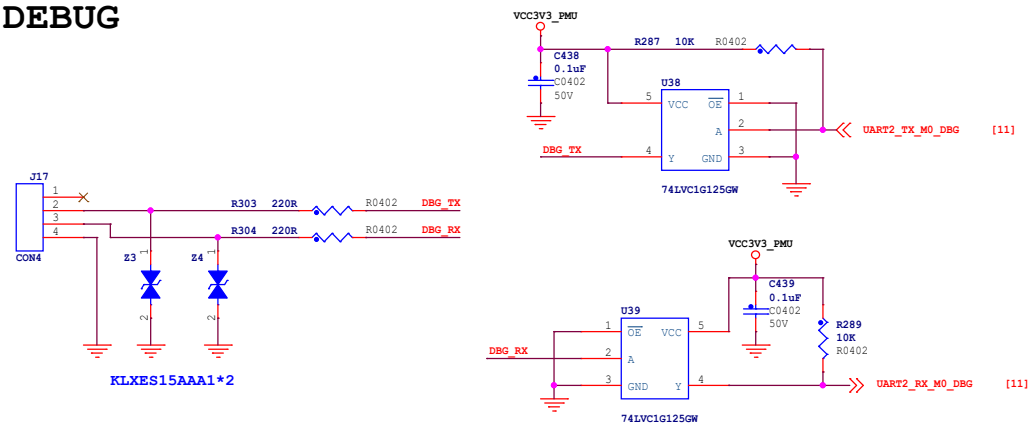
# RECOVERY KEY RESET KEY



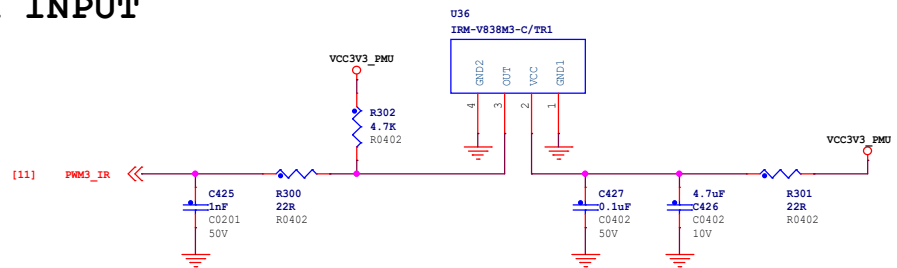
# LED



# DEBUG



# IR INPUT



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Title		
野火_RK3568 LubanCat 2 N_原理图_V1.2		
Size	Document Number	Rev
A3	Earphone/DEBUG/IO_PORT/LED	V1.2
Date:	Thursday, July 13, 2023	Sheet 29 of 29