

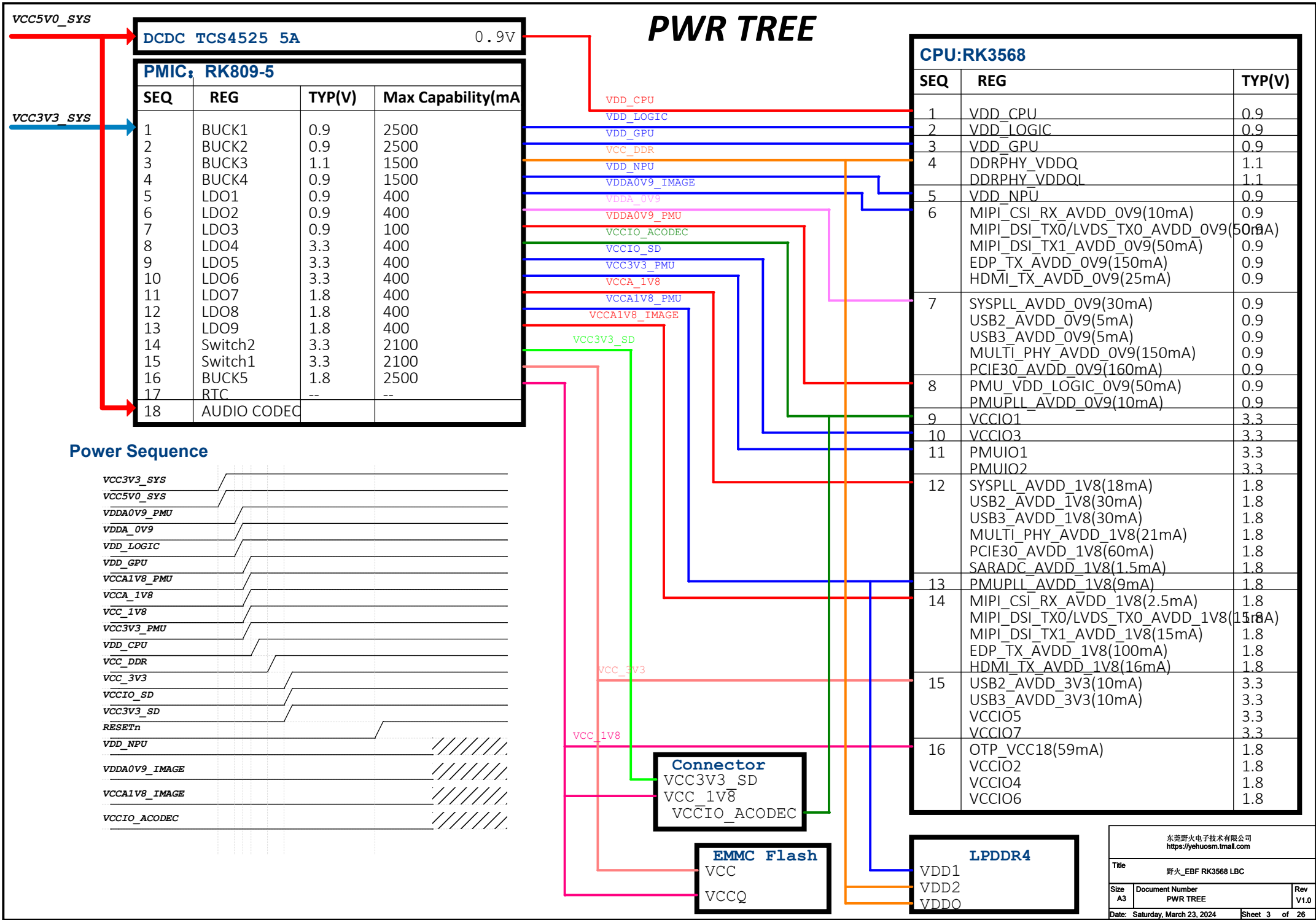
野火 EBF RK3568 LBC

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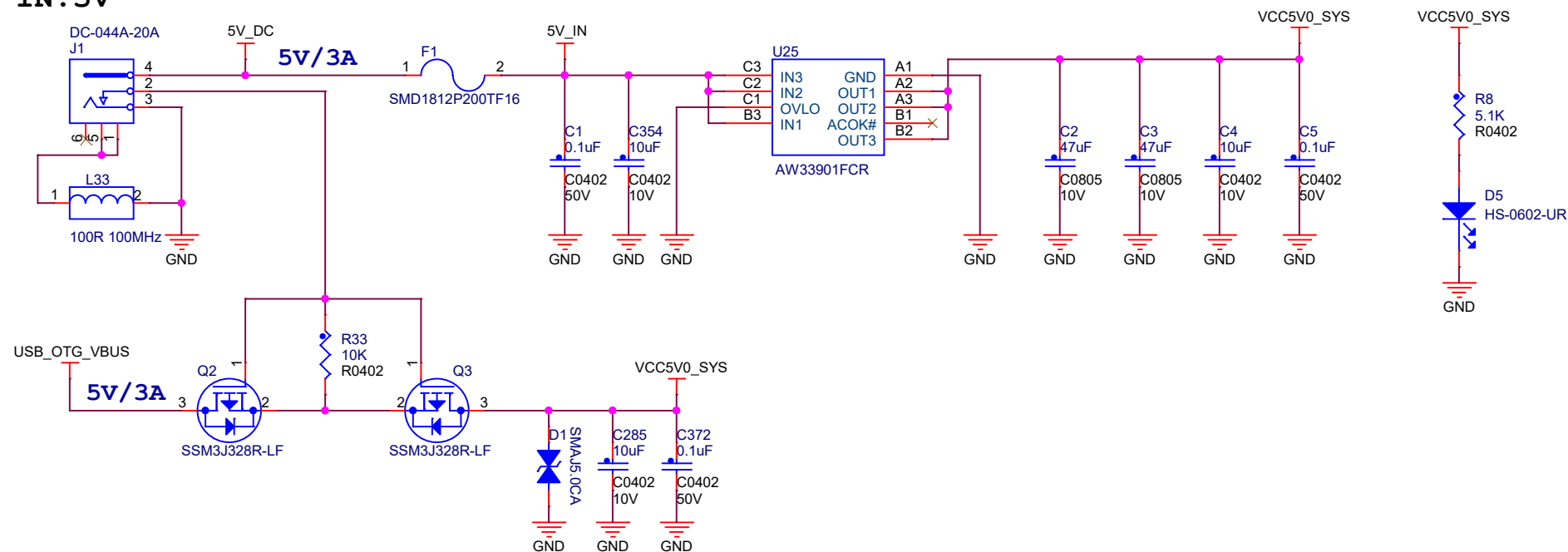
历史版本

版本号	日期	设计	描述
V1.0	2022-01-25	llm	初始版本, 开发阶段
V1.1	2022-05-18	llm	修复初始版本的一些问题，增加SATA接口， typec添加OTG自动识别host/device功能
V1.2	2022-07-27	llm	1.MIPI CSI 添加2 Lanes 2.更新MINI PCIE、M.2 PCIE封装，添加独立的定位孔 3.把Z4、Z3、Z2、Z1位号改前缀为D的位号 4.把sim卡座位号U18改为J18 5.把mini pcie位号CON1改为J17
V1.2	2022-11-29	llm	添加LPDDR4x注释，电路不做任何更改
V1.3	2022-12-08	llm	1.网口外壳增加阻容到地隔离 2.IR接收更换为PWM3_IR, IR接收器电源更改为VCC3V3_PMU, 以支持休眠唤醒
V1.4	2024-3-22	llm	1.mini pcie电源添加220uF钽电容，兼容5G模块供电 2.添加外挂RTC BM8563EMA 3.改为支持40pin排针5V供电 4.USER_LED由GPIO0_C7改为GPIO1_A4 5.更新board id

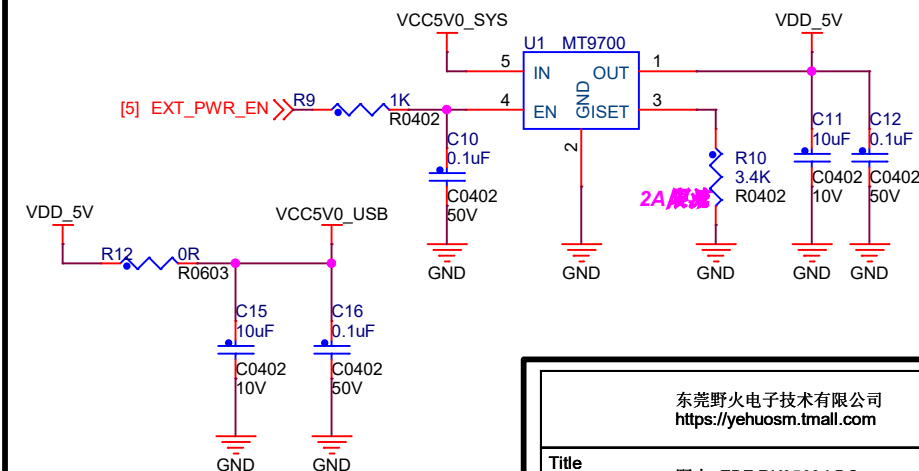
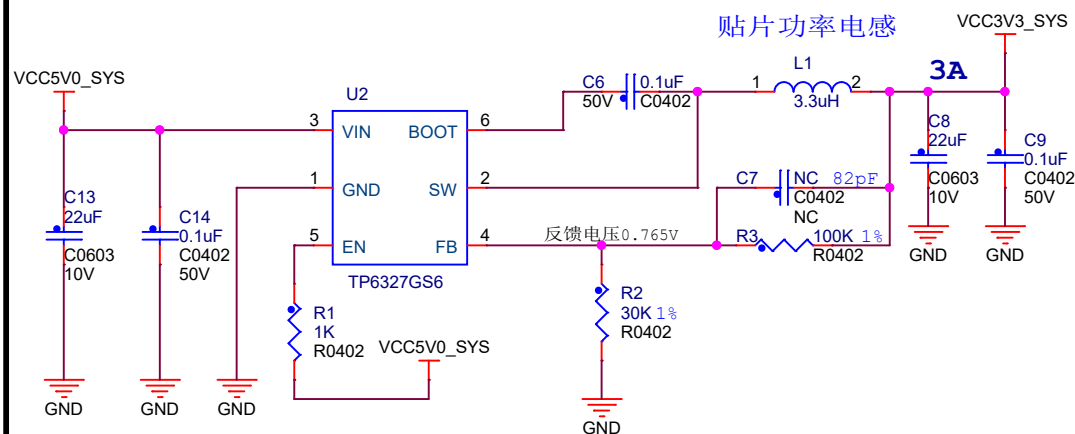
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Title 野火_EBF RK3568 LBC		
Size A4	Document Number 历史版本	Rev V1.0
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DC IN: 5V



5V转3.3V



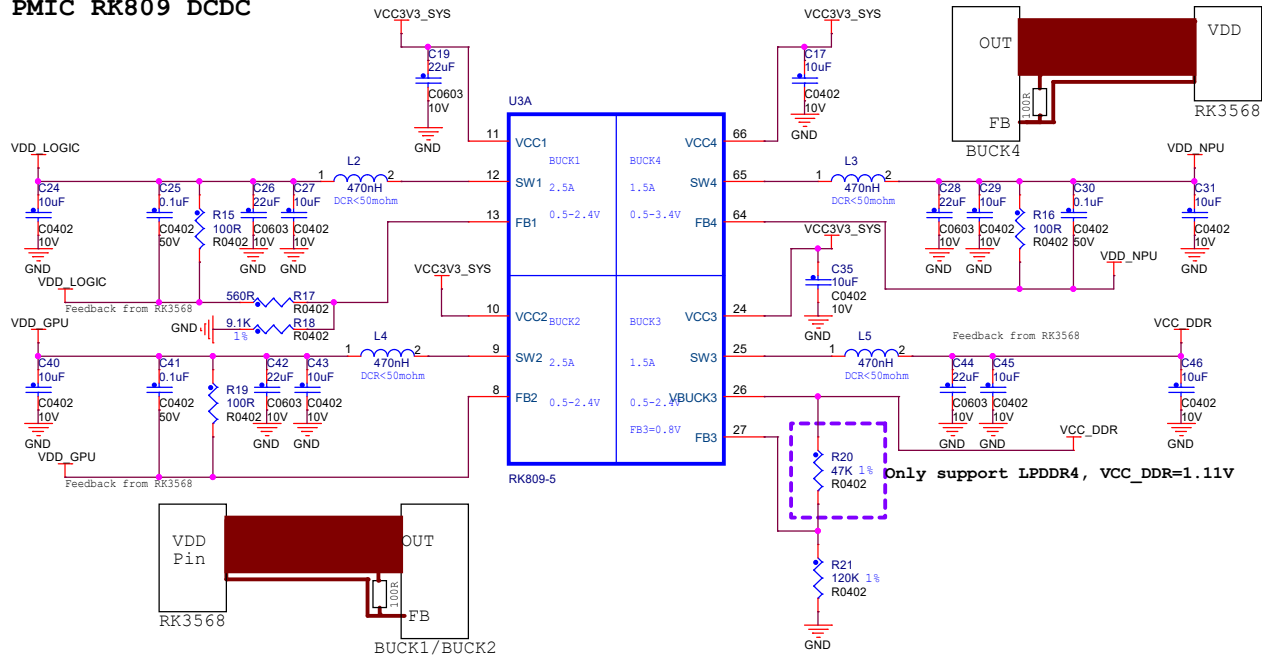
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Title	野火_EBF RK3568 LBC
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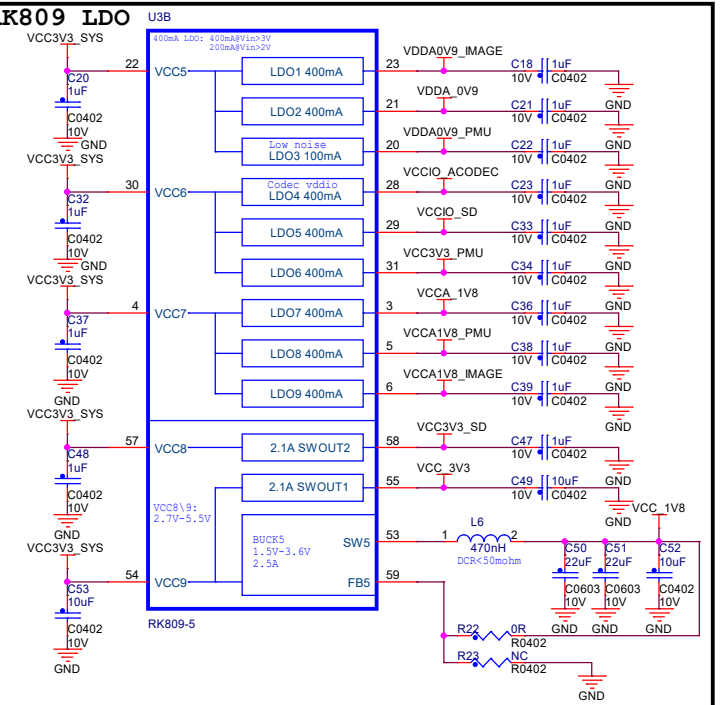
Size A4	Document Number 电源	Rev V1.0
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Date: Saturday, March 23, 2024 Sheet 4 of 26

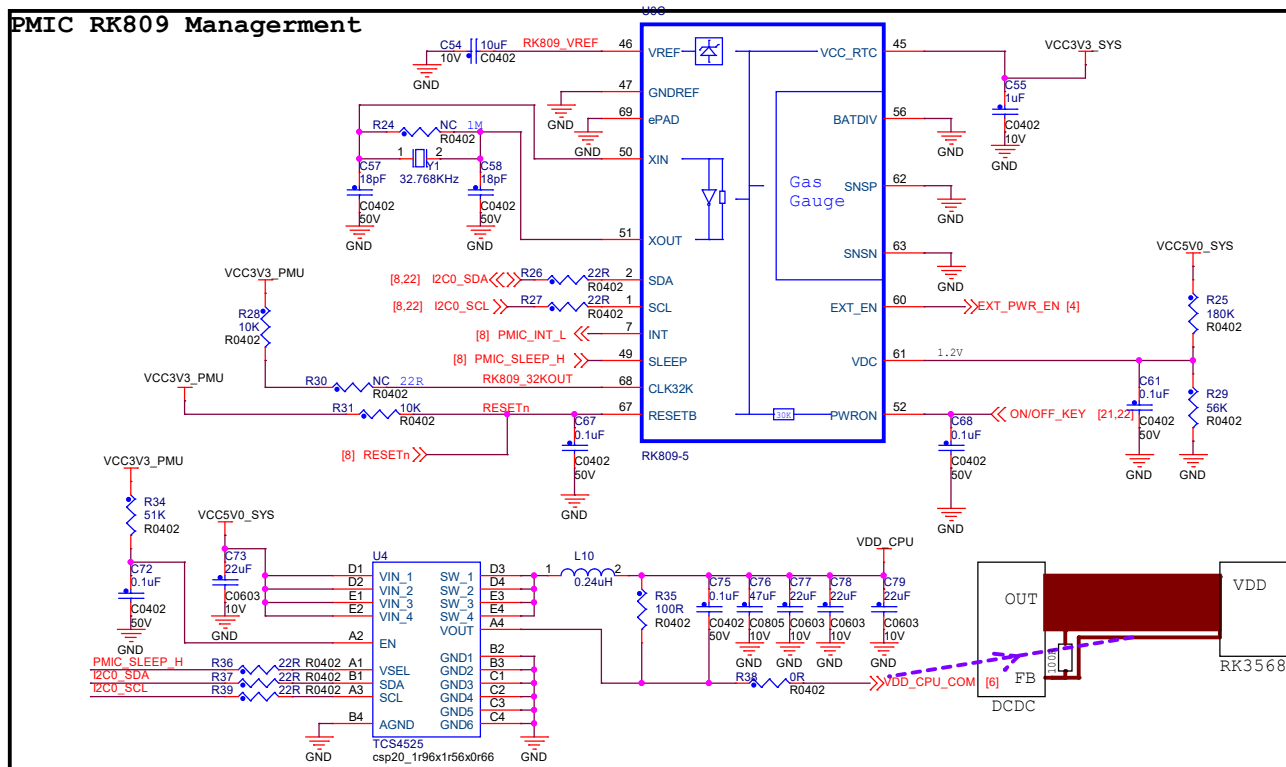
PMIC RK809 DCDC



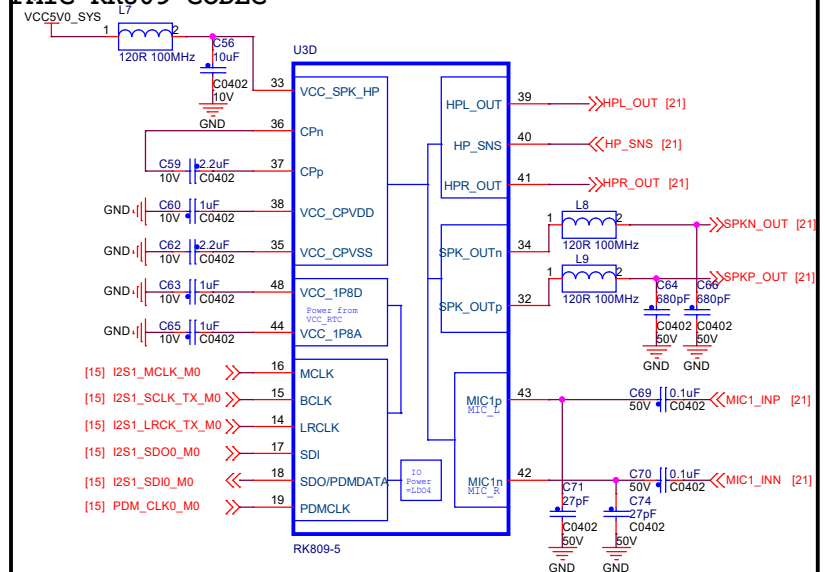
PMIC RK809 LDO



PMIC RK809 Management



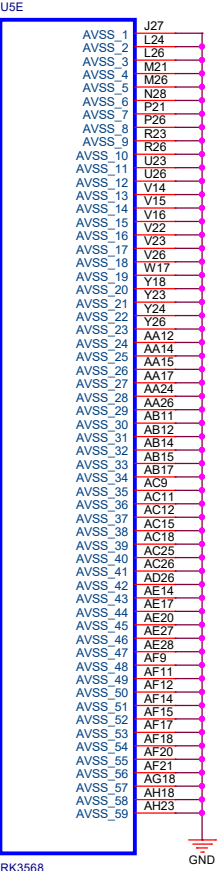
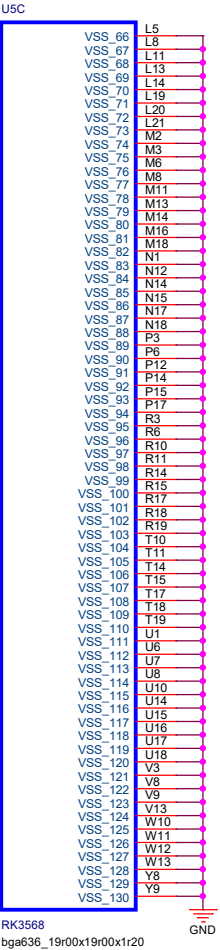
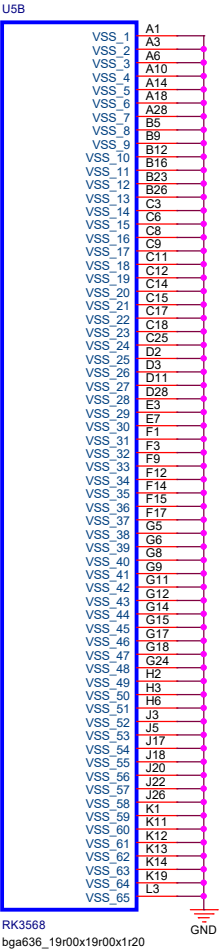
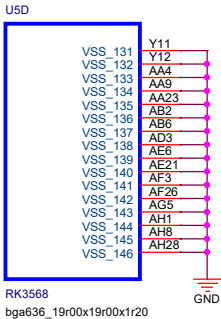
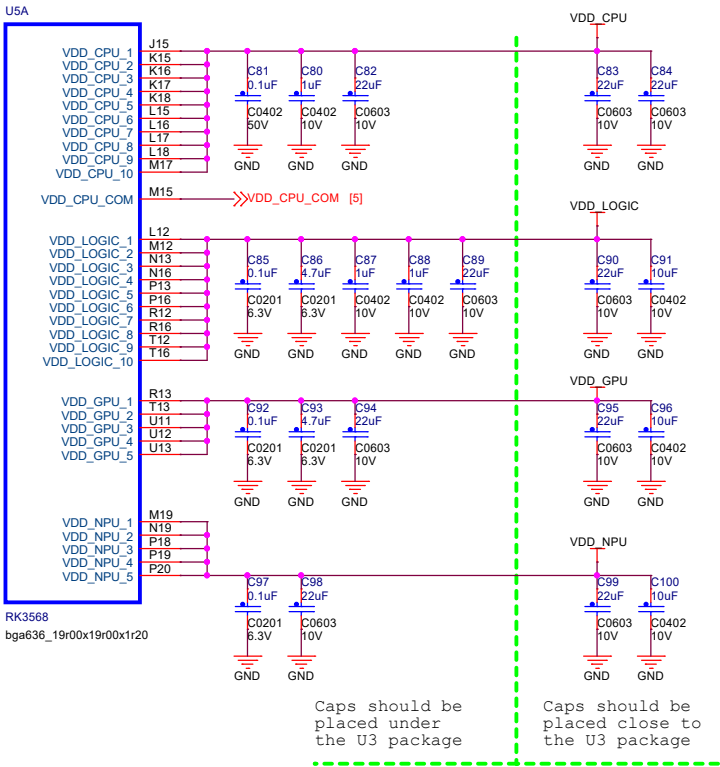
PMIC RK809 CODEC



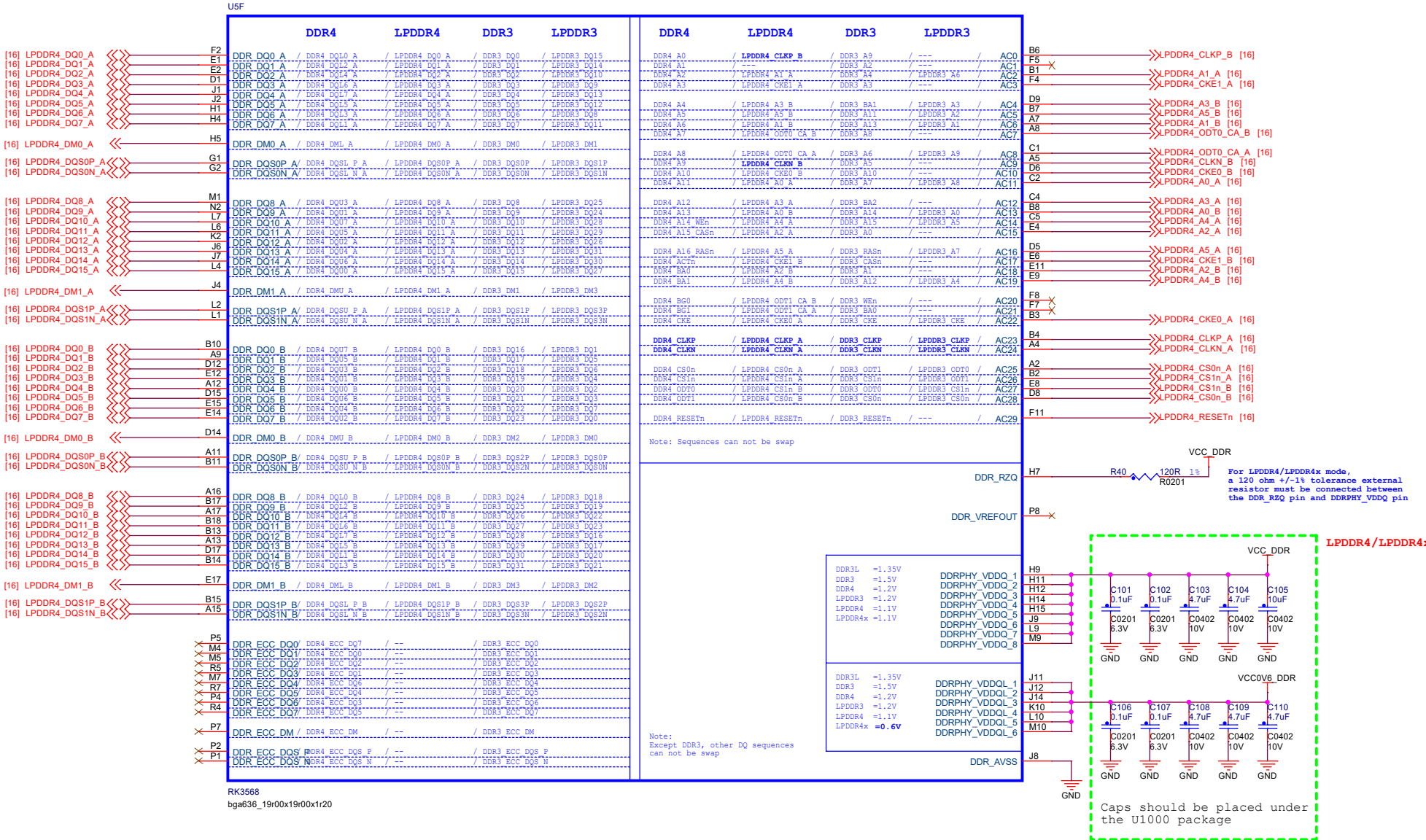
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Title			野火_EBF RK3568 LBC
Size	Document Number	Rev	
A3	SYS PMIC	V1.0	
Date: Saturday, March 23, 2024		Sheet	5 of 26

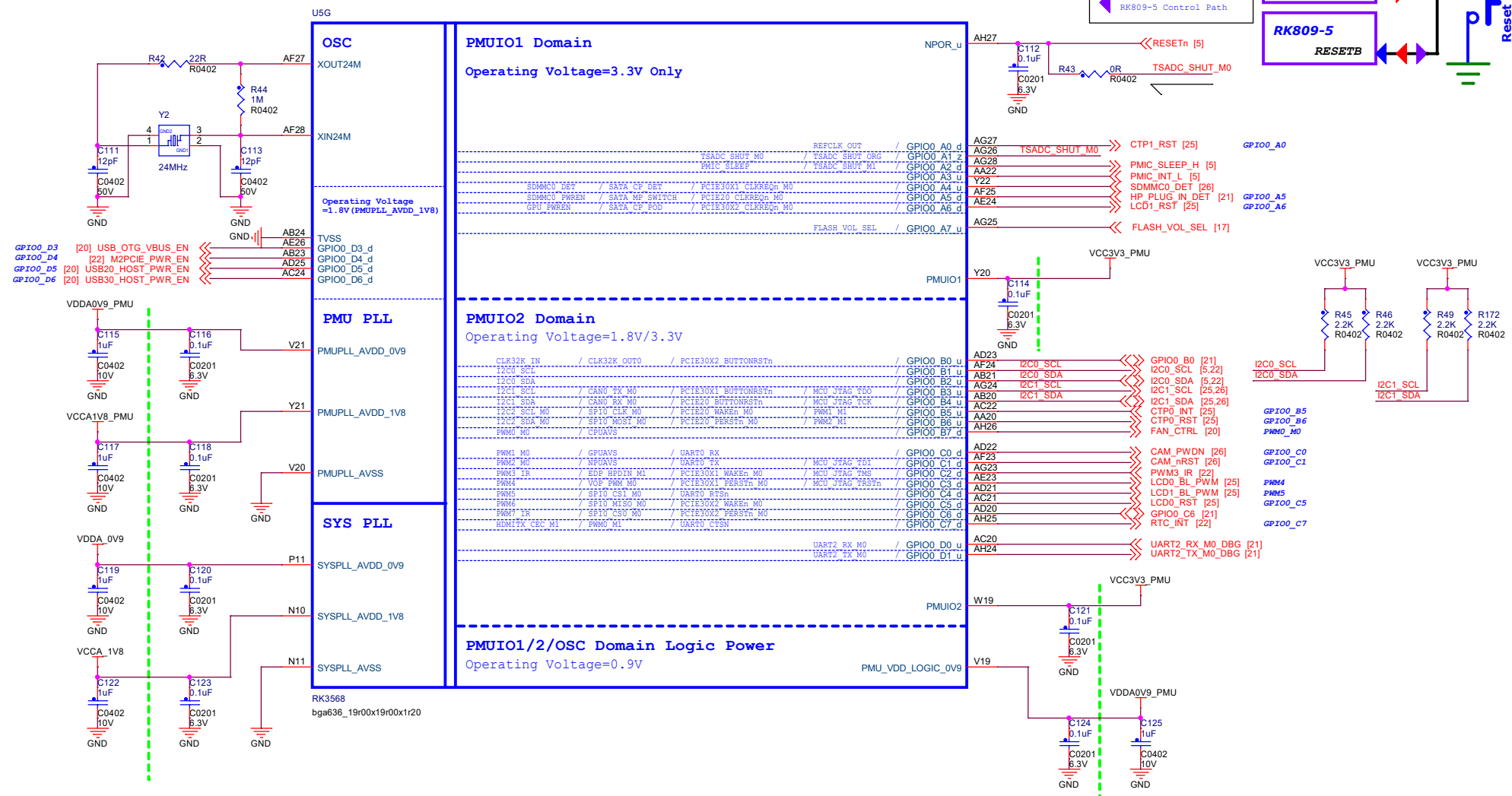
RK3568 PWR



RK3568 DDR PHY



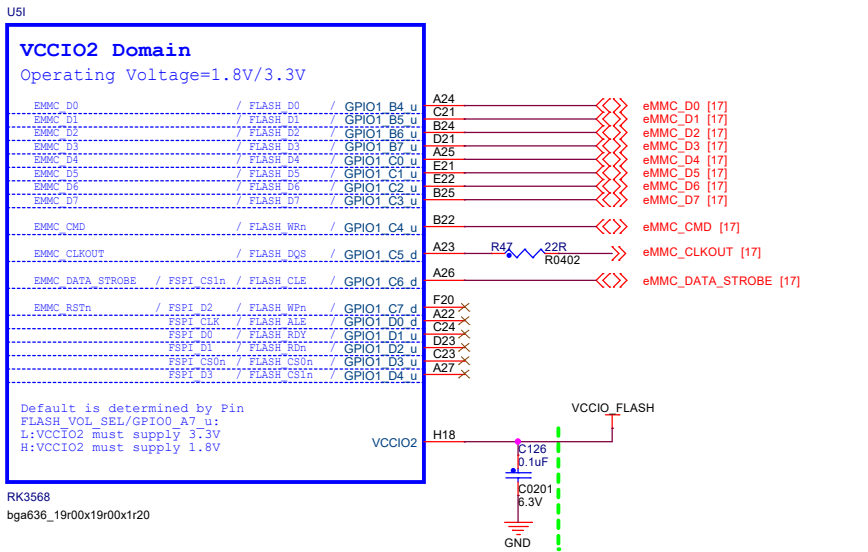
RK3568 OSC/PLL/PMUIO



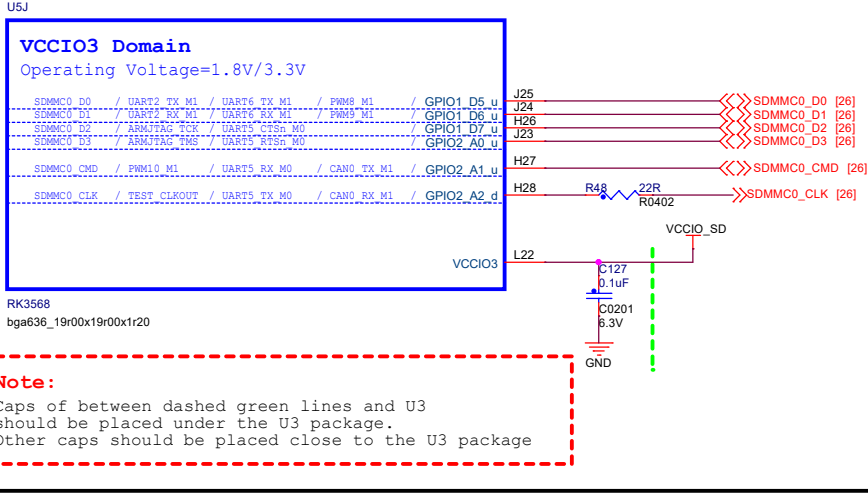
Note:

Caps of between dashed green lines and U3
should be placed under the U3 package.
Other caps should be placed close to the U3 package

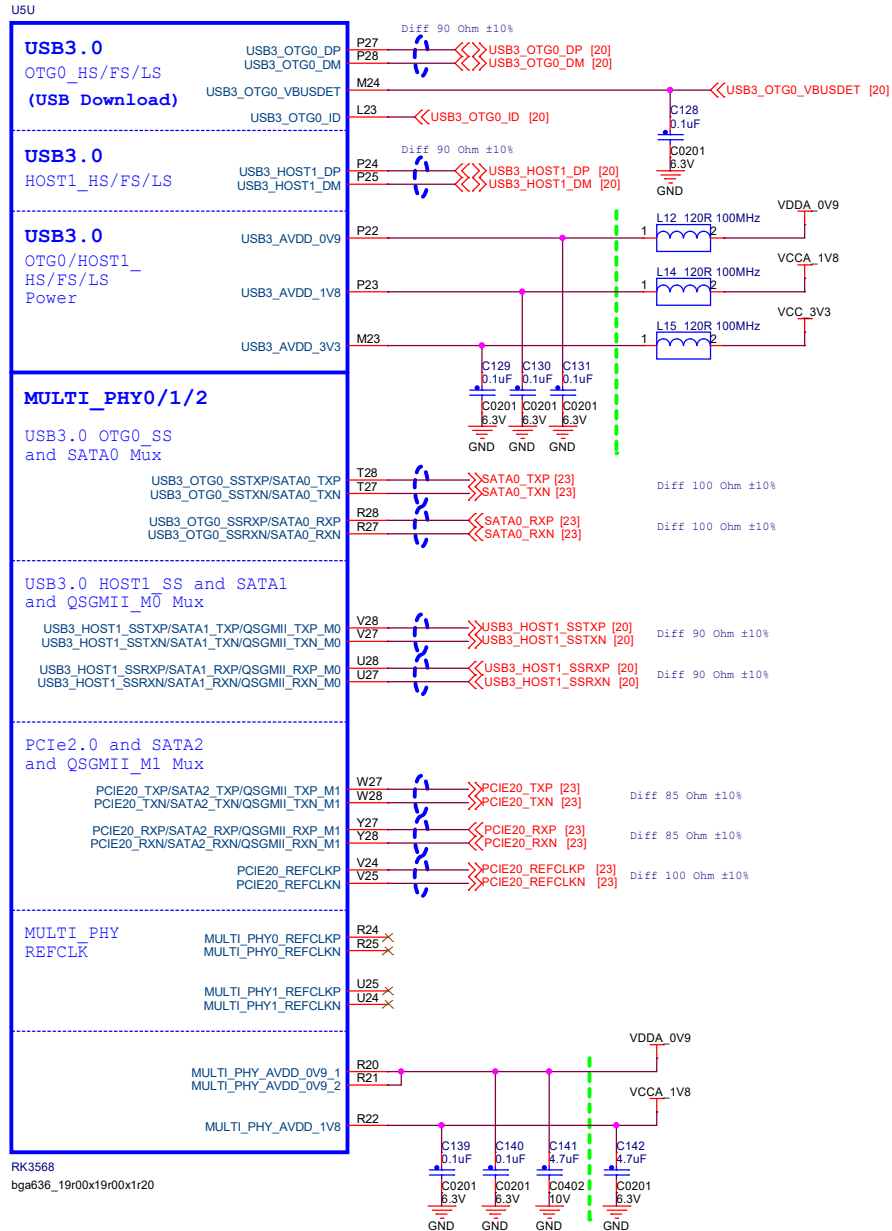
RK3568 VCCIO2 Domain



RK3568 VCCIO3 Domain



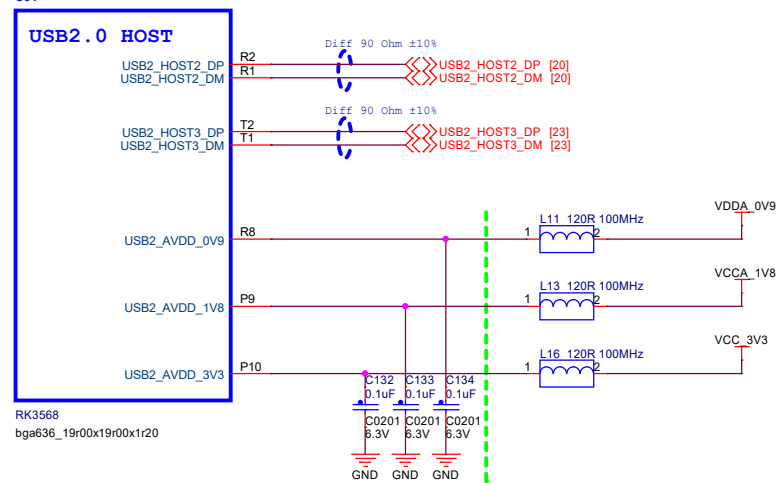
RK3568 USB3.0/SATA/QSGMII/PCIE2.0 x1



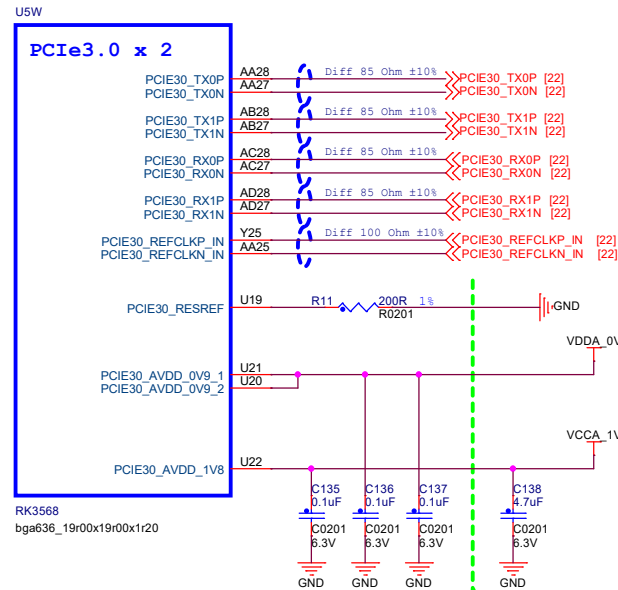
Note:

Caps of between dashed green lines and U3 should be placed under the U3 package.
Other caps should be placed close to the U3 package

RK3568 USB2.0 HOST



RK3568 PCIE3.0 x2



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Size A3	Document Number USB/PCIE/STAT PHY	Rev V1.0
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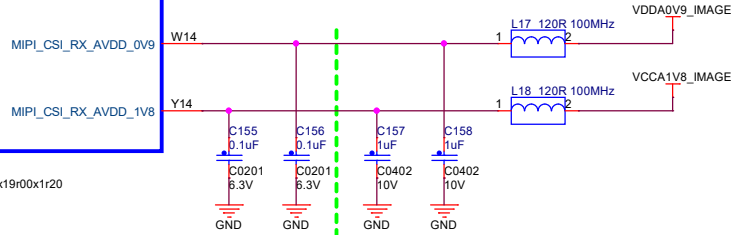
RK3568 MIPI_CSI_RX

U5P

MIPI CSI RX

MIPI_CSI_RX_D0P	AG12	Diff 100 Ohm ±10%	MIPI_CSI_RX_D0P [26]
MIPI_CSI_RX_D0N	AH12		MIPI_CSI_RX_D0N [26]
MIPI_CSI_RX_D1P	AG11	Diff 100 Ohm ±10%	MIPI_CSI_RX_D1P [26]
MIPI_CSI_RX_D1N	AH11		MIPI_CSI_RX_D1N [26]
MIPI_CSI_RX_D2P	AE11	Diff 100 Ohm ±10%	MIPI_CSI_RX_D2P [26]
MIPI_CSI_RX_D2N	AD11		MIPI_CSI_RX_D2N [26]
MIPI_CSI_RX_D3P	AD9	Diff 100 Ohm ±10%	MIPI_CSI_RX_D3P [26]
MIPI_CSI_RX_D3N	AE9		MIPI_CSI_RX_D3N [26]
MIPI_CSI_RX_CLK0P	AG10	Diff 100 Ohm ±10%	MIPI_CSI_RX_CLK0P [26]
MIPI_CSI_RX_CLK0N	AH10		MIPI_CSI_RX_CLK0N [26]
MIPI_CSI_RX_CLK1P	AG9	Diff 100 Ohm ±10%	MIPI_CSI_RX_CLK1P [26]
MIPI_CSI_RX_CLK1N	AH9		MIPI_CSI_RX_CLK1N [26]

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1



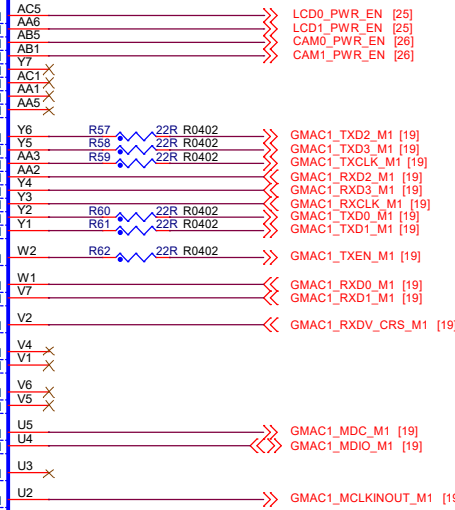
RK3568 VCCIO6 Domain

U5M

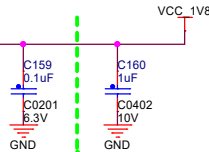
VCCIO6 Domain

Operating Voltage=1.8V/3.3V

CIF_D0	/ EBC SDD00	/ SDMMC2_D0_M0	/ I2S1_MCLK_M1	/ VOP_BT656_D0_M1	/ GPIO3_C6_d
CIF_D1	/ EBC SDD01	/ SDMMC2_D1_M0	/ I2S1_SCLK_TX_M1	/ VOP_BT656_D1_M1	/ GPIO3_C7_d
CIF_D2	/ EBC SDD02	/ SDMMC2_D2_M0	/ I2S1_LCLK_TX_M1	/ VOP_BT656_D2_M1	/ GPIO3_D0_d
CIF_D3	/ EBC SDD03	/ SDMMC2_D3_M0	/ I2S1_SDO0_M1	/ VOP_BT656_D3_M1	/ GPIO3_D1_d
CIF_D4	/ EBC SDD04	/ SDMMC2_D4_M0	/ I2S1_SDO1_M1	/ VOP_BT656_D4_M1	/ GPIO3_D2_d
CIF_D5	/ EBC SDD05	/ SDMMC2_D5_M0	/ I2S1_SDO2_M1	/ VOP_BT656_D5_M1	/ GPIO3_D3_d
CIF_D6	/ EBC SDD06	/ SDMMC2_DET_M0	/ I2S1_SDO2_M1	/ VOP_BT656_D6_M1	/ GPIO3_D4_d
CIF_D7	/ EBC SDD07	/ SDMMC2_PAREN_M0	/ I2S1_SDO3_M1	/ VOP_BT656_D7_M1	/ GPIO3_D5_d
CIF_D8	/ EBC SDD08	/ GMAC1_TXD2_M1	/ UART1_TX_M1	/ PDM_CLK0_M1	/ GPIO3_D6_d
CIF_D9	/ EBC SDD09	/ GMAC1_TXD3_M1	/ UART1_RX_M1	/ PDM_SDO1_M1	/ GPIO3_D7_d
CIF_D10	/ EBC SDD010	/ GMAC1_RXCLK_M1	/ UART1_TX_M1	/ PDM_CLK1_M1	/ GPIO4_A0_d
CIF_D11	/ EBC SDD011	/ GMAC1_RXD2_M1	/ UART1_TX_M2	/ PDM_SDO1_M1	/ GPIO4_A1_d
CIF_D12	/ EBC SDD012	/ GMAC1_RXD3_M1	/ UART1_TX_M2	/ PDM_SDO2_M1	/ GPIO4_A2_d
CIF_D13	/ EBC SDD013	/ GMAC1_RXD0_M1	/ UART1_RX_M2	/ PDM_SDO3_M1	/ GPIO4_A3_d
CIF_D14	/ EBC SDD014	/ GMAC1_TXD0_M1	/ UART1_RX_M2	/ I2S2_LCLK_RX_M1	/ GPIO4_A4_d
CIF_D15	/ EBC SDD015	/ GMAC1_TXD1_M1	/ UART1_RX_M2	/ I2S2_LCLK_RX_M1	/ GPIO4_A5_d
ISP_FLASHTRIGOUT	/ EBC SDCE0	/ GMAC1_TXEN_M1	/ SPI3_CS0_M0	/ I2S1_SCLK_RX_M1	/ GPIO4_A6_d
CAM_CLKOUT0	/ EBC SDCE1	/ GMAC1_RXD0_M1	/ SPI3_CS1_M0	/ I2S1_LCLK_RX_M1	/ GPIO4_A7_d
CAM_CLKOUT1	/ EBC SDCE2	/ GMAC1_RXD1_M1	/ SPI3_MISO_M0	/ I2S1_SDO1_M1	/ GPIO4_B0_d
ISP_PRELIGHT_TRIG	/ EBC SDCE3	/ GMAC1_RXDV_CRS_M1	/ I2S1_SDO2_M1	/ I2S1_SDO2_M1	/ GPIO4_B1_d
I2C4_SDA_M0	/ EBC VCOM	/ GMAC1_RXER_M1	/ SPI3_MOSI_M0	/ I2S2_SDI_M1	/ GPIO4_B2_d
I2C4_SCL_M0	/ EBC GD08	/ ETH1_REFCLK0_25M_M1	/ SPI3_CLK_M0	/ I2S2_SDO_M1	/ GPIO4_B3_d
I2C2_SDA_M1	/ EBC GDSP	/ CAN2_RX_M0	/ I2S2_SDO1_M1	/ I2S2_SDO1_M1	/ GPIO4_B4_d
I2C2_SCL_M1	/ EBC SD58A	/ CAN2_TX_M0	/ I2S1_SDO2_M1	/ I2S1_SDO2_M1	/ GPIO4_B5_d
CIF_HREF	/ EBC SDLE	/ GMAC1_MDC_M1	/ UART1_RTS_M1	/ I2S2_MCLK_M1	/ GPIO4_B6_d
CIF_VSYNC	/ EBC SD0E	/ GMAC1_MDIO_M1	/ I2S2_SCLK_TX_M1	/ I2S2_SCLK_TX_M1	/ GPIO4_B7_d
CIF_CLKOUT	/ EBC GDCLK	/ GMAC1_MDC_M1	/ PWM1_IR_M1	/ I2S2_SCLK_TX_M1	/ GPIO4_C0_d
CIF_CLKIN	/ EBC SDCLK	/ GMAC1_MCLKINOUT_M1	/ UART1_CTS_M1	/ I2S2_SCLK_RX_M1	/ GPIO4_C1_d



RK3568
bga636_19r00x19r00x1r20



Note:

Caps of between dashed green lines and U3 should be placed under the U3 package. Other caps should be placed close to the U3 package

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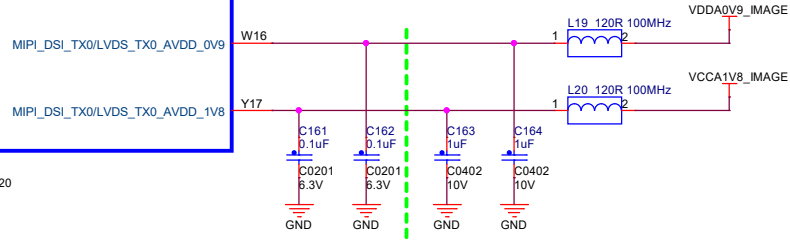
Title 野火_EBF RK3568 LBC		
Size A3	Document Number VI Interface	Rev V1.0
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RK3568 MIPI_DSI_TX0/LVDS_TX0

U5R

MIPI DSI TX0/LVDS TX0

MIPI_DSI_TX0_D0P/LVDS_TX0_D0P AH17 Diff 100 Ohm ±10% MIPI_DSI_TX0_D0P [25]
 MIPI_DSI_TX0_D0N/LVDS_TX0_D0N AG17 MIPI_DSI_TX0_D0N [25]
 MIPI_DSI_TX0_D1P/LVDS_TX0_D1P AH16 Diff 100 Ohm ±10% MIPI_DSI_TX0_D1P [25]
 MIPI_DSI_TX0_D1N/LVDS_TX0_D1N AG16 MIPI_DSI_TX0_D1N [25]
 MIPI_DSI_TX0_D2P/LVDS_TX0_D2P AH14 Diff 100 Ohm ±10% MIPI_DSI_TX0_D2P [25]
 MIPI_DSI_TX0_D2N/LVDS_TX0_D2N AG14 MIPI_DSI_TX0_D2N [25]
 MIPI_DSI_TX0_D3P/LVDS_TX0_D3P AH13 Diff 100 Ohm ±10% MIPI_DSI_TX0_D3P [25]
 MIPI_DSI_TX0_D3N/LVDS_TX0_D3N AG13 MIPI_DSI_TX0_D3N [25]
 MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP AH15 Diff 100 Ohm ±10% MIPI_DSI_TX0_CLKP [25]
 MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN AG15 MIPI_DSI_TX0_CLKN [25]



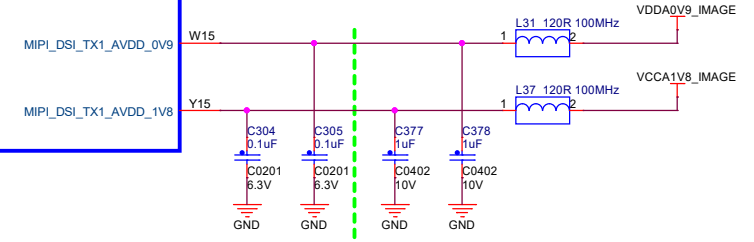
RK3568
bga636_19r00x19r00x1r20

RK3568 MIPI_DSI_TX1

U5S

MIPI DSI TX1

MIPI_DSI_TX1_D0P Diff 100 Ohm ±10% MIPI_DSI_TX1_D0P [25]
 MIPI_DSI_TX1_D0N AE18 MIPI_DSI_TX1_D0N [25]
 MIPI_DSI_TX1_D1P Diff 100 Ohm ±10% MIPI_DSI_TX1_D1P [25]
 MIPI_DSI_TX1_D1N AC17 MIPI_DSI_TX1_D1N [25]
 MIPI_DSI_TX1_D2P Diff 100 Ohm ±10% MIPI_DSI_TX1_D2P [25]
 MIPI_DSI_TX1_D2N AC14 MIPI_DSI_TX1_D2N [25]
 MIPI_DSI_TX1_D3P Diff 100 Ohm ±10% MIPI_DSI_TX1_D3P [25]
 MIPI_DSI_TX1_D3N AE12 MIPI_DSI_TX1_D3N [25]
 MIPI_DSI_TX1_CLKP Diff 100 Ohm ±10% MIPI_DSI_TX1_CLKP [25]
 MIPI_DSI_TX1_CLKN AE15 MIPI_DSI_TX1_CLKN [25]



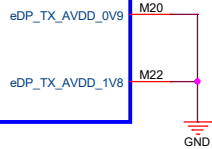
RK3568
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RK3568 eDP TX

U5T

eDP_TX

eDP_TX_D0P J28 X
 eDP_TX_D0N K27 X
 eDP_TX_D1P K28 X
 eDP_TX_D1N L27 X
 eDP_TX_D2P L28 X
 eDP_TX_D2N M27 X
 eDP_TX_D3P M28 X
 eDP_TX_D3N N27 X
 eDP_TX_AUXP L25 X
 eDP_TX_AUXN M25 X



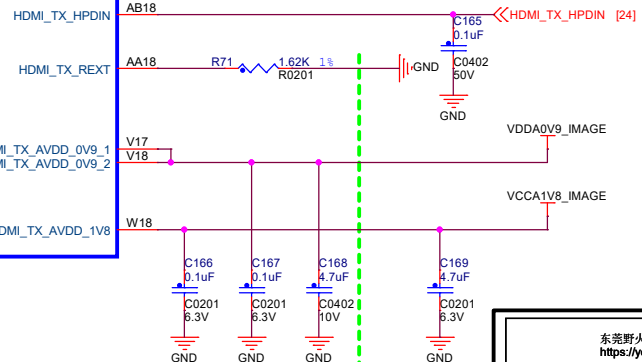
RK3568
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RK3568 HDMI2.0 TX

U5Q

HDMI2.0 TX

HDMI_TX_D2P Diff 100 Ohm ±10% R63 2.2R R0201 HDMI_TX2P_PORT [24]
 HDMI_TX_D2N AH22 R64 2.2R R0201 HDMI_TX2N_PORT [24]
 HDMI_TX_D1P AG21 R65 2.2R R0201 HDMI_TX1P_PORT [24]
 HDMI_TX_D1N AH21 R66 2.2R R0201 HDMI_TX1N_PORT [24]
 HDMI_TX_D0P AG20 R67 2.2R R0201 HDMI_TX0P_PORT [24]
 HDMI_TX_D0N AH20 R68 2.2R R0201 HDMI_TX0N_PORT [24]
 HDMI_TX_CLKP AH19 2.2R R0201 HDMI_TXCLKP_PORT [24]
 HDMI_TX_CLKN AG19 R70 2.2R R0201 HDMI_TXCLKN_PORT [24]



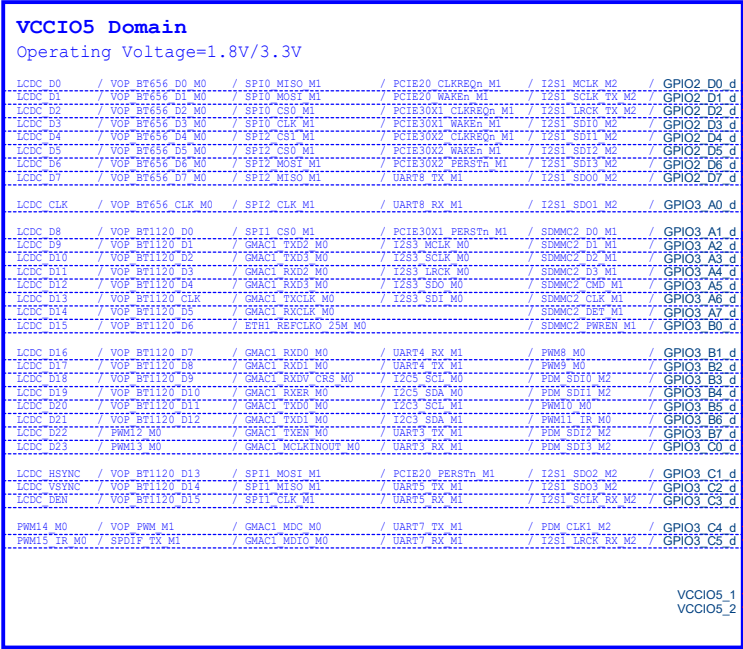
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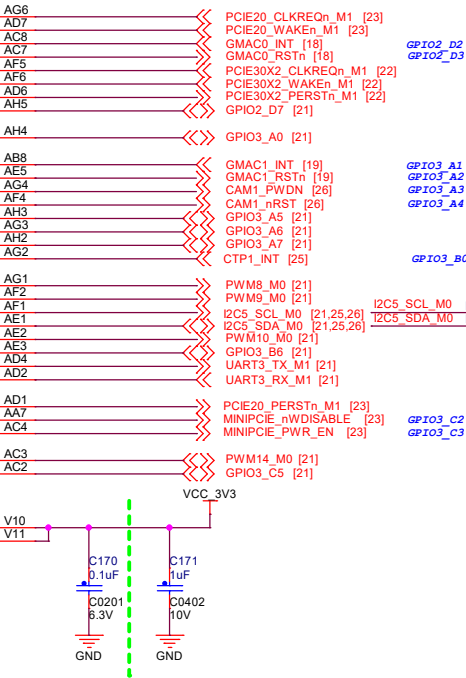
Title		
野火_EBF RK3568 LBC		
Size	Document Number	Rev
A3	VO Interface_1	V1.0
Date: Saturday, March 23, 2024		
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RK3568 VCCIO5 Domain

USL



RK3568
bga636_19r00x19r00x120



Note:

Caps of between dashed green lines and U3 should be placed under the U3 package.
Other caps should be placed close to the U3 package

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Title 野火_EBF RK3568 LBC		
Size A3	Document Number VO Interface_2	Rev V1.0
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U5H

Operating Voltage=1.8V/3.3V

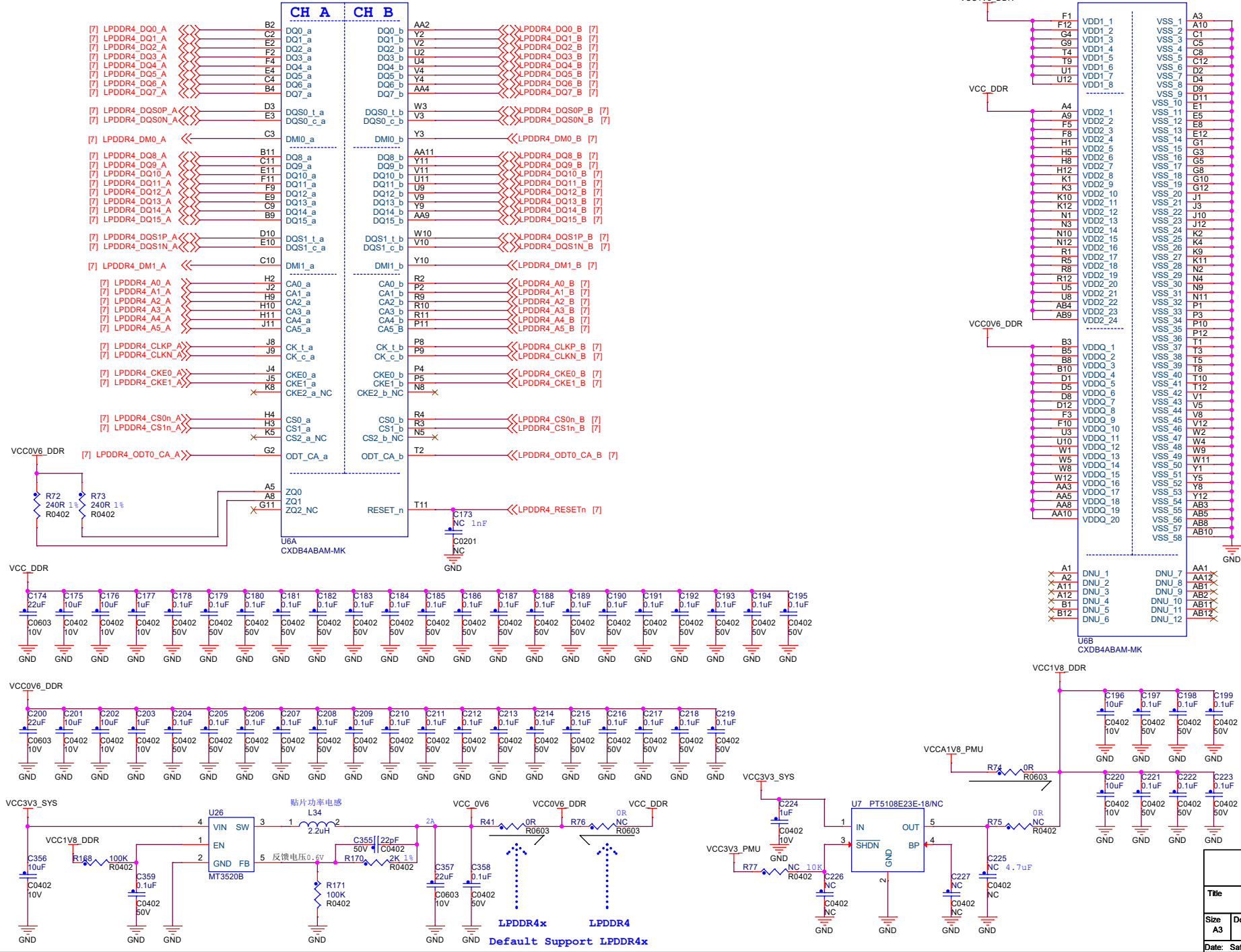
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VCCIO1

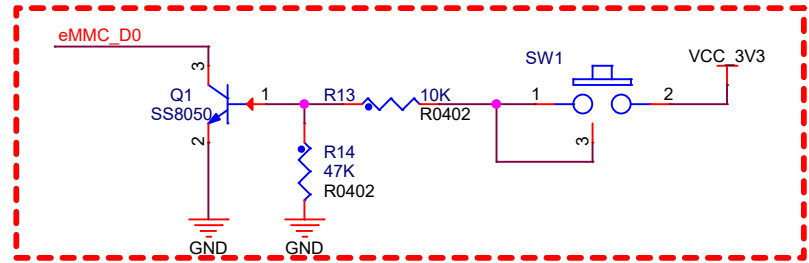
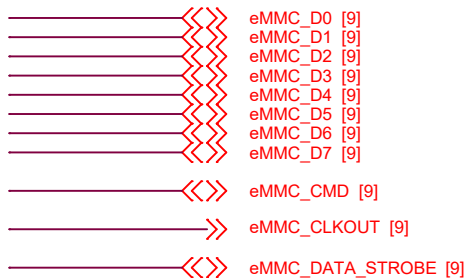
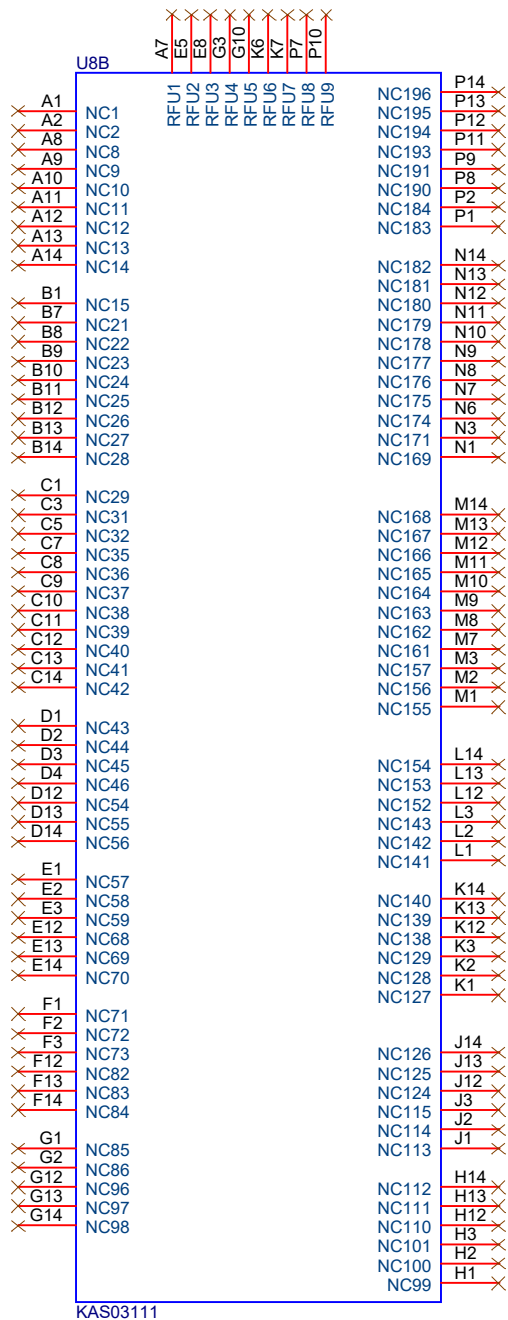
Caps of between dashed green lines and U3
should be placed under the U3 package.
Other caps should be placed close to the U3 package



LPDDR4/4x

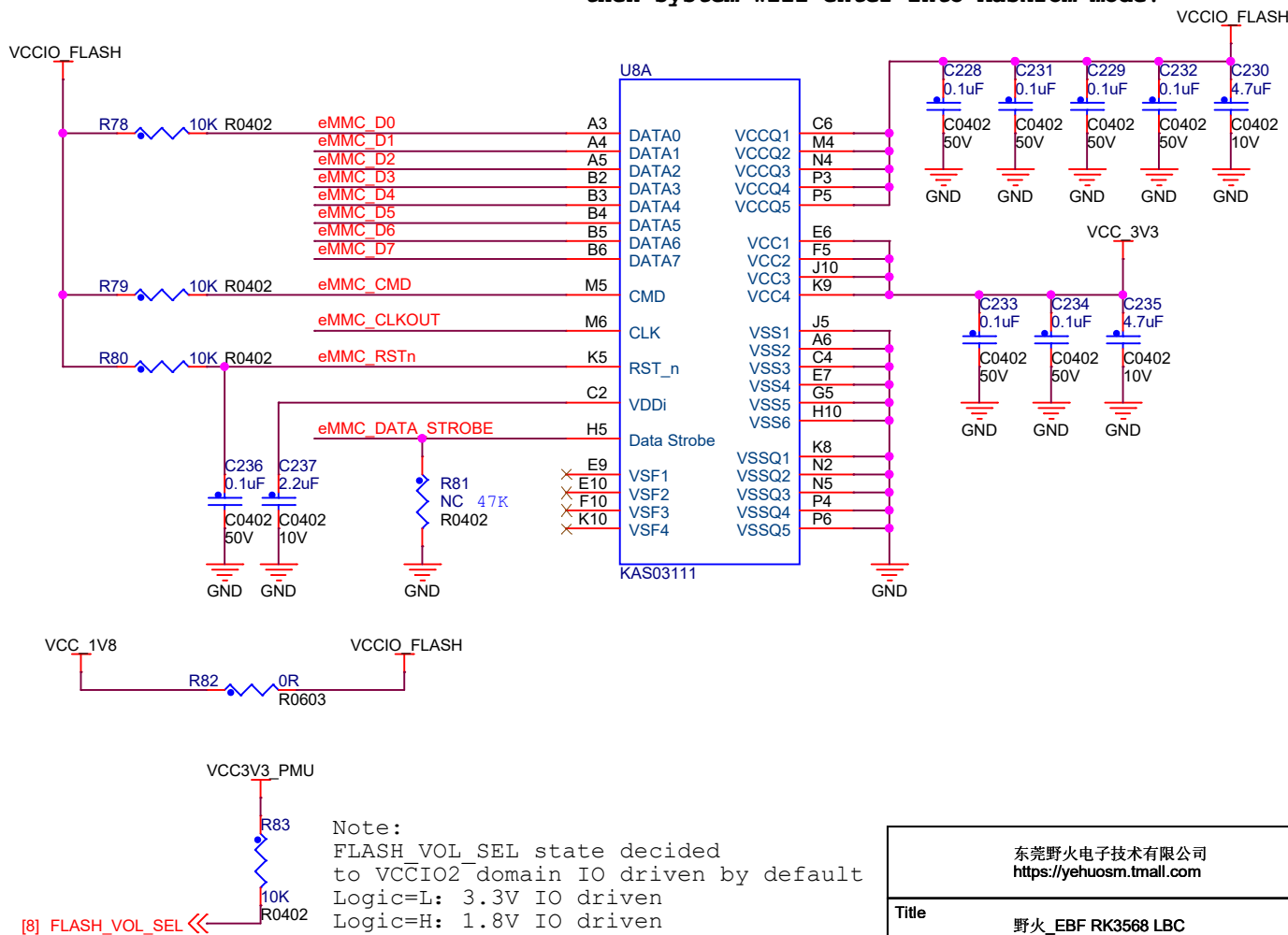


eMMC Flash



Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset,
then system will enter into Maskrom mode.



Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

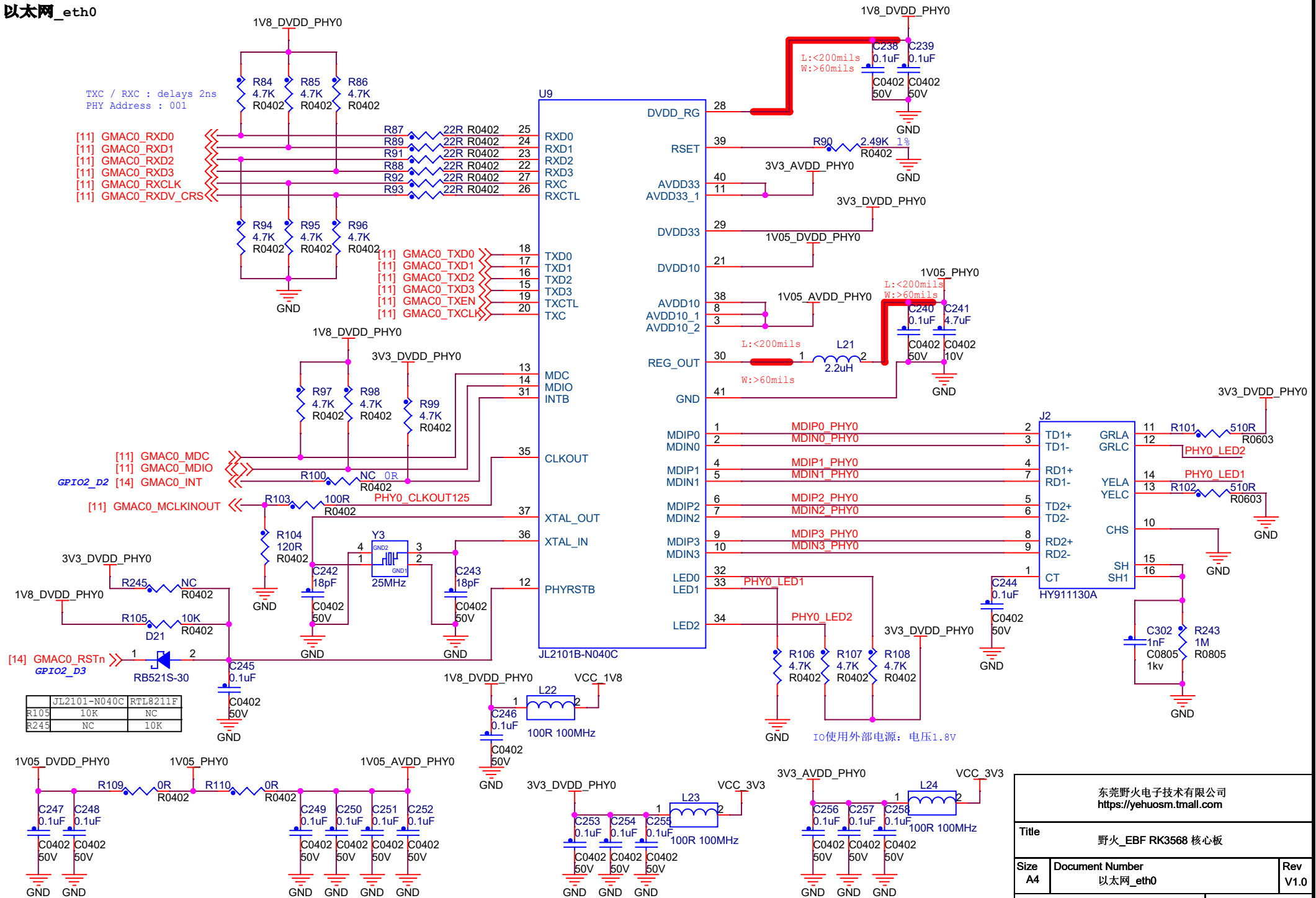
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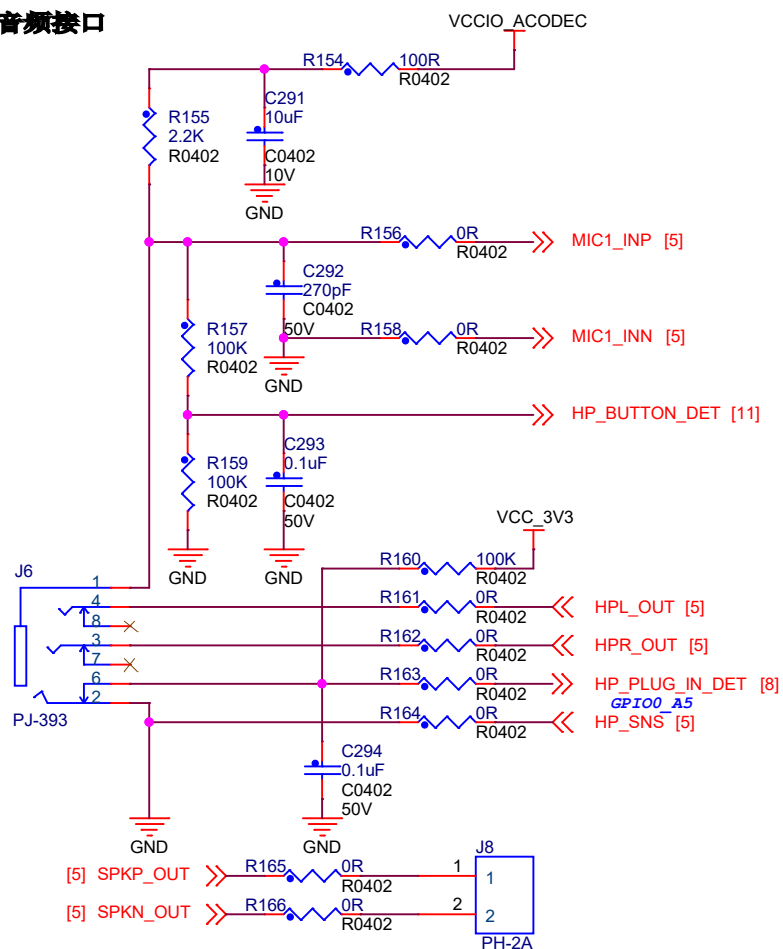
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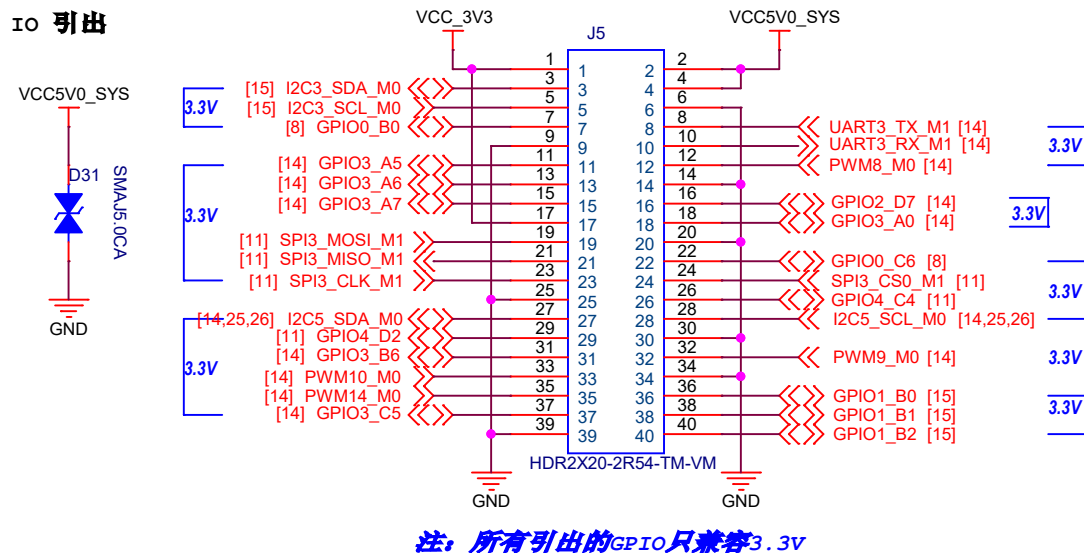
以太网_eth0



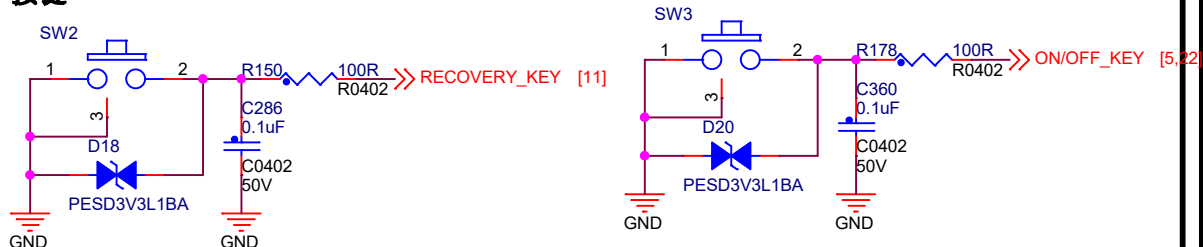
音频接口



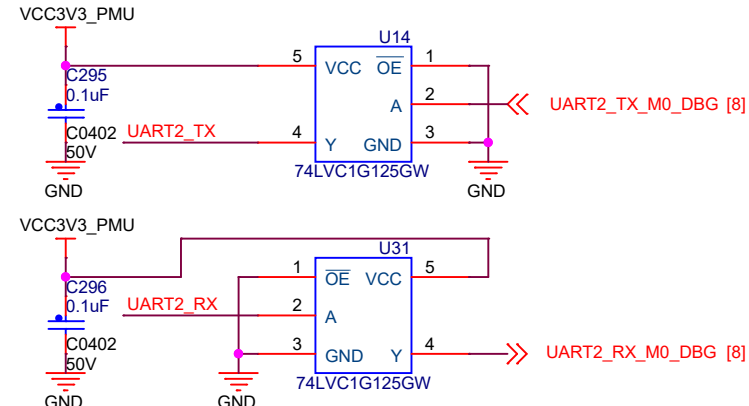
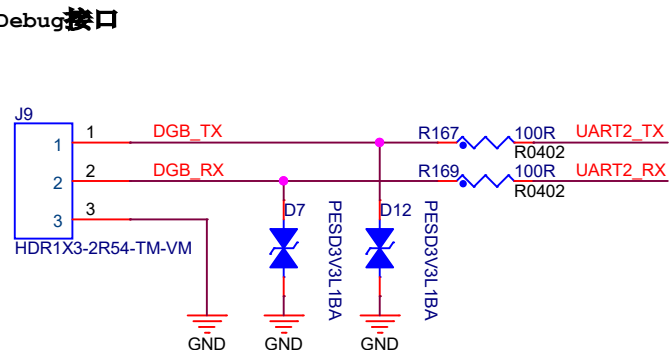
IO 引出



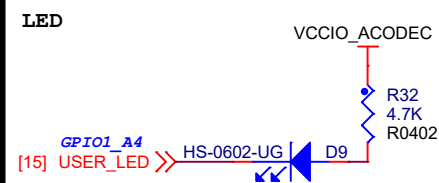
按键



Debug接口

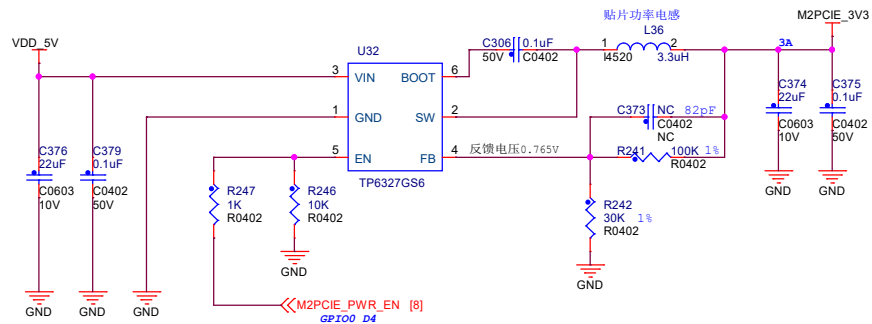


LED

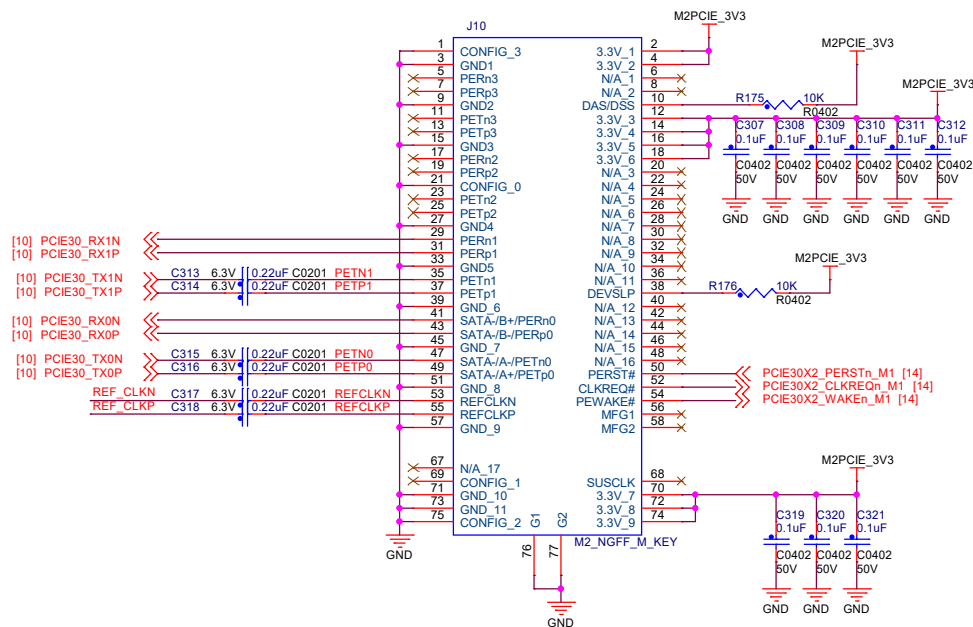


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Size A4	Document Number 音频/DEBUG/IO引出/按键/LED	Rev V1.0
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M.2 PCIE POWER 3.3V



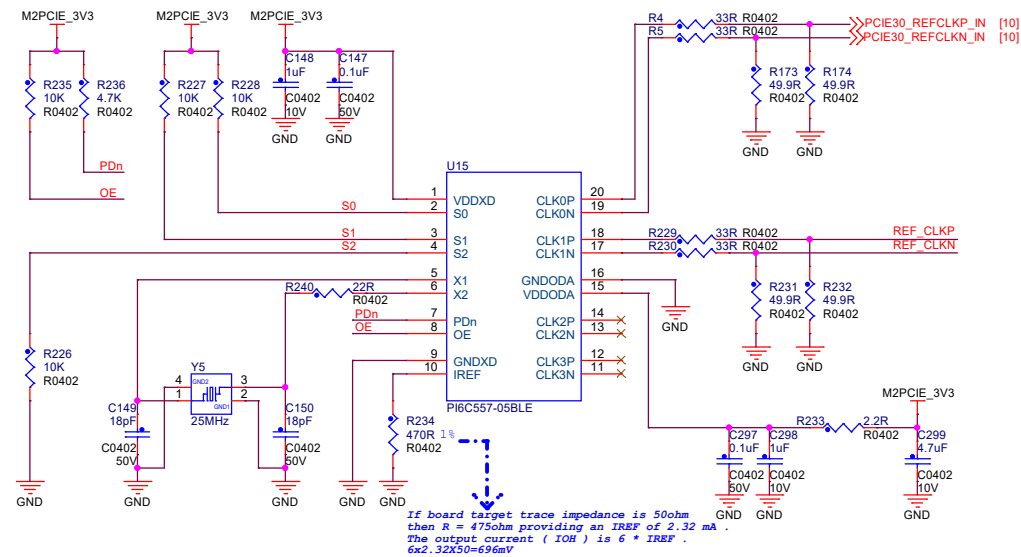
M.2 PCIE3.0 x 2Lanes



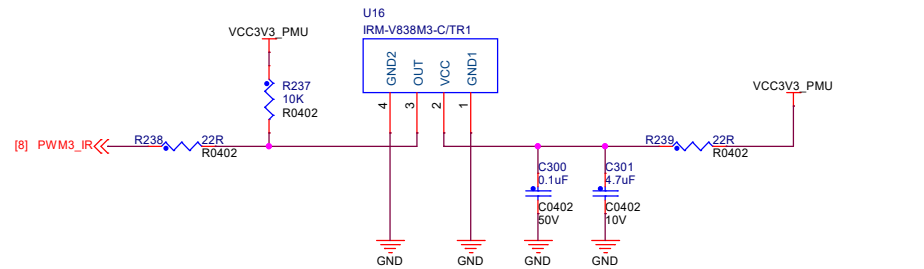
贴片螺母



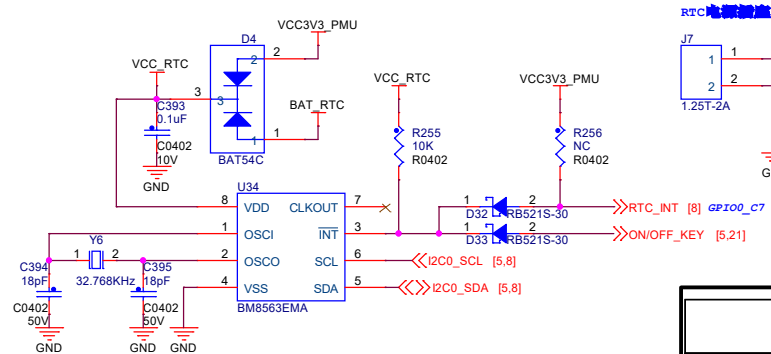
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M.2 PCIE REF_CLKP 100MHz
```



IR 接收器



RTC



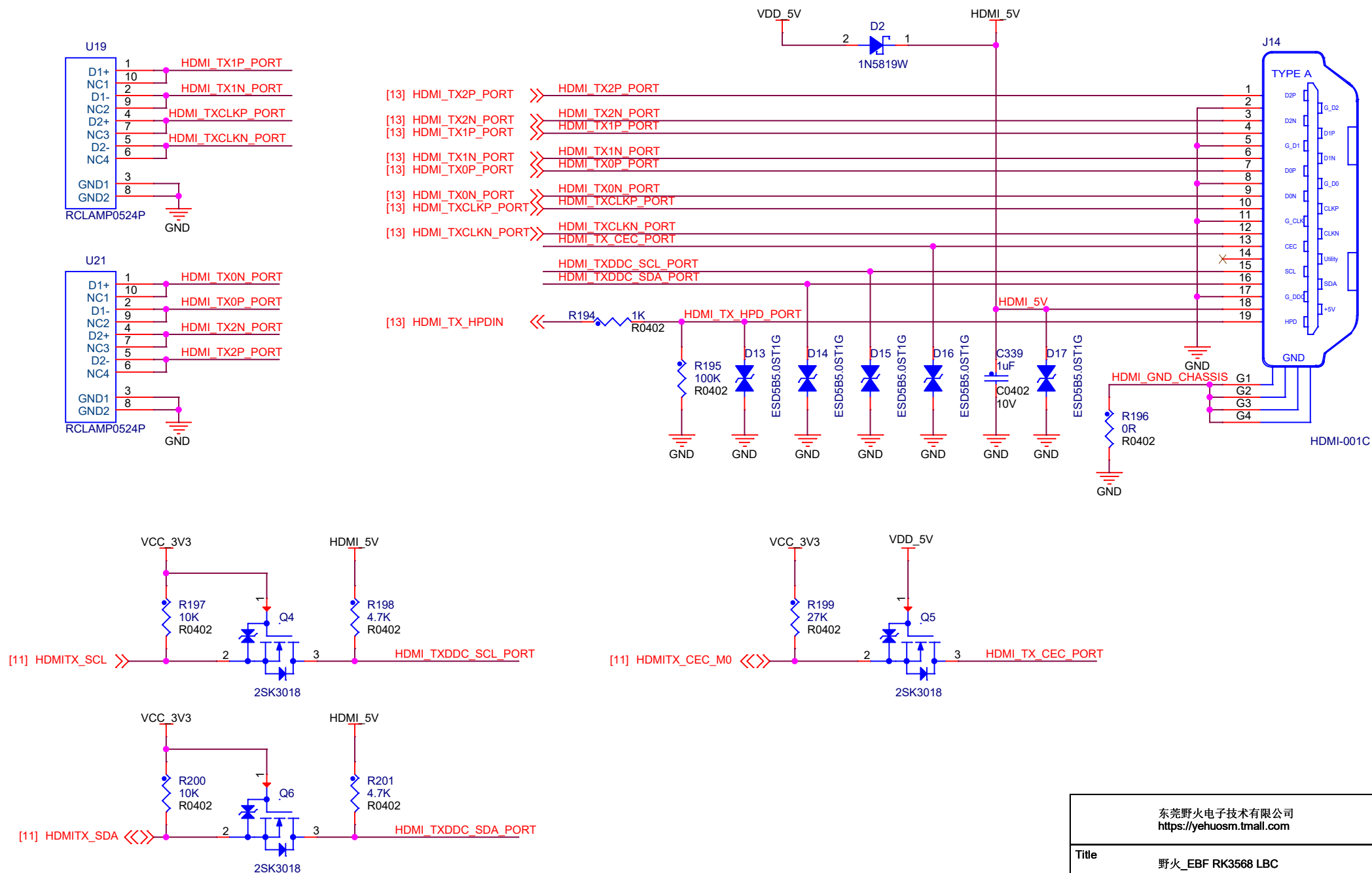
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Size	Document Number
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A3	M.2 PCIE3.0接口/R接收器
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HDMI 2.0接口



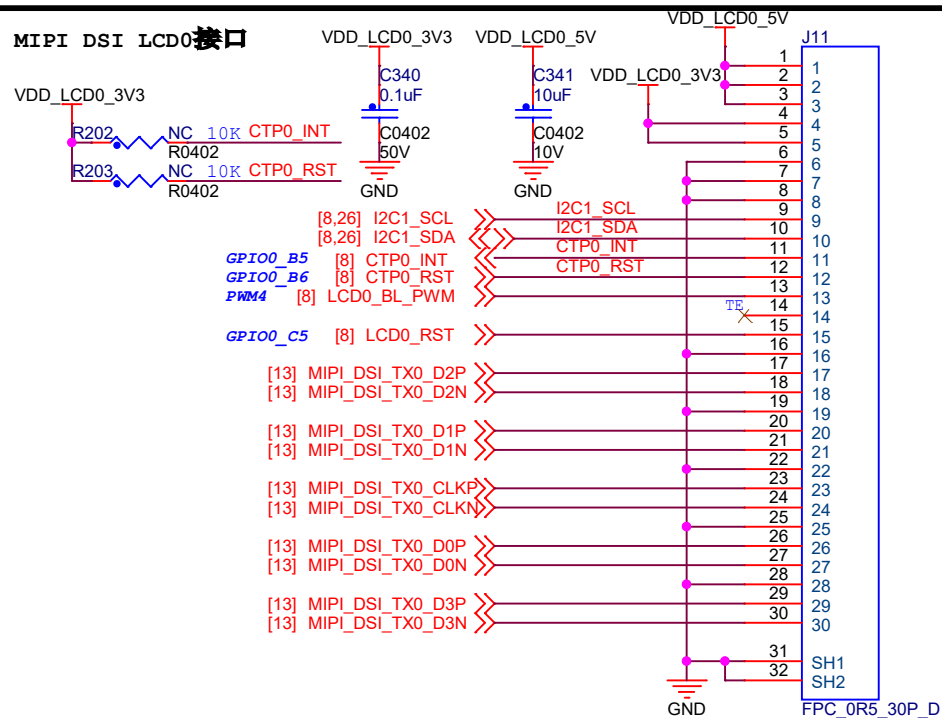
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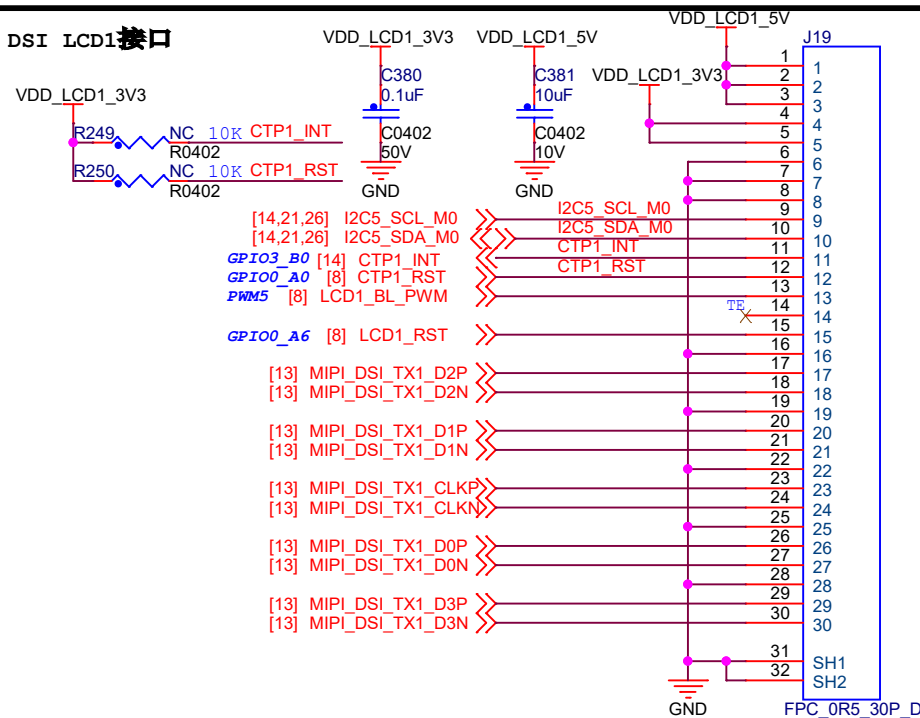
Size A4	Document Number M.2 PCIE3.0接口	Rev V1.0
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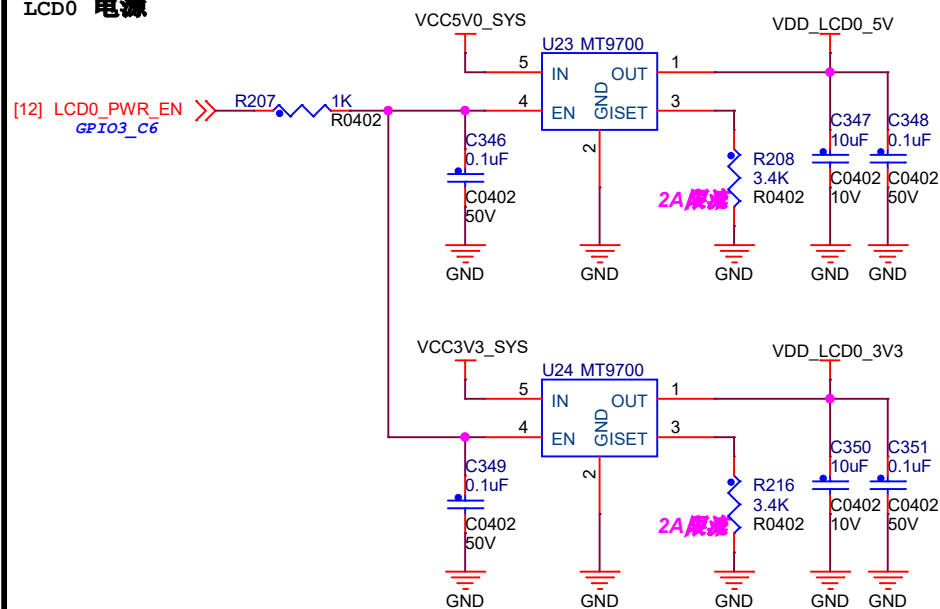
MIPI DSI LCD0接口



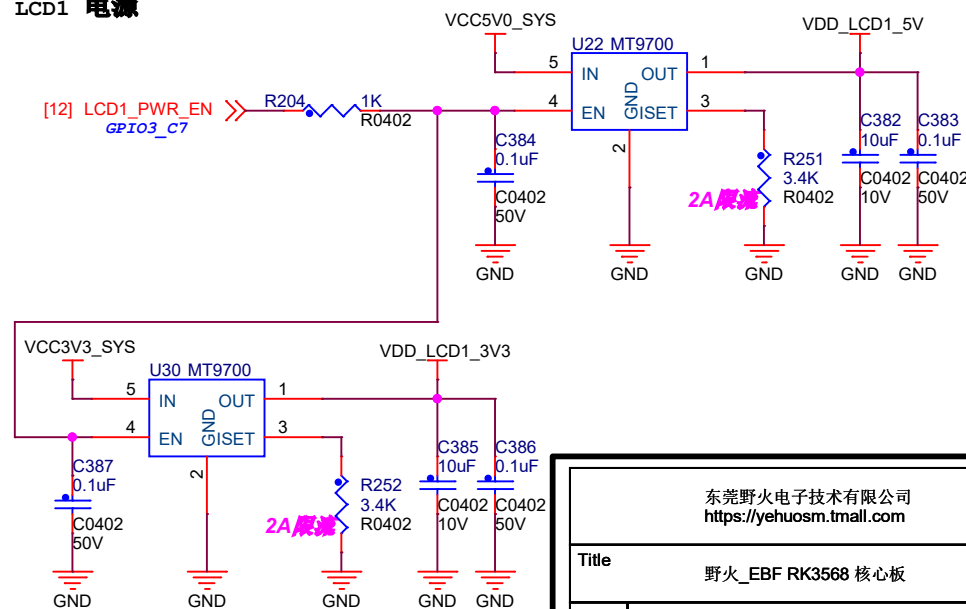
MIPI DSI LCD1接口



LCD0 电源



LCD1 电源



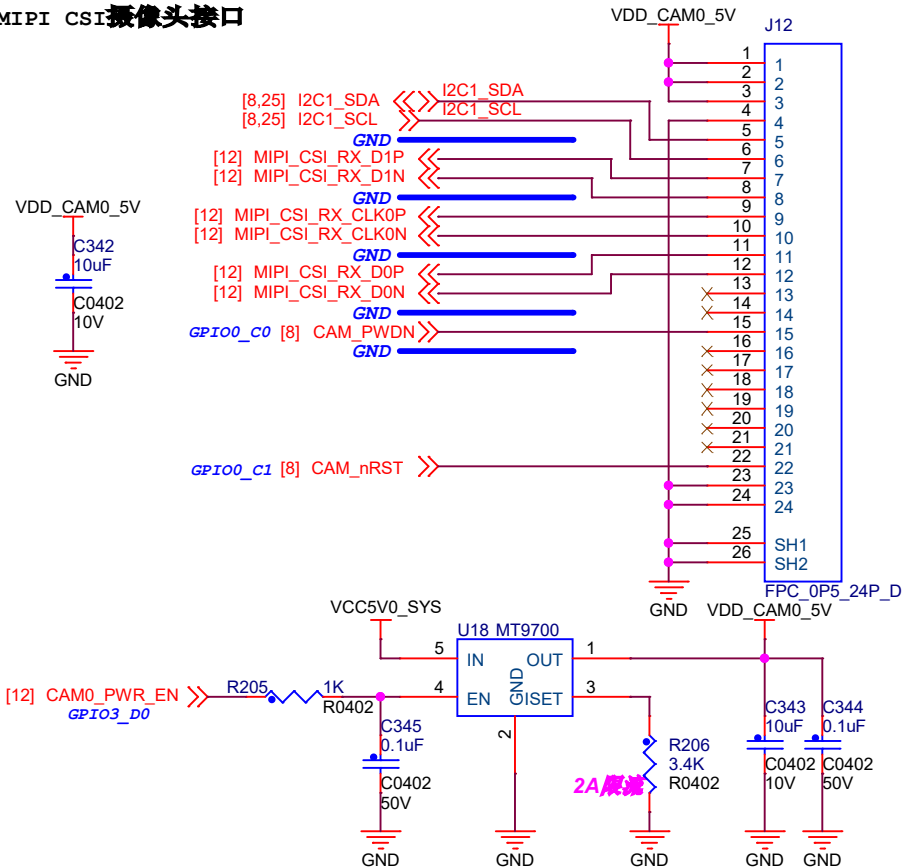
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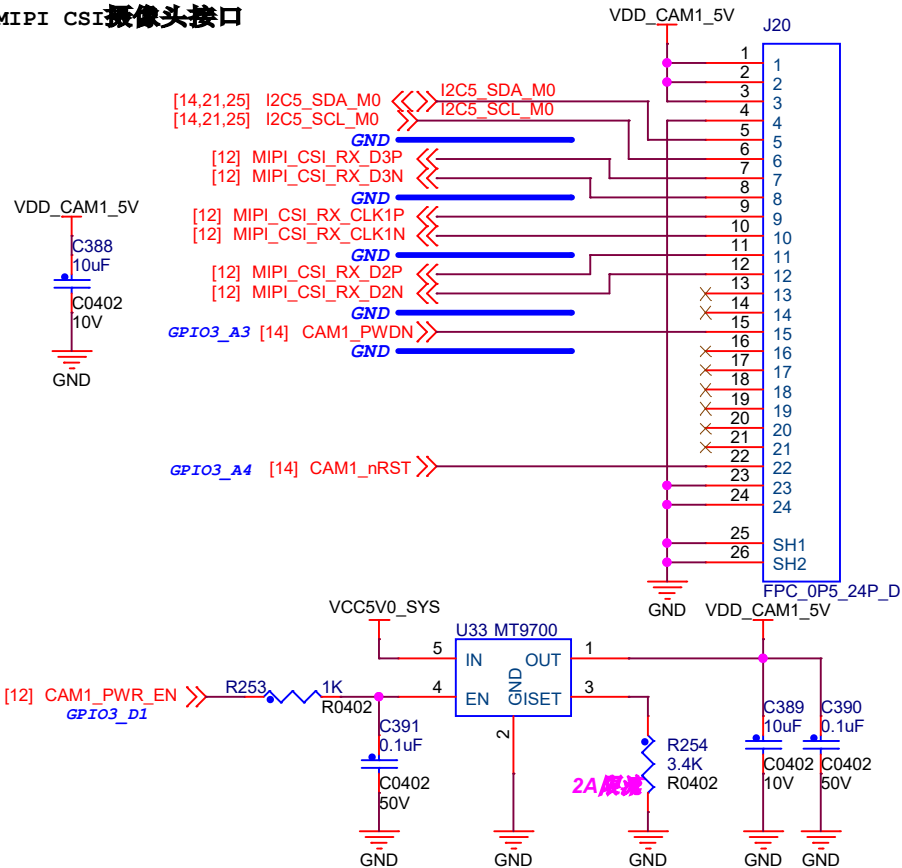
Size A4 Document Number M.2 PCIe3.0接口 Rev V1.0

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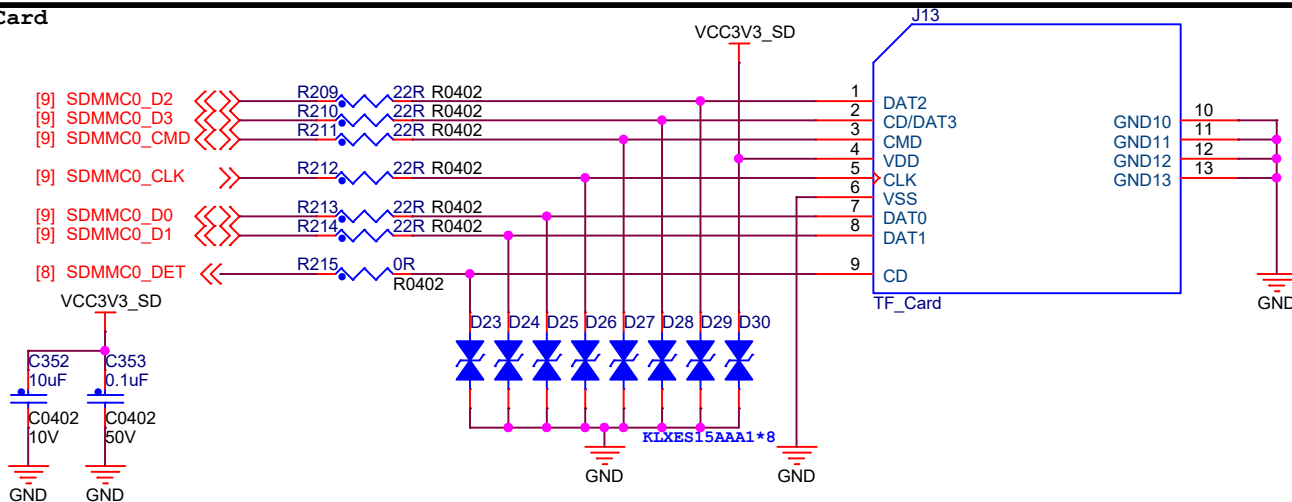
MIPI CSI摄像头接口



MIPI CSI摄像头接口



SD Card



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A4	M.2 PCIe3.0接口	V1.0
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