

# 野火 EBF RK3568 LBC

Page 1	目录	Page 24	HDMI 接口
Page 2	历史版本	Page 25	MIPI DSI/MIPI CSI接口
Page 3	PWR TREE		
Page 4	电源		
Page 5	PMIC		
Page 6	CPU PWR		
Page 7	DDR PHY		
Page 8	OSC/PLL/PMUIO		
Page 9	Flash/SD Controller		
Page 10	USB/PCIe/SATA PHY		
Page 11	SARADC/GPIO		
Page 12	VI Interface		
Page 13	VO Interface_1		
Page 14	VO Interface_2		
Page 15	Audio Interface		
Page 16	LPDDR4/4x		
Page 17	eMMC Flash		
Page 18	以太网_1		
Page 19	以太网_2		
Page 20	USB HOST/USB OTG/FAN		
Page 21	音频/DEBUG/IO引出/按键/LED		
Page 22	M.2 PCIE3.0接口/IR接收器		
Page 23	MINI PCIE接口/SATA		

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Title 野火\_EBF RK3568 LBC

Size A4	Document Number 目录	Rev V1.0
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Date: Monday, December 12, 2022 Sheet 1 of 25

# 历史版本

版本号	日期	设计	描述
V1.0	2022-01-25	llm	初始版本, 开发阶段
V1.1	2022-05-18	llm	修复初始版本的一些问题, 增加SATA接口, typec添加OTG自动识别host/device功能
V1.2	2022-07-27	llm	1. MIPI CSI 添加2 Lanes 2. 更新MINI PCIE、M.2 PCIE封装, 添加独立的定位孔 3. 把Z4、Z3、Z2、Z1位号改前缀为D的位号 4. 把sim卡座位号U18改为J18 5. 把mini pcie位号CON1改为J17
V1.2	2022-11-29	llm	添加LPDDR4x注释, 电路不做任何更改
V1.3	2022-12-08	llm	1. 网口外壳增加阻容到地隔离 2. IR接收更换为PWM3_IR, IR接收器电源更改为VCC3V3_PMU, 以支持休眠唤醒 3. 修复以太网PHY复位引脚漏电问题, 并兼容RTL8211F

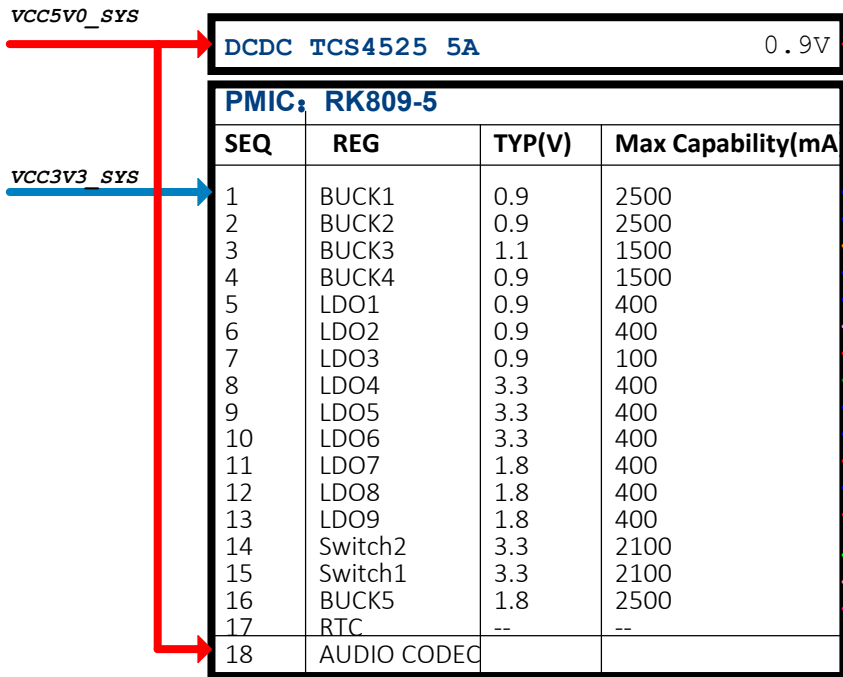
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Title 野火\_EBF RK3568 LBC

Size A4	Document Number 历史版本	Rev V1.0
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Date: Wednesday, July 12, 2023	Sheet 2 of 25
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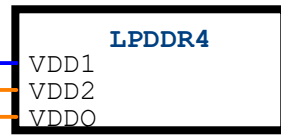
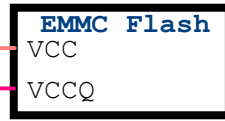
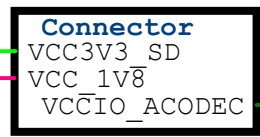
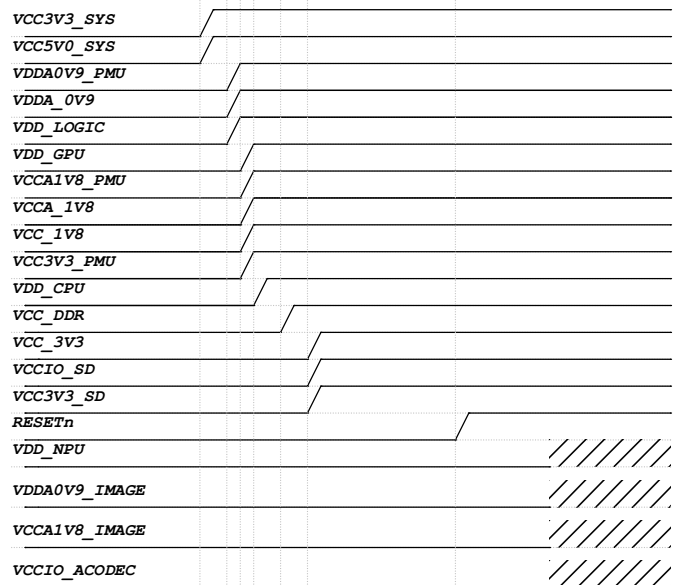
# PWR TREE



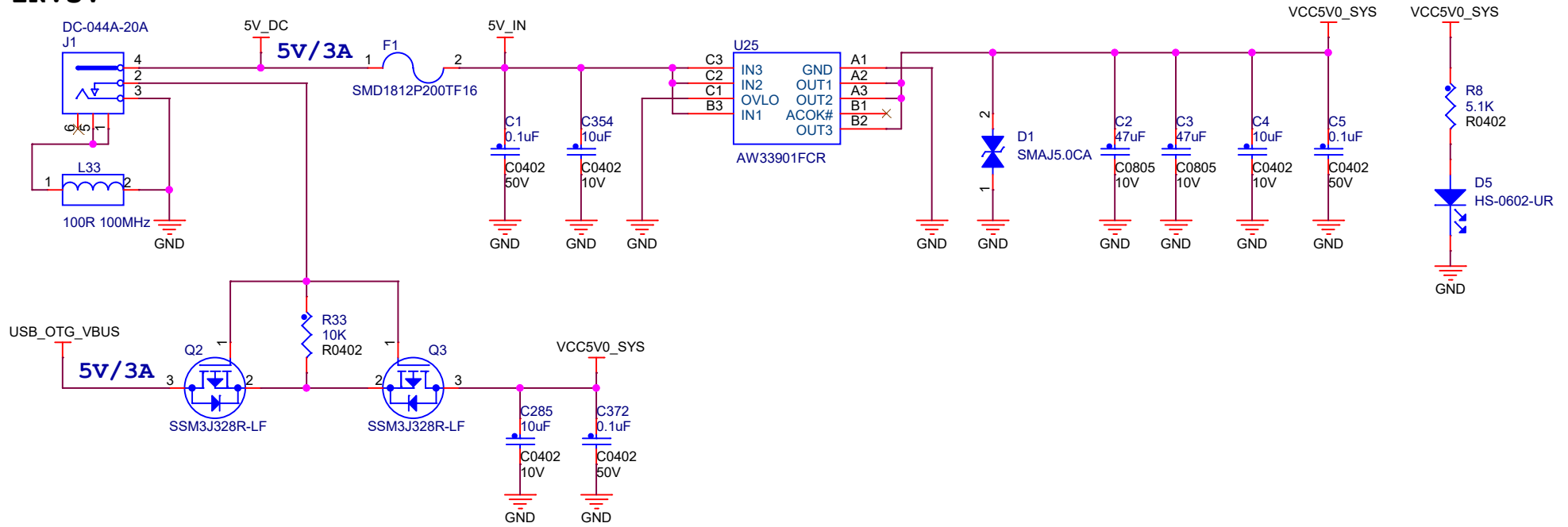
**CPU:RK3568**

SEQ	REG	TYP(V)
1	VDD_CPU	0.9
2	VDD_LOGIC	0.9
3	VDD_GPU	0.9
4	DDRPHY_VDDQ	1.1
	DDRPHY_VDDQL	1.1
5	VDD_NPU	0.9
6	MIPI_CSI_RX_AVDD_0V9(10mA)	0.9
	MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9(50mA)	0.9
	MIPI_DSI_TX1_AVDD_0V9(50mA)	0.9
	EDP_TX_AVDD_0V9(150mA)	0.9
	HDMI_TX_AVDD_0V9(25mA)	0.9
7	SYSPLL_AVDD_0V9(30mA)	0.9
	USB2_AVDD_0V9(5mA)	0.9
	USB3_AVDD_0V9(5mA)	0.9
	MULTI_PHY_AVDD_0V9(150mA)	0.9
	PCIE30_AVDD_0V9(160mA)	0.9
8	PMU_VDD_LOGIC_0V9(50mA)	0.9
	PMUPLL_AVDD_0V9(10mA)	0.9
9	VCCIO1	3.3
10	VCCIO3	3.3
11	PMUIO1	3.3
	PMUIO2	3.3
12	SYSPLL_AVDD_1V8(18mA)	1.8
	USB2_AVDD_1V8(30mA)	1.8
	USB3_AVDD_1V8(30mA)	1.8
	MULTI_PHY_AVDD_1V8(21mA)	1.8
	PCIE30_AVDD_1V8(60mA)	1.8
	SARADC_AVDD_1V8(1.5mA)	1.8
13	PMUPLL_AVDD_1V8(9mA)	1.8
14	MIPI_CSI_RX_AVDD_1V8(2.5mA)	1.8
	MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8(15mA)	1.8
	MIPI_DSI_TX1_AVDD_1V8(15mA)	1.8
	EDP_TX_AVDD_1V8(100mA)	1.8
	HDMI_TX_AVDD_1V8(16mA)	1.8
15	USB2_AVDD_3V3(10mA)	3.3
	USB3_AVDD_3V3(10mA)	3.3
	VCCIO5	3.3
	VCCIO7	3.3
16	OTP_VCC18(59mA)	1.8
	VCCIO2	1.8
	VCCIO4	1.8
	VCCIO6	1.8

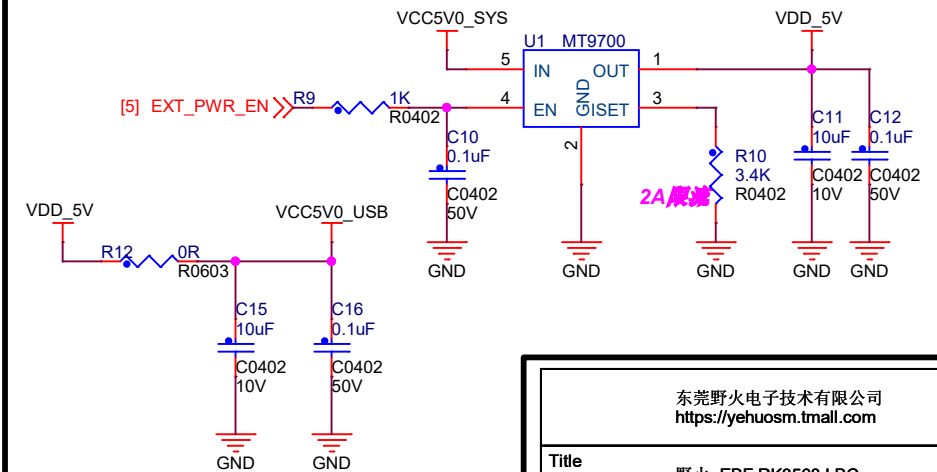
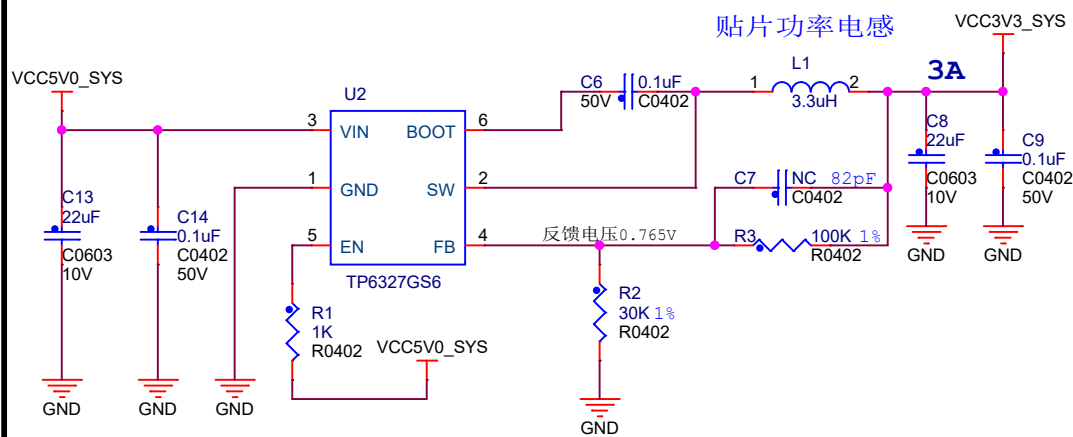
## Power Sequence



# DC IN: 5V



# 5V转3.3V



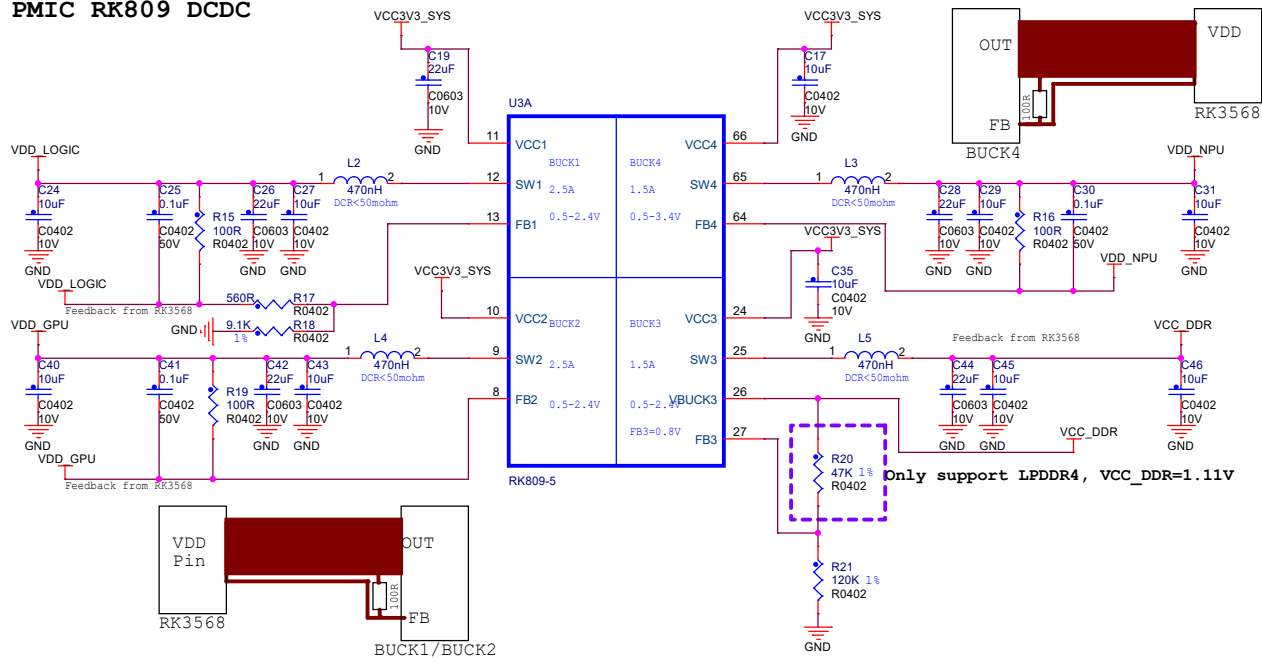
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Title 野火\_EBF RK3568 LBC

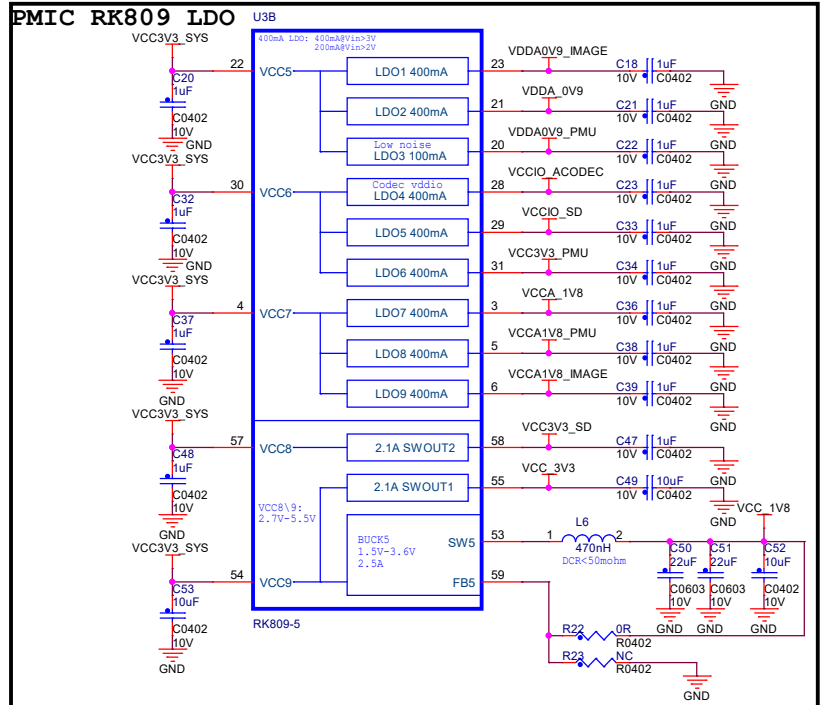
Size A4	Document Number 电源	Rev V1.0
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Date: Monday, December 12, 2022 Sheet 4 of 25

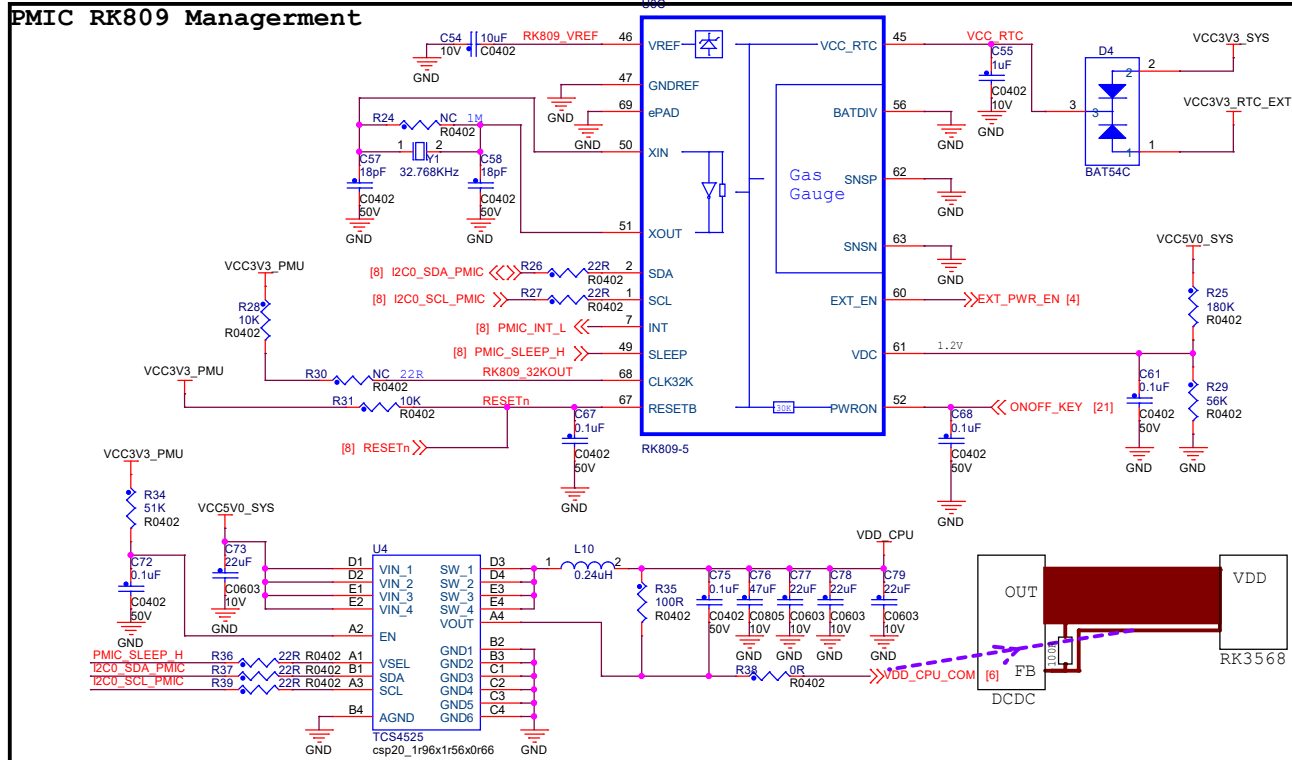
### PMIC RK809 DCDC



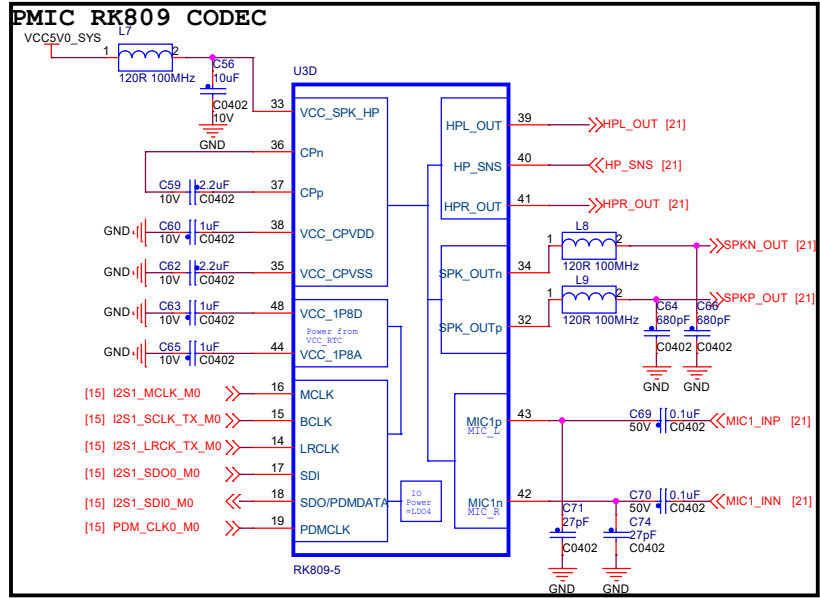
### PMIC RK809 LDO



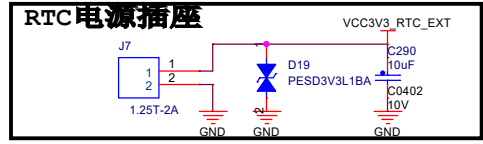
### PMIC RK809 Management



### PMIC RK809 CODEC

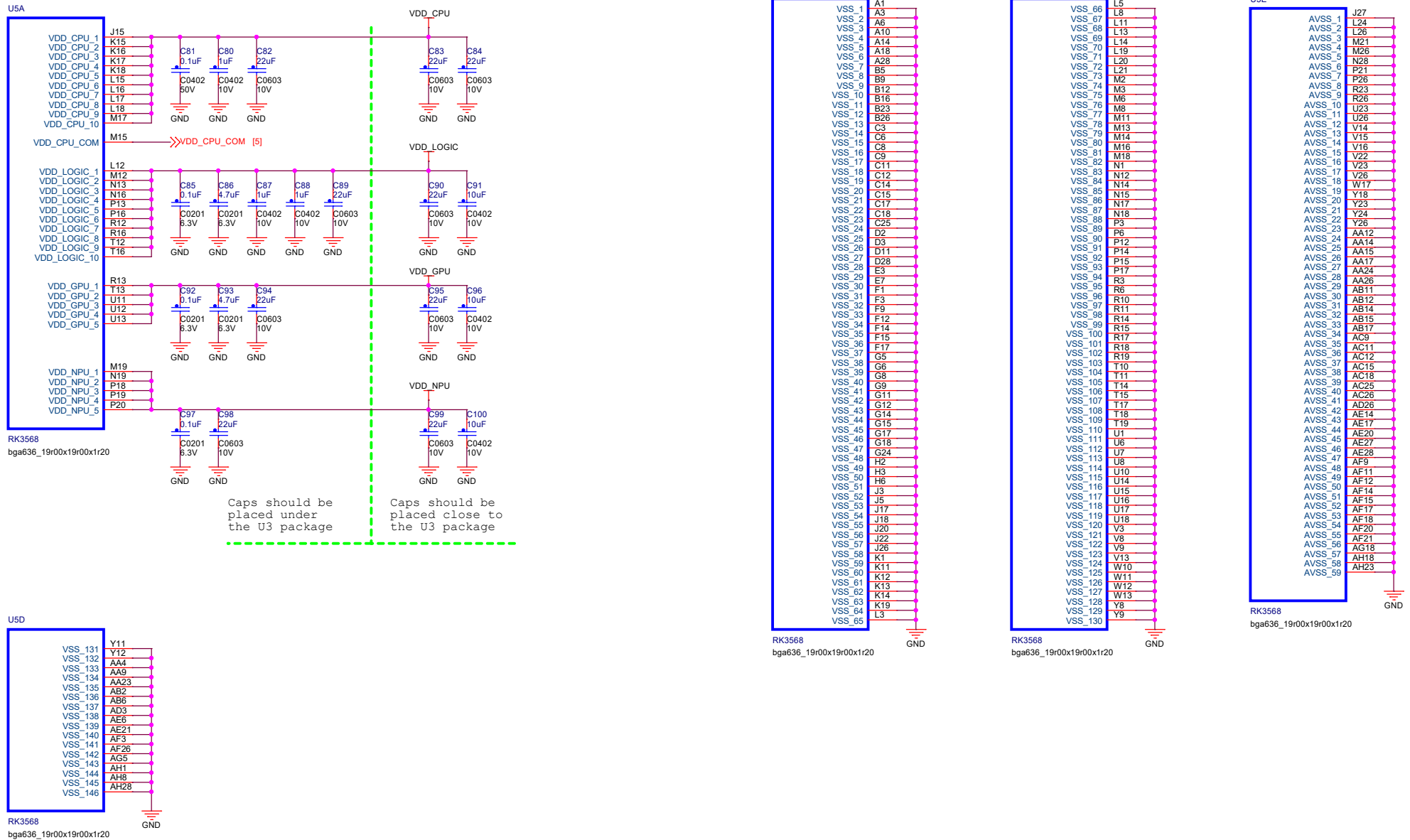


### RTC电源插座



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Title 野火_EBF RK3568 LBC		
Size A3	Document Number SYS PMIC	Rev V1.0
Date: Monday, December 12, 2022 Sheet 5 of 25		

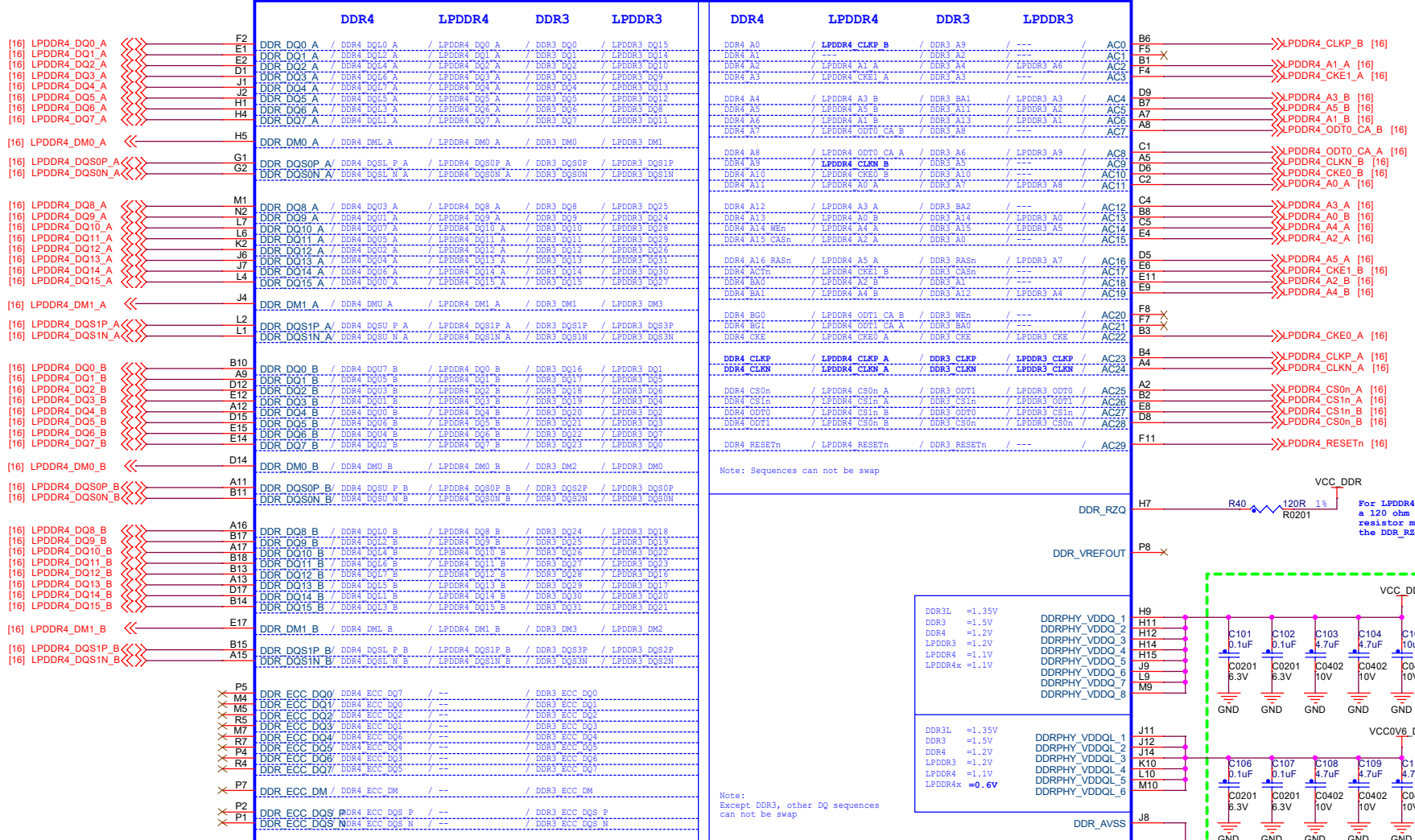
# RK3568 PWR



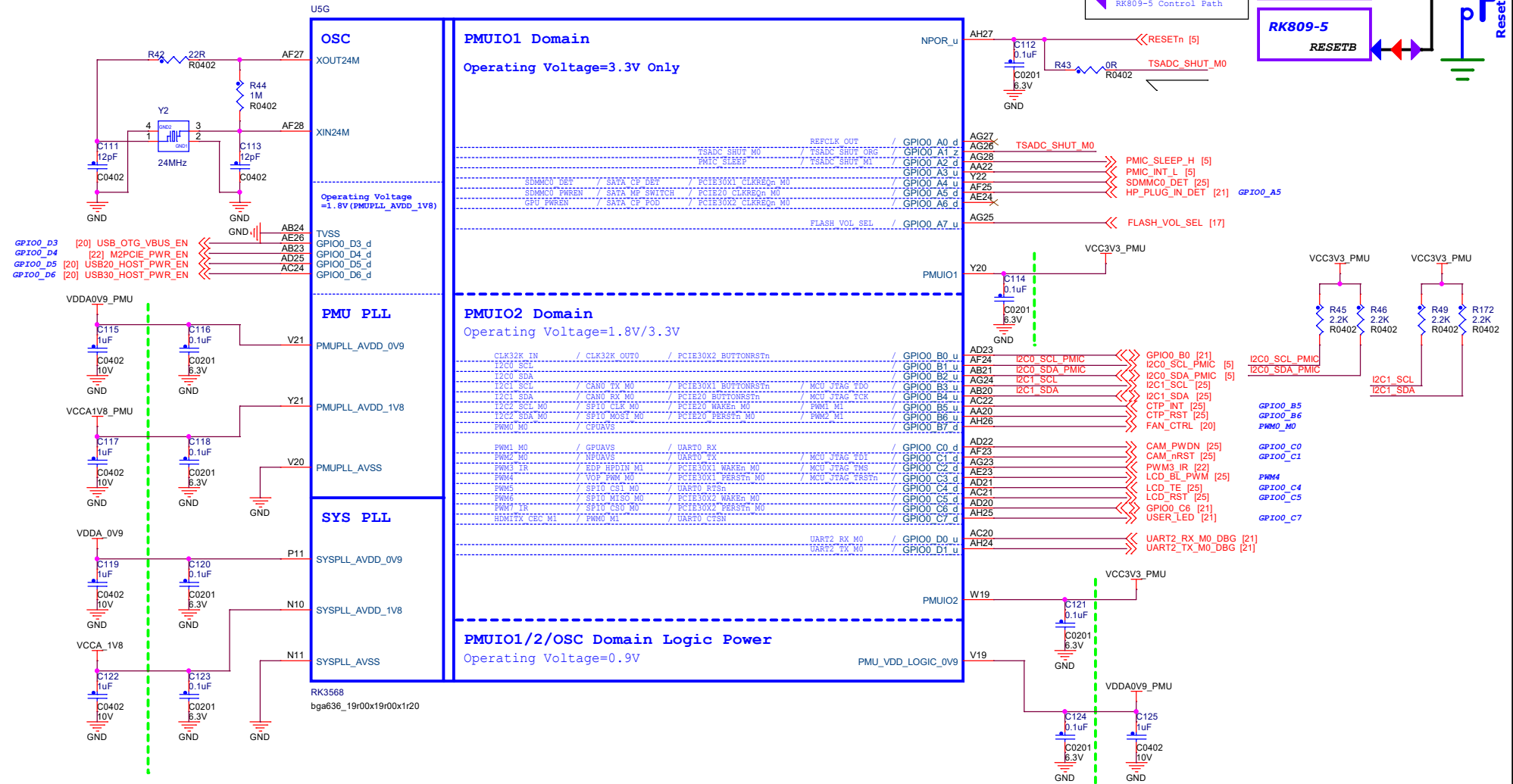
东莞野火电子有限公司 https://yehuosm.taobao.com		
Title 野火_EBF RK3568 LBC		
Size A3	Document Number CPU PWR	Rev V1.0
Date: Monday, December 12, 2022 Sheet 6 of 25		

# RK3568 DDR PHY

USF



# RK3568 OSC/PLL/PMUIO



**Note:**

Caps of between dashed green lines and U3 should be placed under the U3 package. Other caps should be placed close to the U3 package

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Title 野火_EBF RK3568 LBC		
Size A3	Document Number OSC/PLL/PMUIO	Rev V1.0
Date: Monday, December 12, 2022 Sheet 8 of 25		

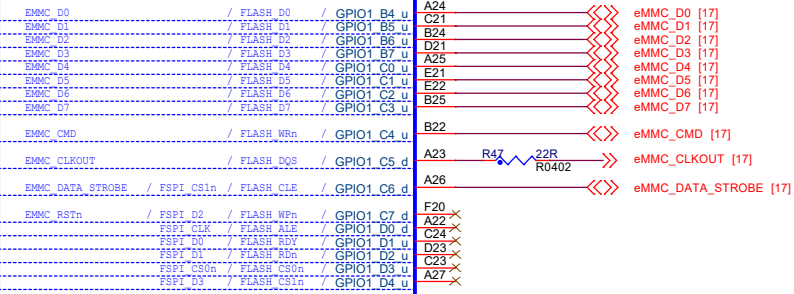


# RK3568 VCCIO2 Domain

U5I

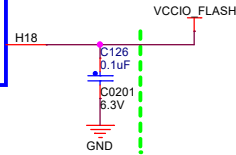
## VCCIO2 Domain

Operating Voltage=1.8V/3.3V



Default is determined by Pin  
FLASH\_VOL\_SEL/GPIO0 A7 u:  
L:VCCIO2 must supply 3.3V  
H:VCCIO2 must supply 1.8V

VCCIO2



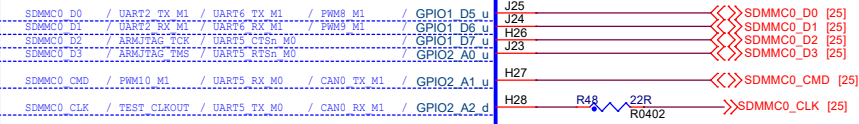
RK3568  
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# RK3568 VCCIO3 Domain

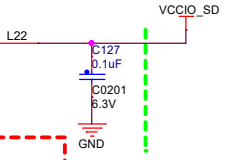
U5J

## VCCIO3 Domain

Operating Voltage=1.8V/3.3V



VCCIO3



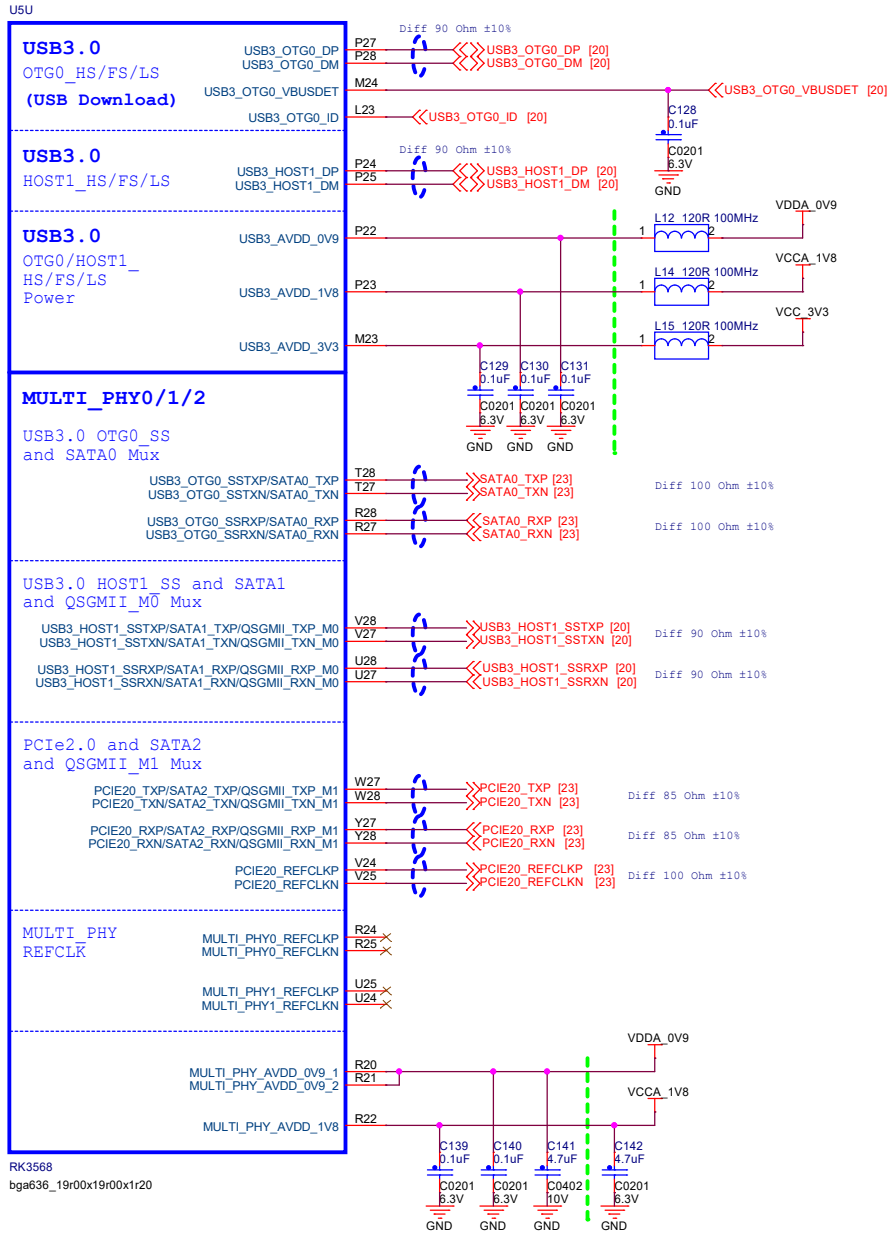
RK3568  
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### Note:

Caps of between dashed green lines and U3 should be placed under the U3 package. Other caps should be placed close to the U3 package

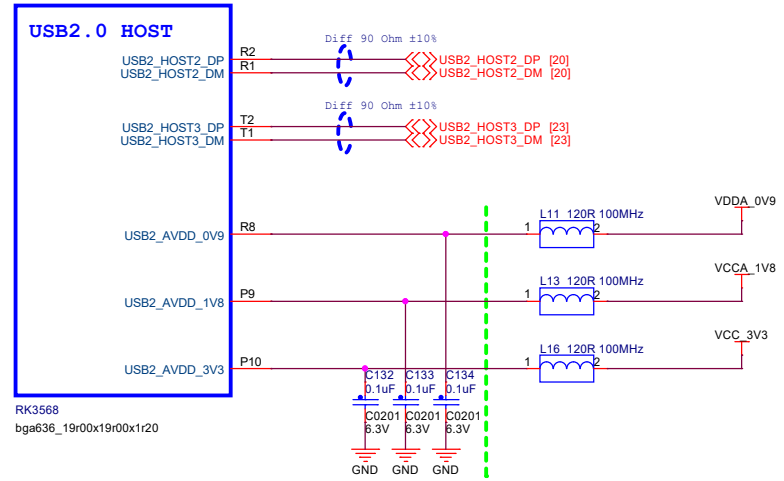
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Title 野火_EBF RK3568 核心板		
Size A3	Document Number SARADC/GPIO	Rev V1.0
Date: Monday, December 12, 2022	Sheet 9	of 25

# RK3568 USB3.0/SATA/QSGMII/PCIe2.0 x1

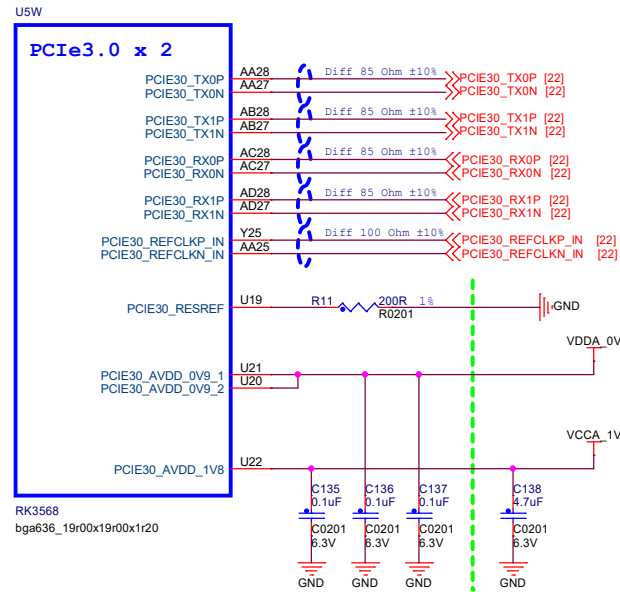


**Note:**  
 Caps of between dashed green lines and U3 should be placed under the U3 package.  
 Other caps should be placed close to the U3 package

# RK3568 USB2.0 HOST



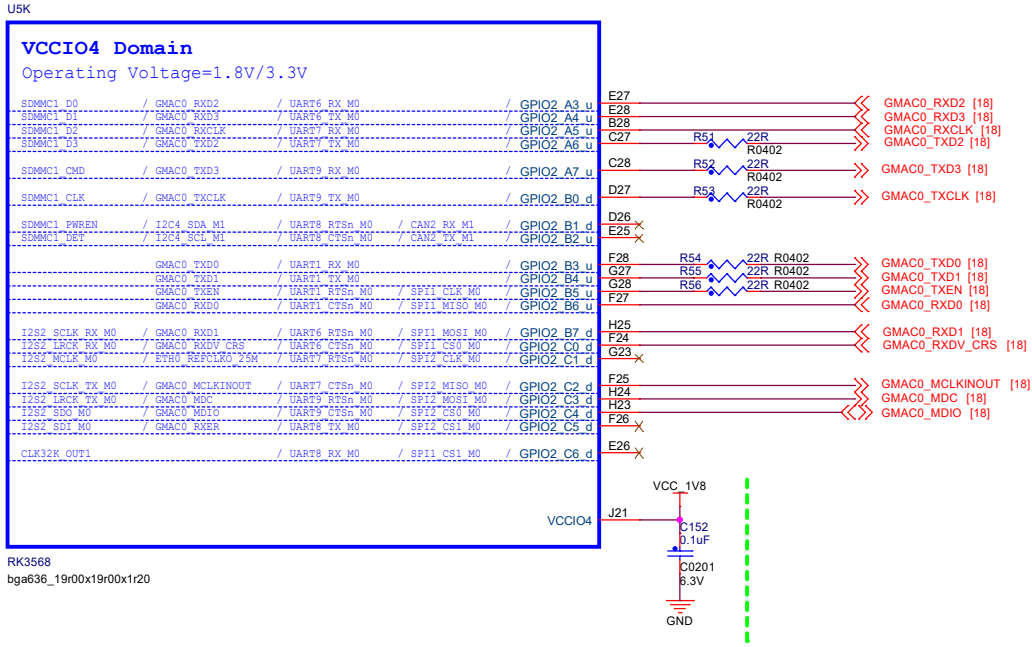
# RK3568 PCIe3.0 x2



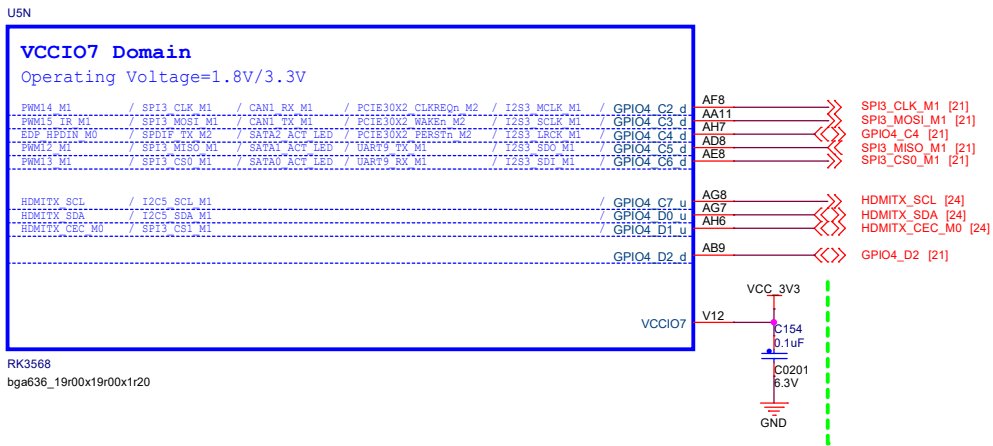
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Title 野火_EBF RK3568 LBC		
Size A3	Document Number USB/PCIe/STAT PHY	Rev V1.0
Date: Monday, December 12, 2022 Sheet 10 of 25		

# RK3568 VCCIO4 Domain

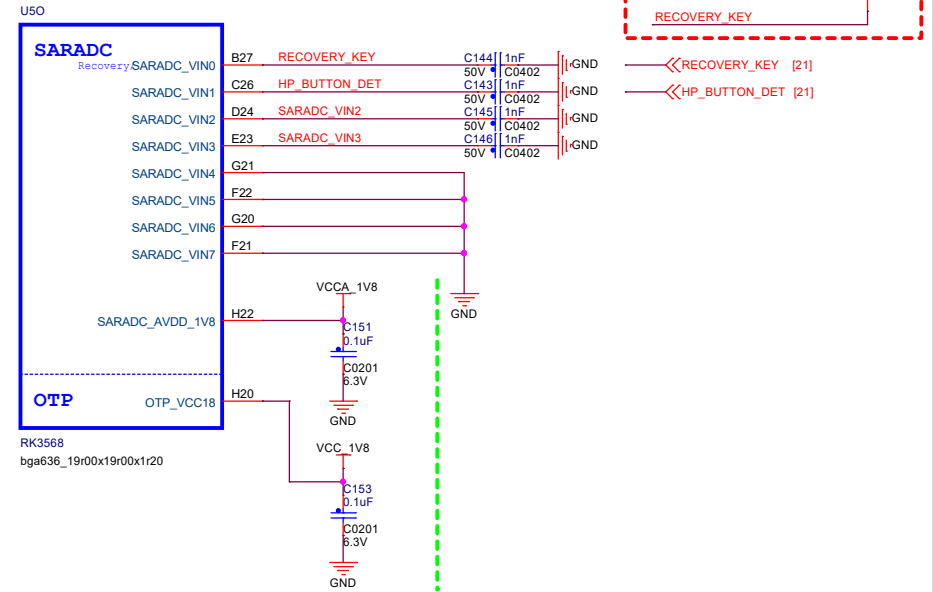


# RK3568 VCCIO7 Domain

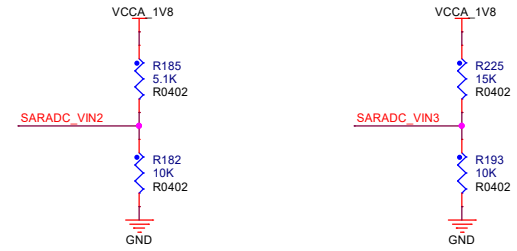


**Note:**  
Caps of between dashed green lines and U3 should be placed under the U3 package.  
Other caps should be placed close to the U3 package

# RK3568 SARADC/OTP



**Note:**  
Must be mounted  
RECOVERY KEY



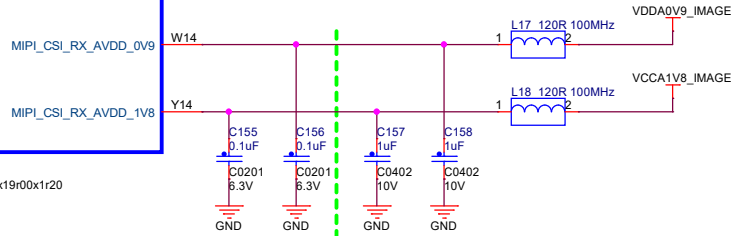
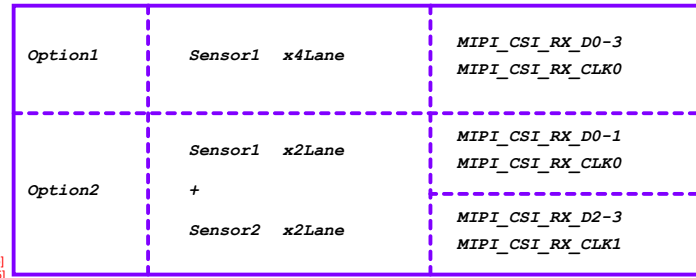
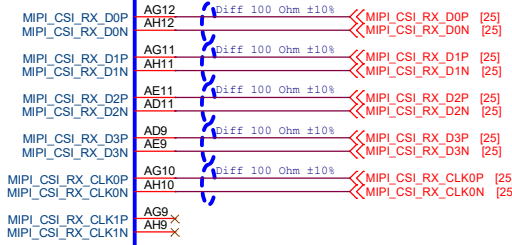
Board ID:05.1 电压: VIN2:1.192V VIN3:0.3V ADC: VIN2:678 VIN3:170

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Title 野火_EBF RK3568 LBC		
Size A3	Document Number SARADC/GPIO	Rev V1.0
Date: Monday, December 12, 2022 Sheet 11 of 25		

# RK3568 MIPI\_CSI\_RX

USP

## MIPI CSI RX



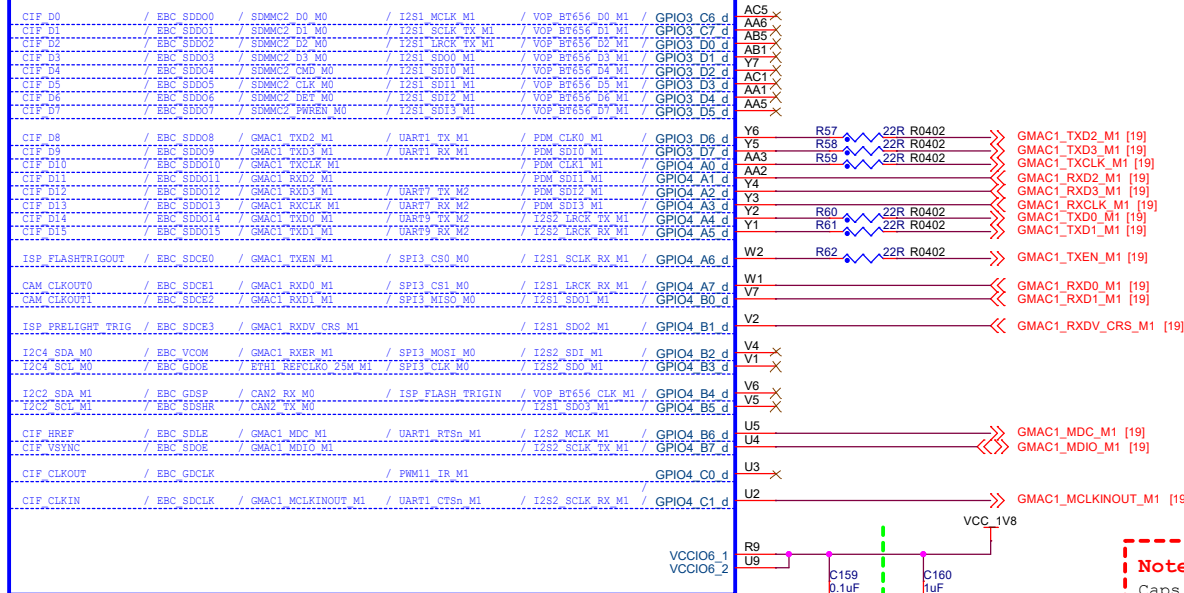
RK3568  
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# RK3568 VCCIO6 Domain

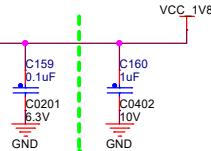
USM

## VCCIO6 Domain

Operating Voltage=1.8V/3.3V



RK3568  
bga636\_19r00x19r00x1r20



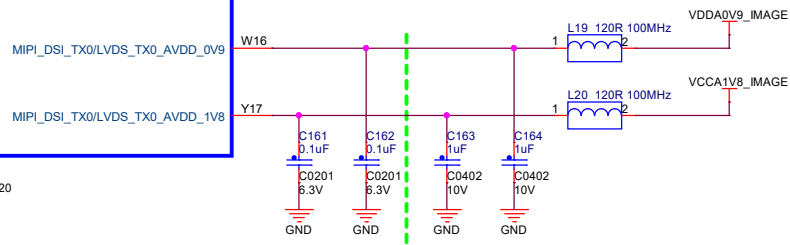
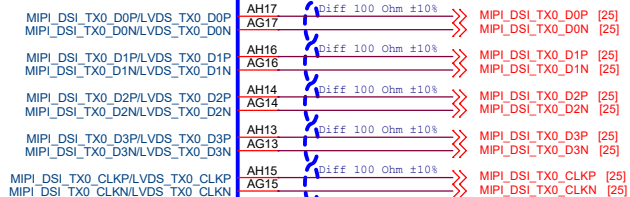
**Note:**  
Caps of between dashed green lines and U3 should be placed under the U3 package. Other caps should be placed close to the U3 package

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Title 野火_EBF RK3568 LBC		
Size A3	Document Number VI Interface	Rev V1.0
Date: Monday, December 12, 2022 Sheet 12 of 25		

# RK3568 MIPI\_DSI\_TX0/LVDS\_TX0

U5R

## MIPI DSI TX0/LVDS TX0

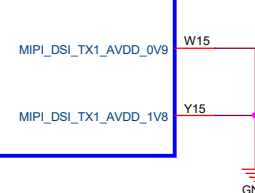
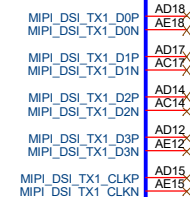


RK3568  
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# RK3568 MIPI\_DSI\_TX1

U5S

## MIPI DSI TX1

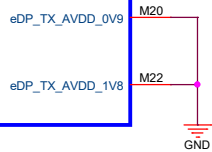
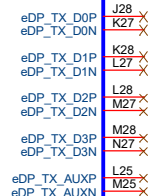


RK3568  
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# RK3568 eDP TX

U5T

## eDP\_TX

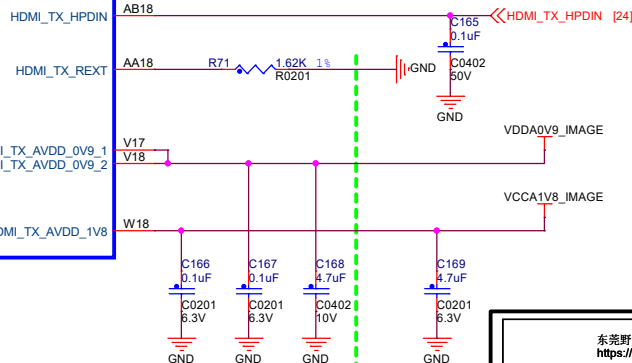
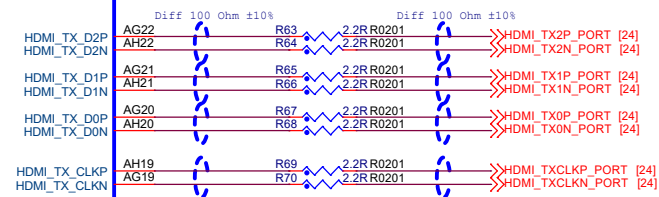


RK3568  
bga636\_19r00x19r00x1r20

# RK3568 HDMI2.0 TX

U5Q

## HDMI2.0 TX



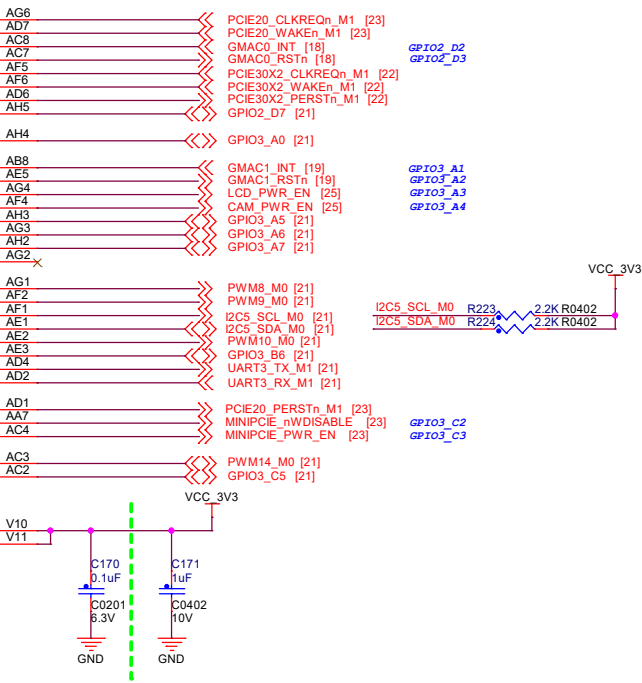
RK3568  
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Title 野火_EBF RK3568 LBC		
Size A3	Document Number VO Interface_1	Rev V1.0
Date: Monday, December 12, 2022 Sheet 13 of 25		

# RK3568 VCCIO5 Domain

USL

VCCIO5 Domain									
Operating Voltage=1.8V/3.3V									
LCDC D0	/ VOP BT656 D0 M0	/ SPI0 MISO M1	/ PCIE20 CLKREQn M1	/ I2S1 MCLK M2	/ GPIO2 D0 d	AG6	<>	PCIE20_CLKREQn_M1 [23]	
LCDC D1	/ VOP BT656 D1 M0	/ SPI0 MOSI M1	/ PCIE20 WAKEn M1	/ I2S1 SCLK TX M2	/ GPIO2 D1 d	AD7	<>	PCIE20_WAKEn_M1 [23]	
LCDC D2	/ VOP BT656 D2 M0	/ SPI0 CS0 M1	/ PCIE30X1 CLKREQn M1	/ I2S1 SCLK RX M2	/ GPIO2 D2 d	AC8	<>	GMAC0_INT [18]	GPIO2_D2
LCDC D3	/ VOP BT656 D3 M0	/ SPI0 CLK M1	/ PCIE30X1 WAKEn M1	/ I2S1 SD10 M2	/ GPIO2 D3 d	AF7	<>	GMAC0_RSTn [18]	GPIO2_D3
LCDC D4	/ VOP BT656 D4 M0	/ SPI2 CS1 M1	/ PCIE30X2 CLKREQn M1	/ I2S1 SD11 M2	/ GPIO2 D4 d	AF6	<>	PCIE30X2_CLKREQn_M1 [22]	GPIO2_D4
LCDC D5	/ VOP BT656 D5 M0	/ SPI2 CS0 M1	/ PCIE30X2 WAKEn M1	/ I2S1 SD12 M2	/ GPIO2 D5 d	AD6	<>	PCIE30X2_WAKEn_M1 [22]	GPIO2_D5
LCDC D6	/ VOP BT656 D6 M0	/ SPI2 MOSI M1	/ PCIE30X2 PERSTn M1	/ I2S1 SD13 M2	/ GPIO2 D6 d	AH5	<>	PCIE30X2_PERSTn_M1 [22]	GPIO2_D6
LCDC D7	/ VOP BT656 D7 M0	/ SPI2 MISO M1	/ UART9 TX M1	/ I2S1 SD00 M2	/ GPIO2 D7 d	AH5	<>	GPIO2_D7 [21]	GPIO2_D7
LCDC CLK	/ VOP BT656 CLK M0	/ SPI2 CLK M1	/ UART9 RX M1	/ I2S1 SD01 M2	/ GPIO3 A0 d	AH4	<>	GPIO3_A0 [21]	GPIO3_A0_d
LCDC D8	/ VOP BT1120 D0	/ SPI1 CS0 M1	/ PCIE30X1 PERSTn M1	/ SDMMC2 D0 M1	/ GPIO3 A1 d	AB8	<>	GMAC1_INT [19]	GPIO3_A1
LCDC D9	/ VOP BT1120 D1	/ GMAC1 RXD2 M0	/ I2S3 MCLK M0	/ SDMMC2 D1 M1	/ GPIO3 A2 d	AE5	<>	GMAC1_RSTn [19]	GPIO3_A2
LCDC D10	/ VOP BT1120 D2	/ GMAC1 RXD3 M0	/ I2S3 SCLK M0	/ SDMMC2 D2 M1	/ GPIO3 A3 d	AG4	<>	LCD_PWR_EN [25]	GPIO3_A3
LCDC D11	/ VOP BT1120 D3	/ GMAC1 RXD2 M0	/ I2S3 SCLK M0	/ SDMMC2 D3 M1	/ GPIO3 A4 d	AF4	<>	CAM_PWR_EN [25]	GPIO3_A4
LCDC D12	/ VOP BT1120 D4	/ GMAC1 RXD3 M0	/ I2S3 CS0 M0	/ SDMMC2 D4 M1	/ GPIO3 A5 d	AH3	<>	GPIO3_A5 [21]	GPIO3_A5
LCDC D13	/ VOP BT1120 D5	/ GMAC1 RXD4 M0	/ I2S3 CS1 M0	/ SDMMC2 D5 M1	/ GPIO3 A6 d	AG3	<>	GPIO3_A6 [21]	GPIO3_A6
LCDC D14	/ VOP BT1120 D6	/ GMAC1 RXD4 M0	/ I2S3 CS1 M0	/ SDMMC2 D6 M1	/ GPIO3 A7 d	AH2	<>	GPIO3_A7 [21]	GPIO3_A7
LCDC D15	/ VOP BT1120 D6	/ ETH1 REPEATER 25M M0		/ SDMMC2 PWREN M1	/ GPIO3 B0 d	AG2	<>		GPIO3_B0_d
LCDC D16	/ VOP BT1120 D7	/ GMAC1 RXD0 M0	/ UART4 RX M1	/ PWM8 M0	/ GPIO3 B1 d	AG1	<>	PWM8_M0 [21]	GPIO3_B1_d
LCDC D17	/ VOP BT1120 D8	/ GMAC1 RXD1 M0	/ UART4 TX M1	/ PWM9 M0	/ GPIO3 B2 d	AF2	<>	PWM9_M0 [21]	GPIO3_B2_d
LCDC D18	/ VOP BT1120 D9	/ GMAC1 RXD0 CRS M0	/ I2S3 SCL M0	/ PWM SD10 M2	/ GPIO3 B3 d	AE1	<>	I2C5_SCL_M0 [21]	GPIO3_B3_d
LCDC D19	/ VOP BT1120 D10	/ GMAC1 RXD1 M0	/ I2S3 SDA M0	/ PWM SD11 M2	/ GPIO3 B4 d	AE1	<>	I2C5_SDA_M0 [21]	GPIO3_B4_d
LCDC D20	/ VOP BT1120 D11	/ GMAC1 RXD0 M0	/ I2S3 SCL M1	/ PWM10 M0	/ GPIO3 B5 d	AE2	<>	PWM10_M0 [21]	GPIO3_B5_d
LCDC D21	/ VOP BT1120 D12	/ GMAC1 RXD1 M0	/ I2S3 SDA M1	/ PWM11 IR M0	/ GPIO3 B6 d	AE3	<>	GPIO3_B6 [21]	GPIO3_B6_d
LCDC D22	/ PWM12 M0	/ GMAC1 TXEN M0	/ UART3 TX M1	/ PDM SD12 M2	/ GPIO3 B7 d	AD2	<>	UART3_TX_M1 [21]	GPIO3_B7_d
LCDC D23	/ PWM13 M0	/ GMAC1 MCLKINOUT M0	/ UART3 RX M1	/ PDM SD13 M2	/ GPIO3 C0 d	AD2	<>	UART3_RX_M1 [21]	GPIO3_C0_d
LCDC HSYNC	/ VOP BT1120 D13	/ SPI1 MOSI M1	/ PCIE20 PERSTn M1	/ I2S1 SD02 M2	/ GPIO3 C1 d	AD1	<>	PCIE20_PERSTn_M1 [23]	GPIO3_C1_d
LCDC VSYNC	/ VOP BT1120 D14	/ SPI1 MISO M1	/ UART5 TX M1	/ I2S1 SD03 M2	/ GPIO3 C2 d	AA7	<>	MINIPcie_nWDISABLE [23]	GPIO3_C2_d
LCDC DEN	/ VOP BT1120 D15	/ SPI1 CLK M1	/ UART5 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C3 d	AC4	<>	MINIPcie_PWR_EN [23]	GPIO3_C3_d
PWM14 M0	/ VOP PWM M1	/ GMAC1 MDC M0	/ UART7 TX M1	/ PDM CLK1 M2	/ GPIO3 C4 d	AC3	<>	PWM14_M0 [21]	GPIO3_C4_d
PWM13 TX M0	/ SP017 TX M1	/ GMAC1 MDC M0	/ UART7 RX M1	/ I2S1 SCLK RX M2	/ GPIO3 C5 d	AC2	<>	GPIO3_C5 [21]	GPIO3_C5_d



RK3568  
bga636\_19r00x19r00x1r20

**Note:**  
Caps of between dashed green lines and U3 should be placed under the U3 package.  
Other caps should be placed close to the U3 package

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Title 野火_EBF RK3568 LBC		
Size A3	Document Number VO Interface_2	Rev V1.0
Date: Monday, December 12, 2022		Sheet 14 of 25

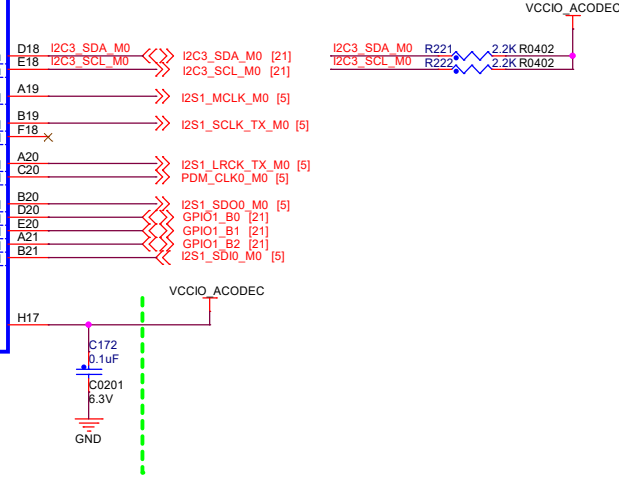
# RK3568 VCCIO1 Domain

USH

## VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERStn_M2		/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK0_M0	/ SPS0IF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATA1	/ GPIO1_A7_d
I2S1_SDI0_M0	/ I2S1_SDI0_M0	/ PDM_SDI0_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATA0	/ GPIO1_B0_d
I2S1_SDO1_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_PERStn_M2		/ GPIO1_B2_d
I2S1_SDI0_M0	/ I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d

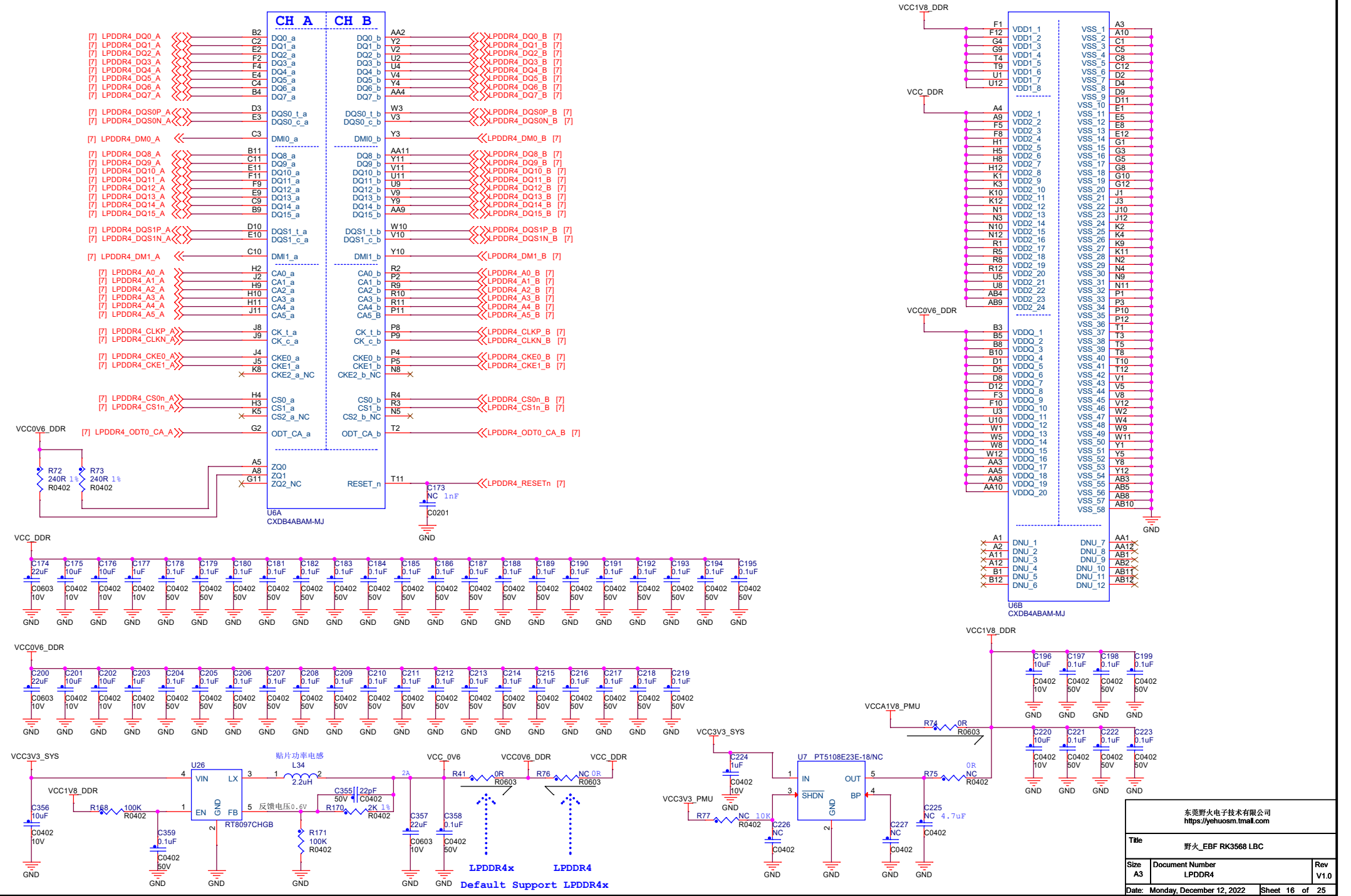


RK3568  
bga636\_19r00x19r00x1r20

**Note:**  
Caps of between dashed green lines and U3 should be placed under the U3 package.  
Other caps should be placed close to the U3 package

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Title 野火_EBF RK3568 核心板		
Size A3	Document Number Audio Interface	Rev V1.0
Date: Monday, December 12, 2022   Sheet 15 of 25		

# LPDDR4/4x

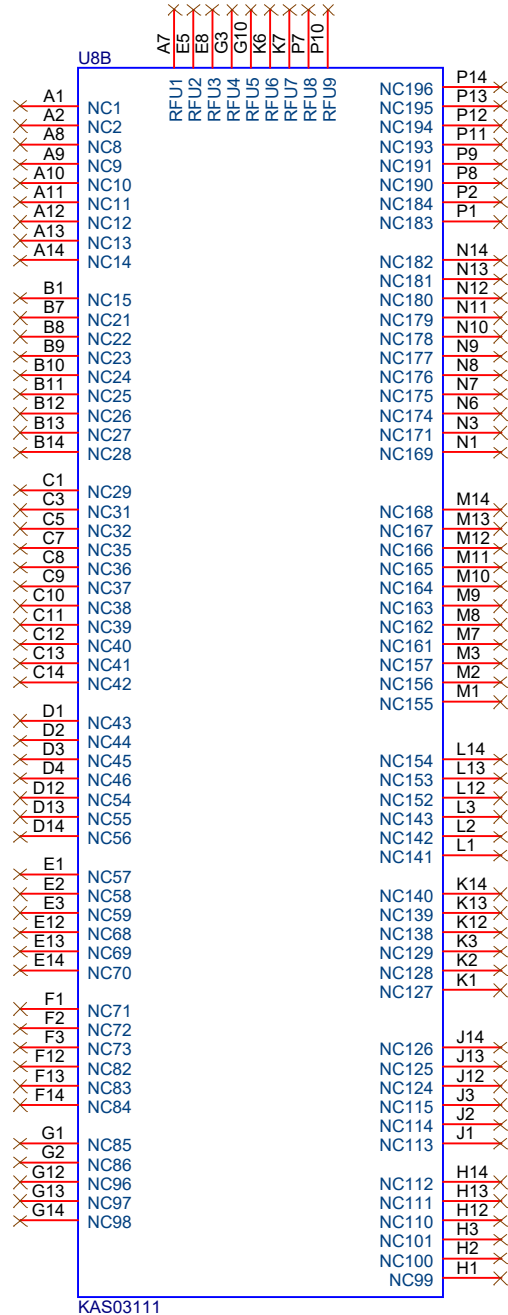


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Title 野火_EBF RK3568 LBC		
Size A3	Document Number LPDDR4	Rev V1.0
Date: Monday, December 12, 2022 Sheet 16 of 25		

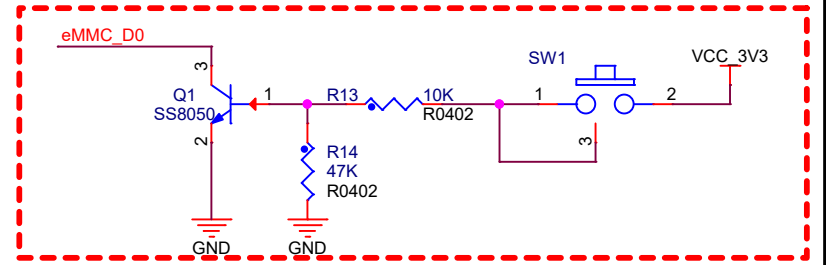
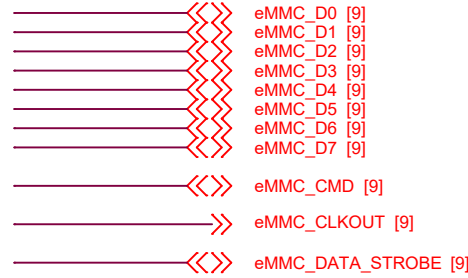
Default Support LPDDR4x



# eMMC Flash

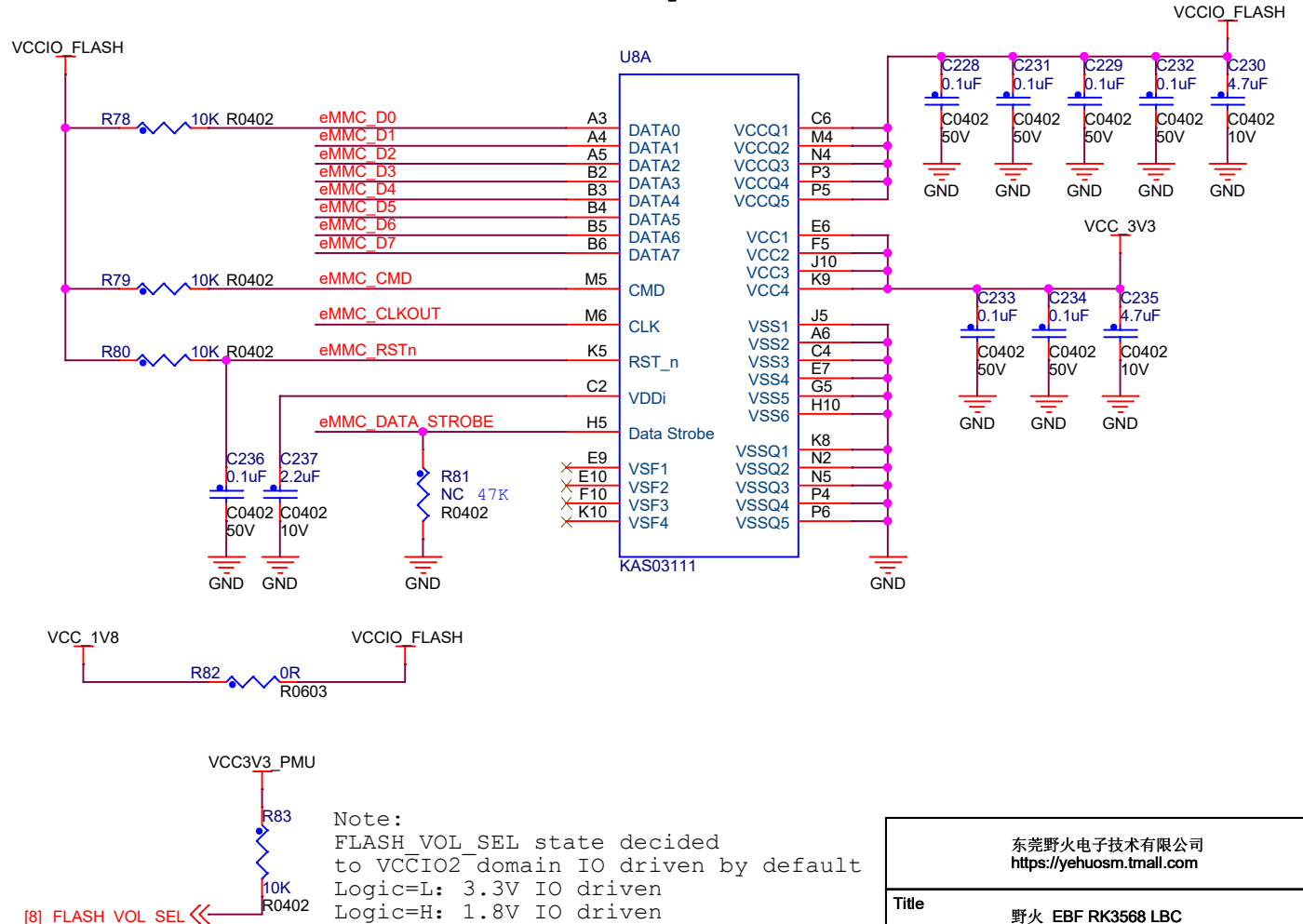


KAS03111



## Note:

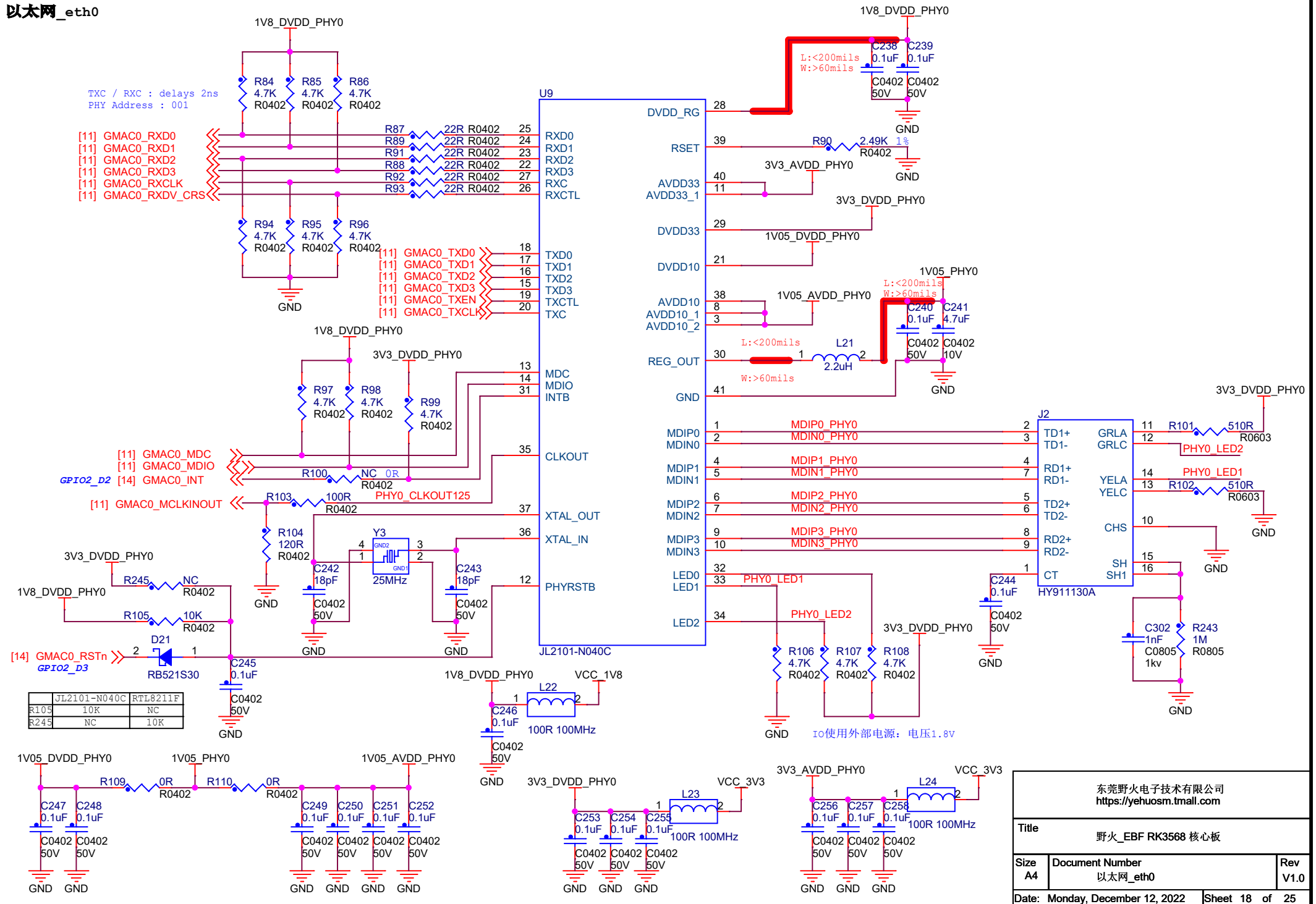
For eMMC or Nand Flash:  
If eMMC\_D0/FLASH\_D0=0V at after power on and reset,  
then system will enter into Maskrom mode.



Note:  
FLASH\_VOL\_SEL state decided  
to VCCIO2 domain IO driven by default  
Logic=L: 3.3V IO driven  
Logic=H: 1.8V IO driven

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Title 野火_EBF RK3568 LBC		
Size A4	Document Number eMMC Flash	Rev V1.0
Date: Monday, December 12, 2022	Sheet 17 of 25	

# 以太网\_eth0



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Title: 野火\_EBF RK3568 核心板

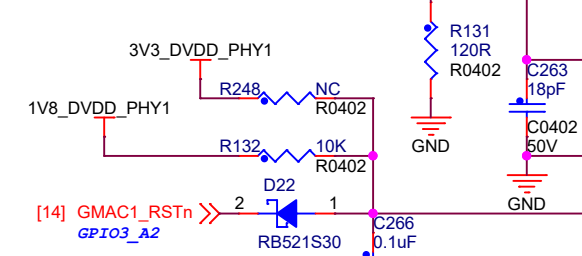
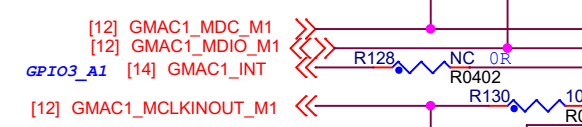
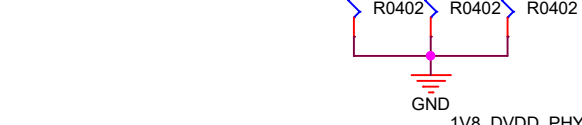
Size: A4	Document Number: 以太网_eth0	Rev: V1.0
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Date: Monday, December 12, 2022 Sheet 18 of 25

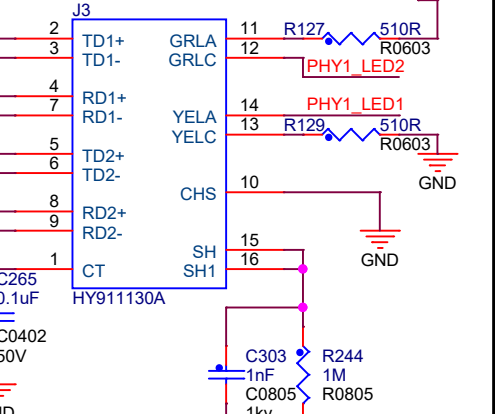
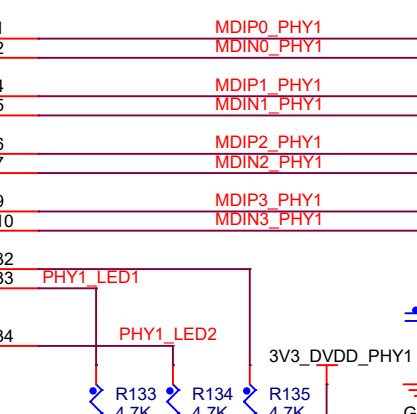
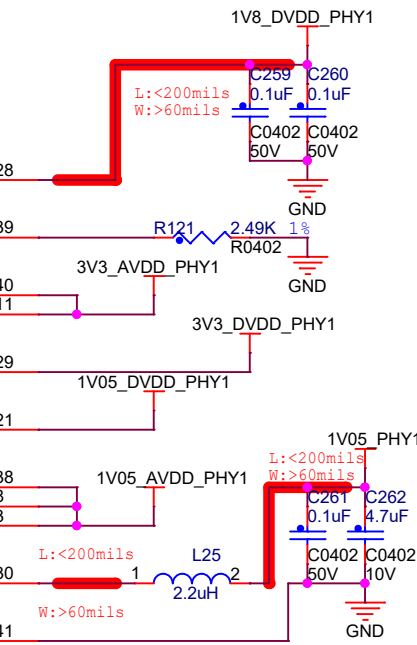
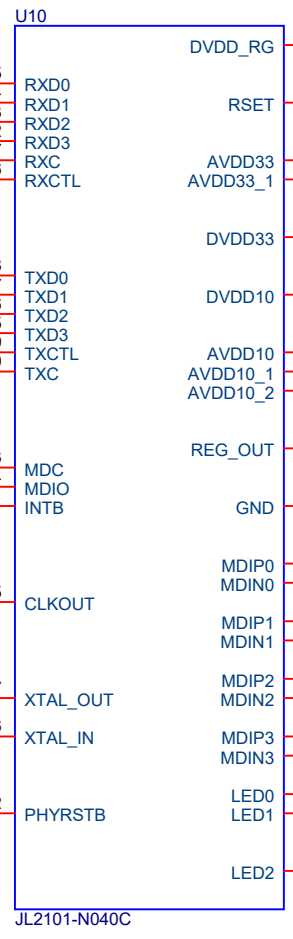
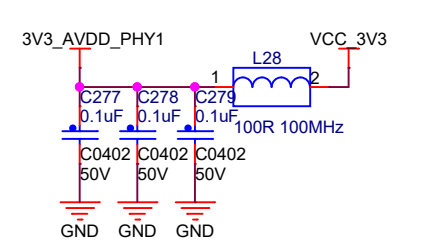
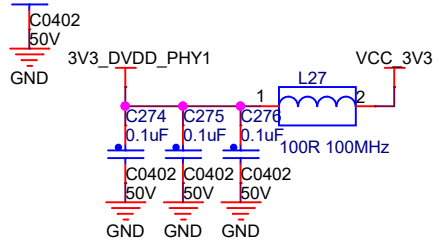
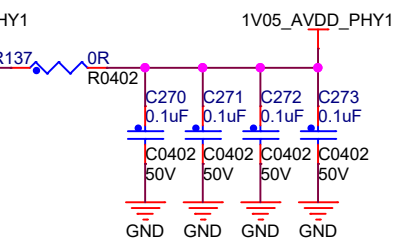
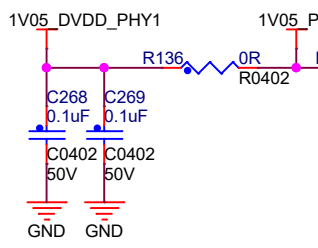
# 以太网\_eth1

TXC / RXC : delays 2ns  
PHY Address : 010

- [12] GMAC1\_RXD0\_M1
- [12] GMAC1\_RXD1\_M1
- [12] GMAC1\_RXD2\_M1
- [12] GMAC1\_RXD3\_M1
- [12] GMAC1\_RXCLK\_M1
- [12] GMAC1\_RXDV\_CRS\_M1



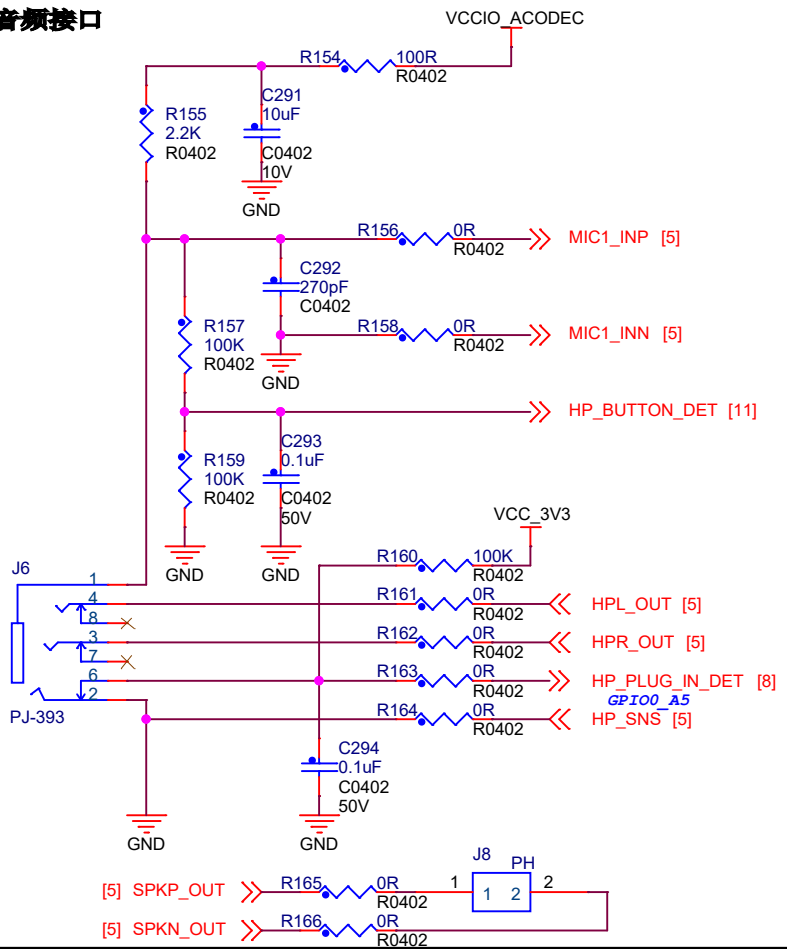
JL2101-N040C		RTL8211F	
R132	10K	NC	10K
R248	NC	NC	10K



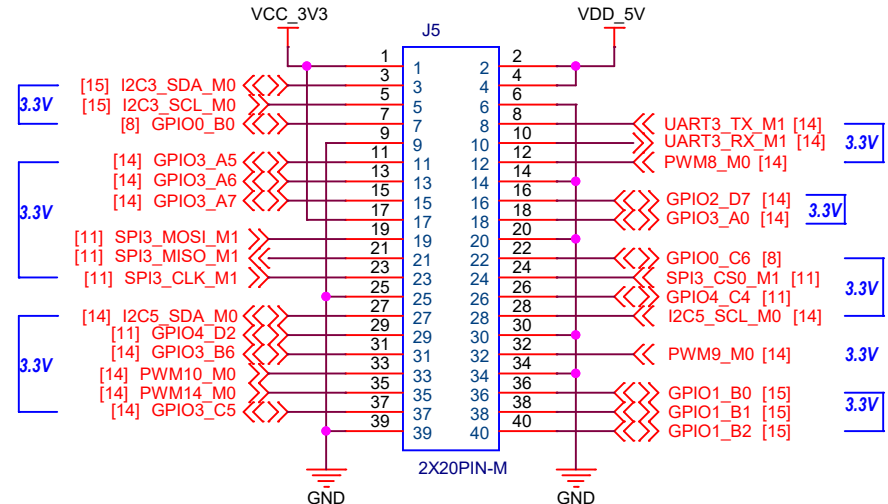
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Title: 野火_EBF RK3568 核心板		
Size: A4	Document Number: 以太网_eth1	Rev: V1.0
Date: Monday, December 12, 2022	Sheet 19 of 25	



### 音频接口

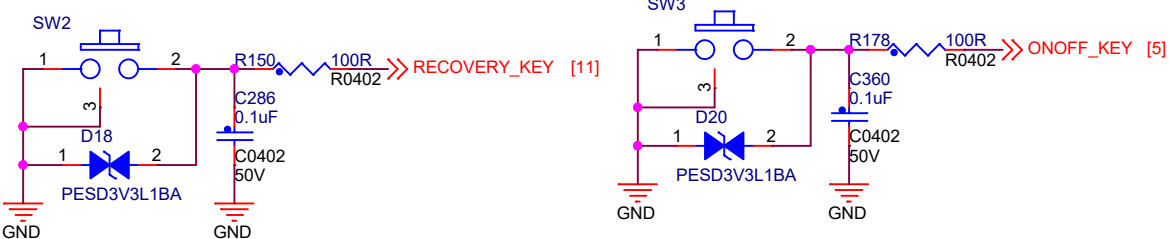


### IO 引出

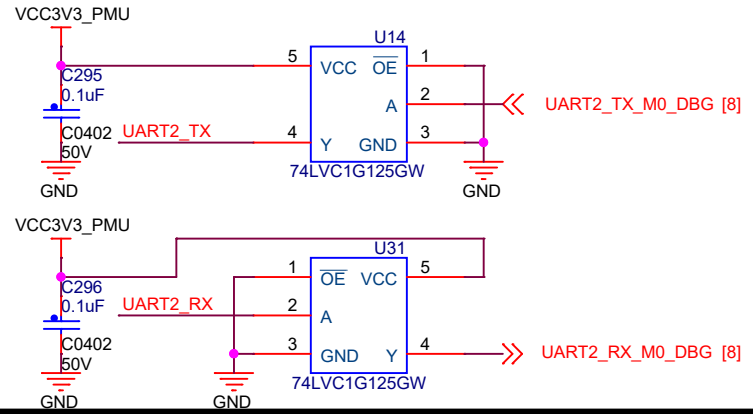
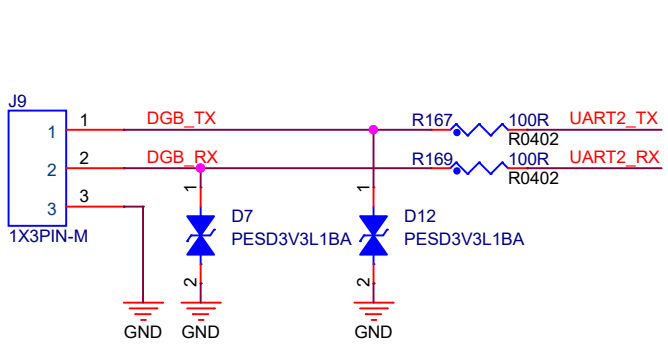


注：所有引出的GPIO只兼容3.3V

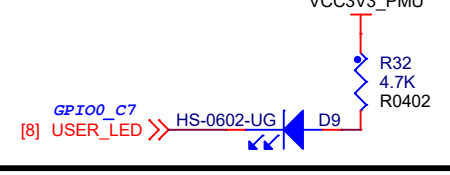
### 按键



### Debug接口

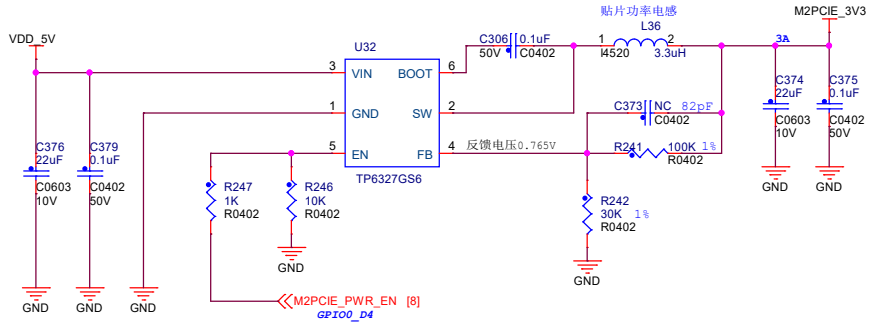


### LED

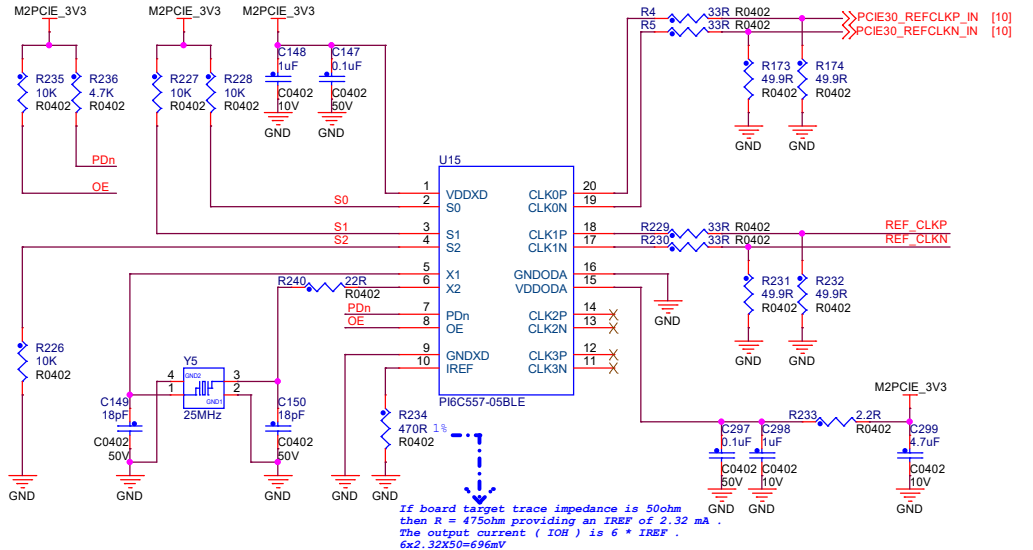


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Title 野火_EBF RK3568 LBC		
Size A4	Document Number 音频DEBUG/IO引出/按键/LED	Rev V1.0
Date: Monday, December 12, 2022	Sheet 21 of 25	

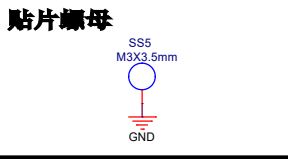
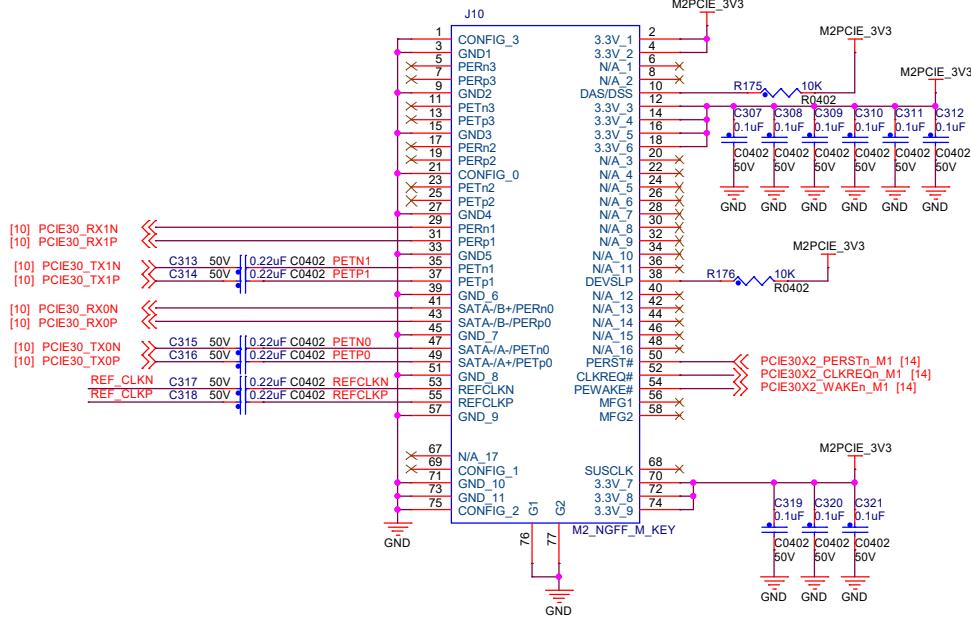
M.2 PCIe POWER 3.3V



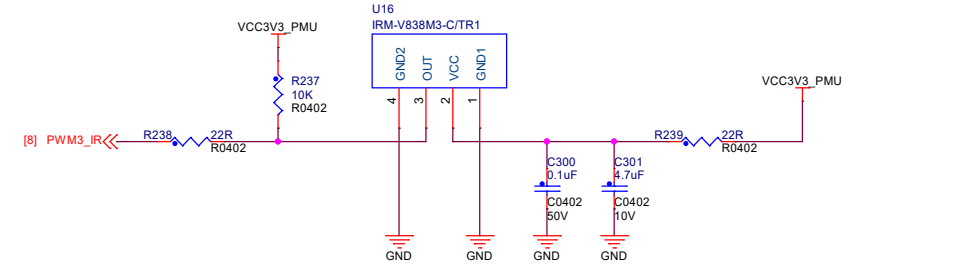
M.2 PCIe REF\_CLKP 100MHz



M.2 PCIe3.0 x 2Lanes

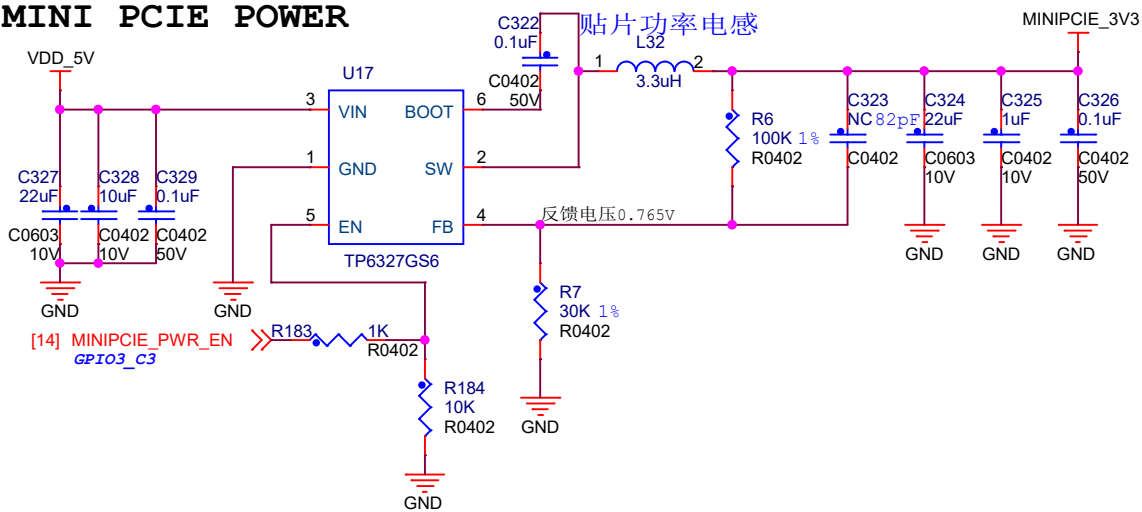


IR 接收器

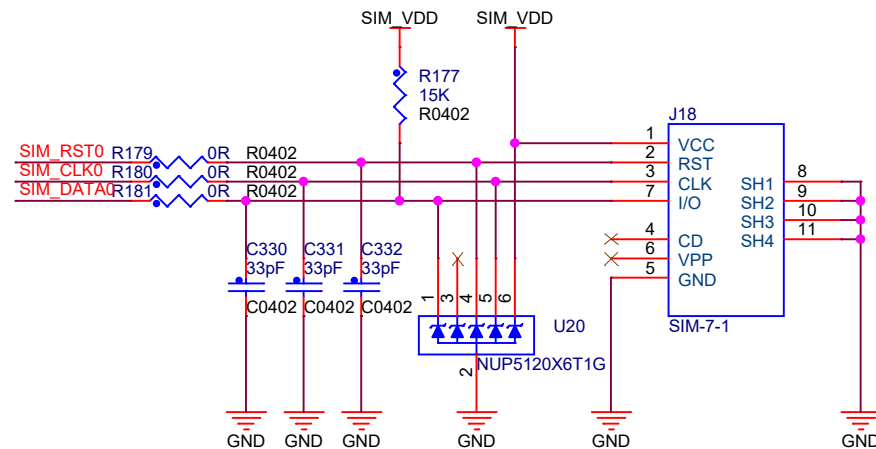


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Title 野火_EBF RK3568 LBC		
Size A3	Document Number M.2 PCIe3.0接口/IR接收器	Rev V1.0
Date: Monday, December 12, 2022	Sheet 22 of 25	

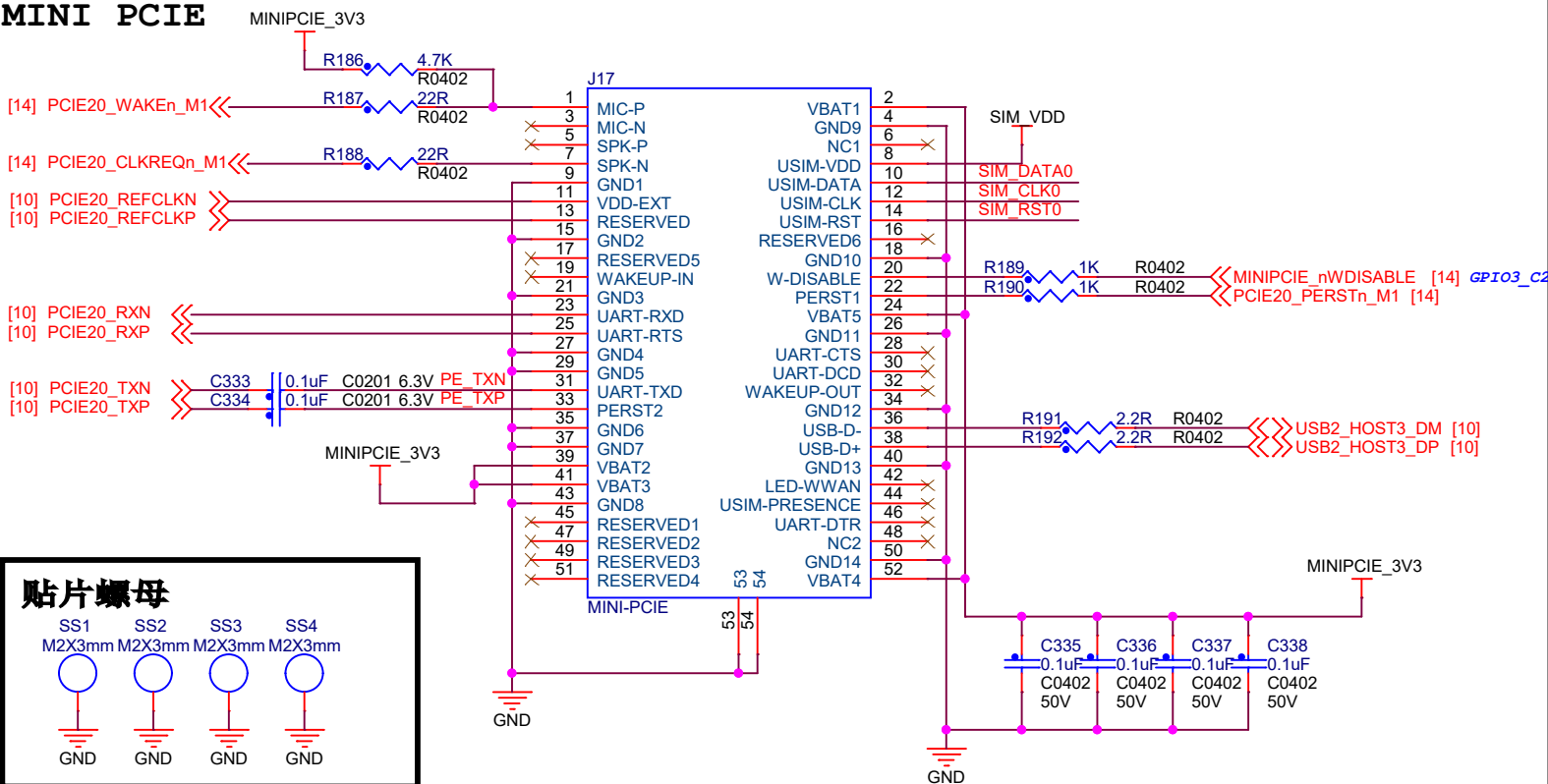
### MINI PCIE POWER



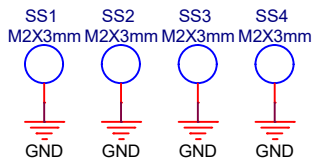
### SIM CARD



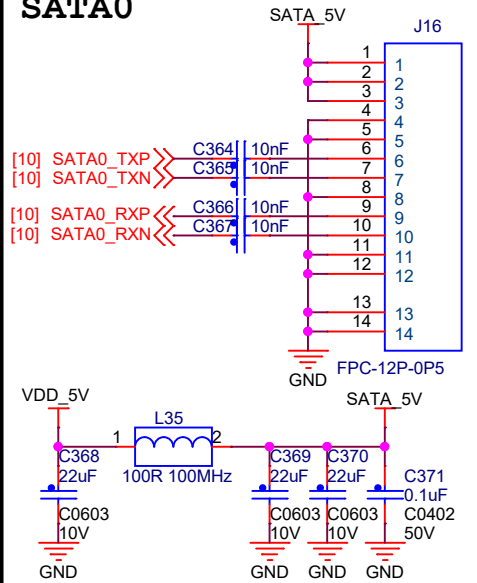
### MINI PCIE



#### 贴片螺母



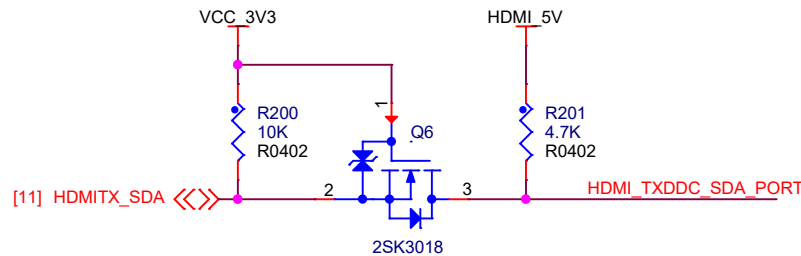
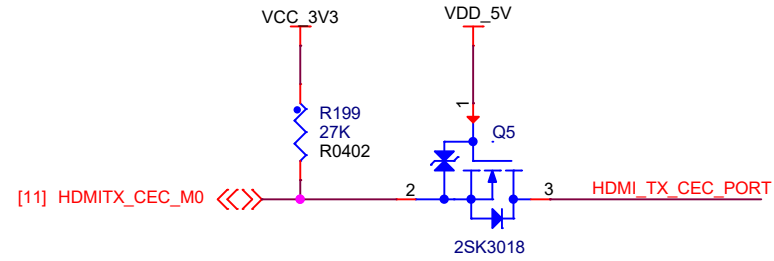
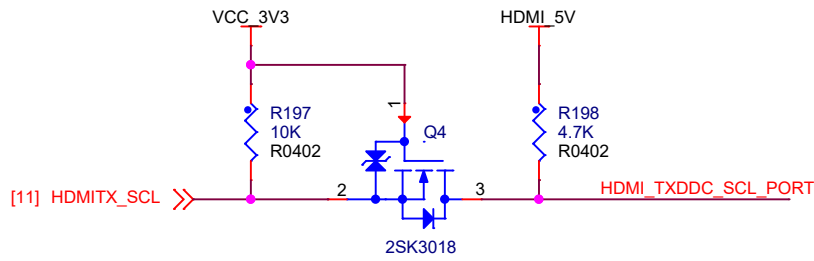
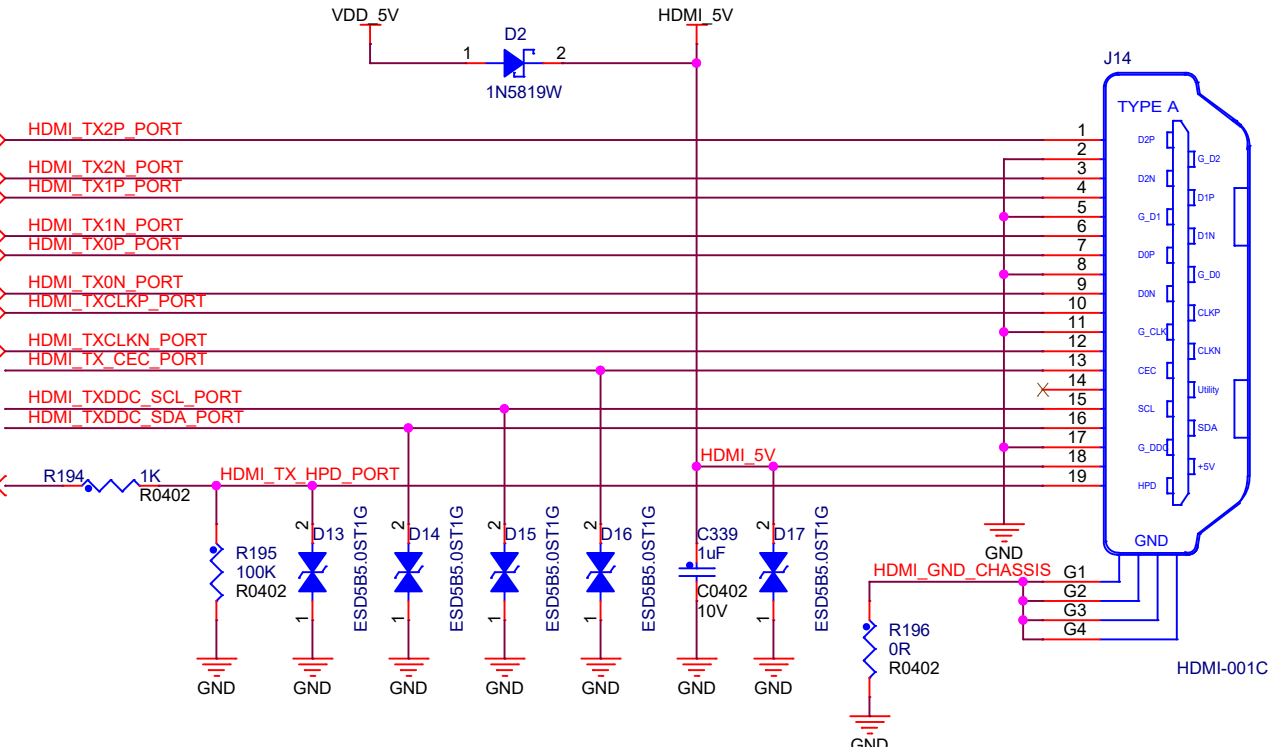
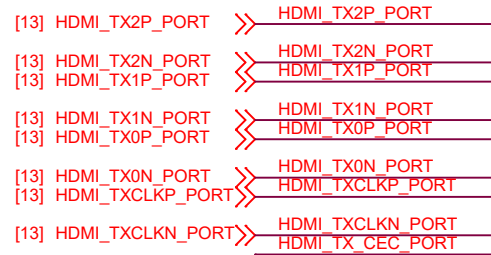
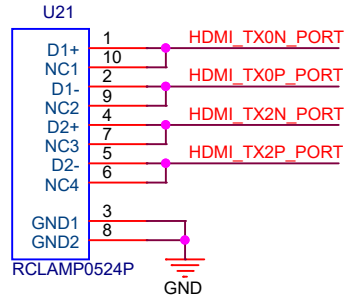
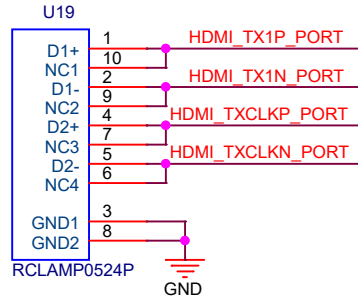
### SATA0



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Title			野火_EBF RK3568 LBC
Size	Document Number	Rev	
A4	M.2 PCIE3.0接口/SATA	V1.0	
Date:	Monday, December 12, 2022	Sheet	23 of 25

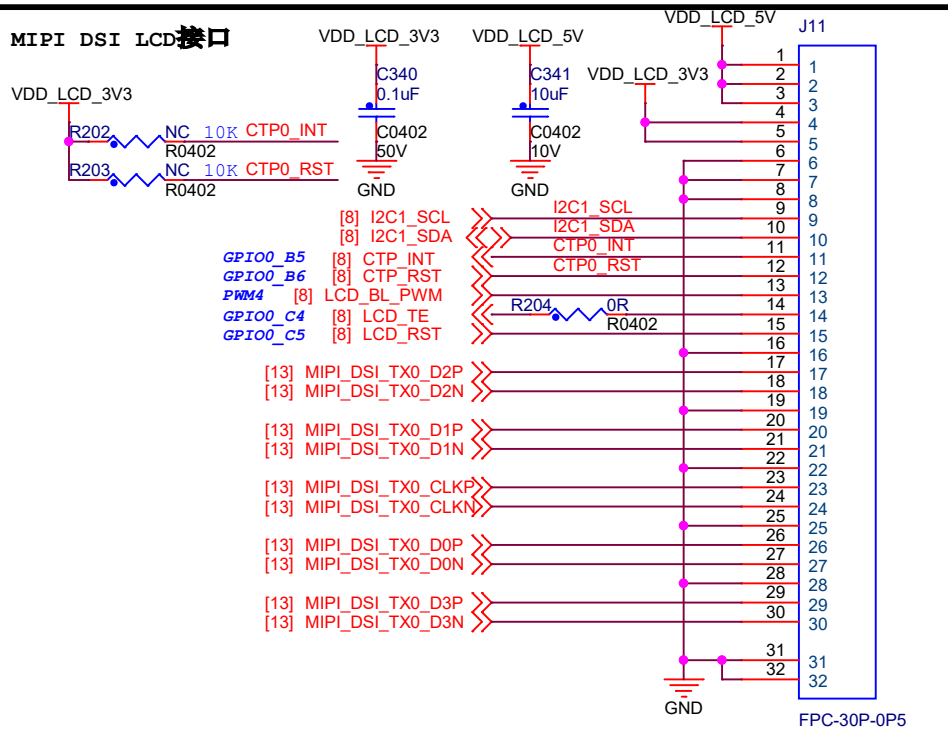
# HDMI 2.0 接口



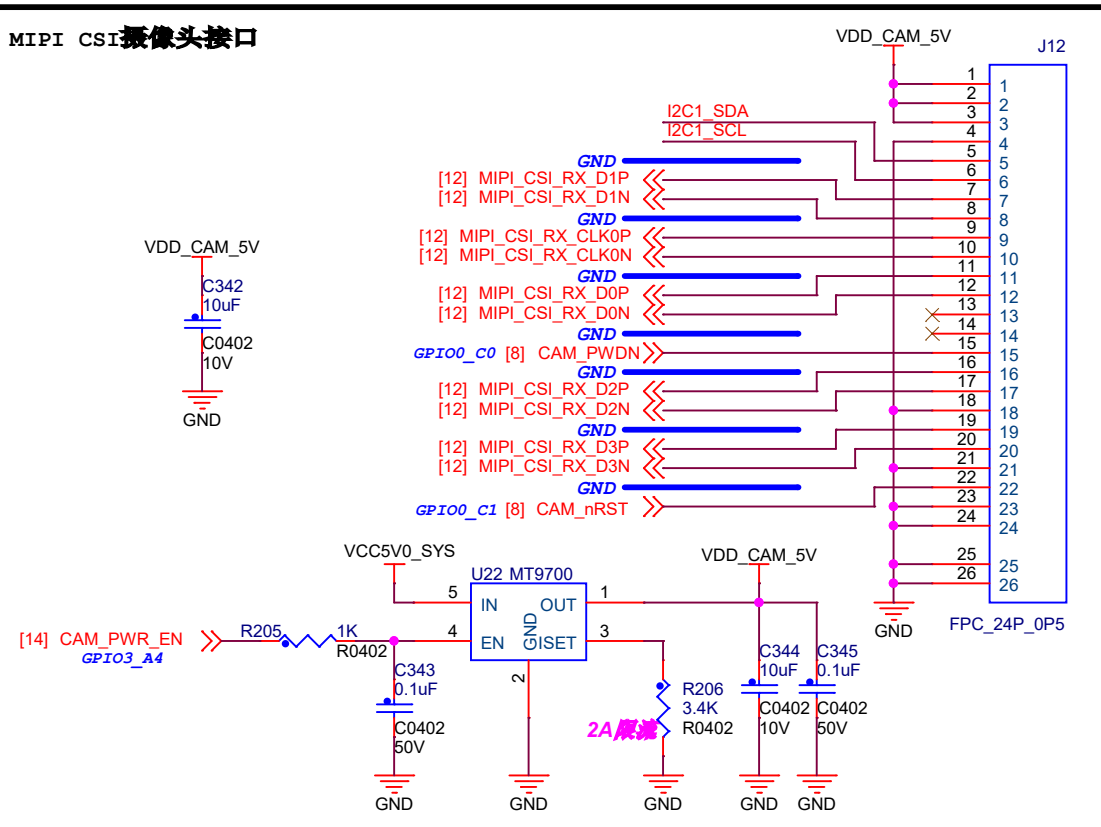
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Title 野火_EBF RK3568 LBC		
Size A4	Document Number M.2 PCIe3.0接口	Rev V1.0
Date: Monday, December 12, 2022	Sheet 24 of 25	



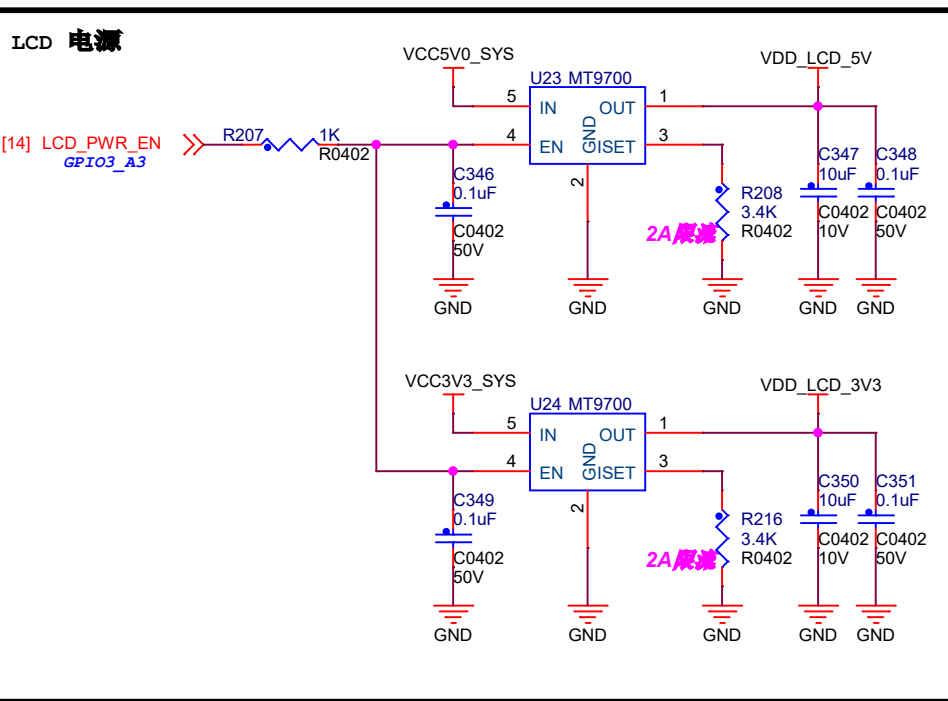
### MIPI DSI LCD接口



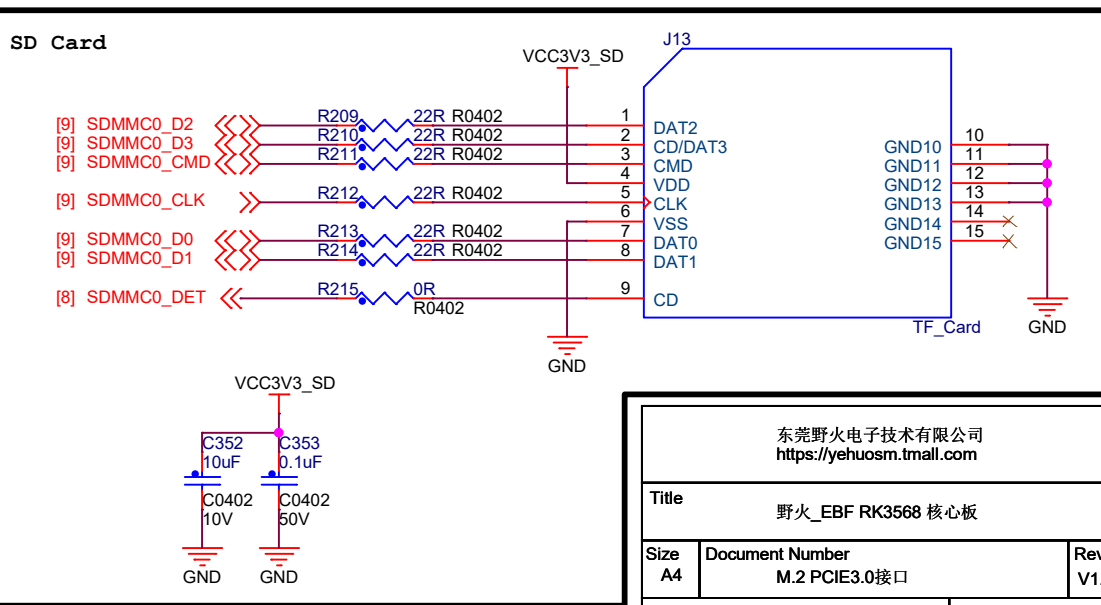
### MIPI CSI摄像头接口



### LCD 电源



### SD Card



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Size A4	Document Number M.2 PCIe3.0接口	Rev V1.0
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Date: Monday, December 12, 2022 Sheet 25 of 25