

野火_RK3566 LubanCat 1 N 原理图_v1.0

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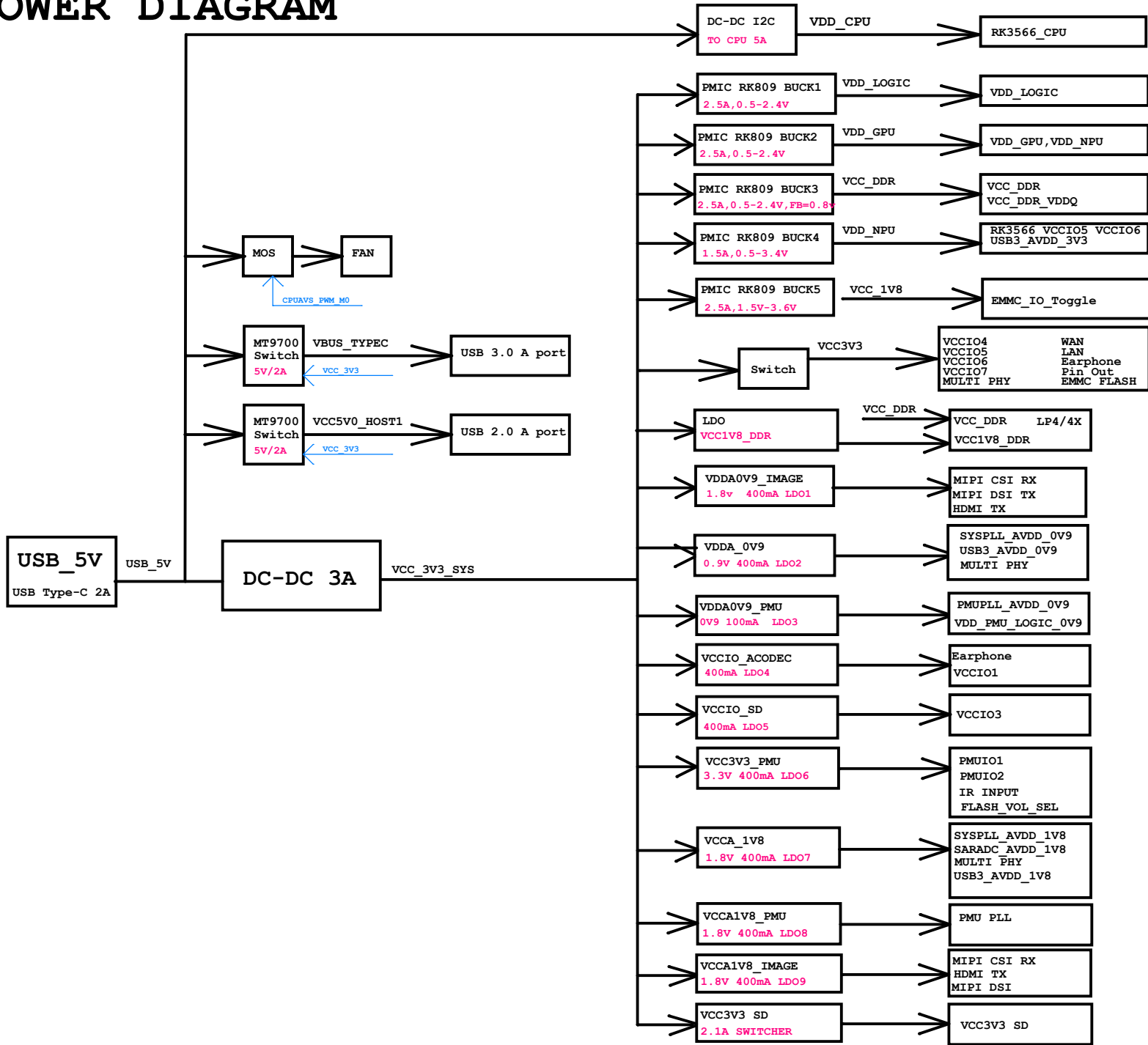
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历史版本

版本号	日期	设计	描述
V0.1	2022-03-18	ghs	初始版本
V0.2	2022-06-24	ghs	修正版本，修正GMAC网口的电压域，同时更换WIFI网卡模块，优化主供电滤波
V1.0	2022-12-12	ghs	修正PHY芯片的RST引脚电平匹配问题

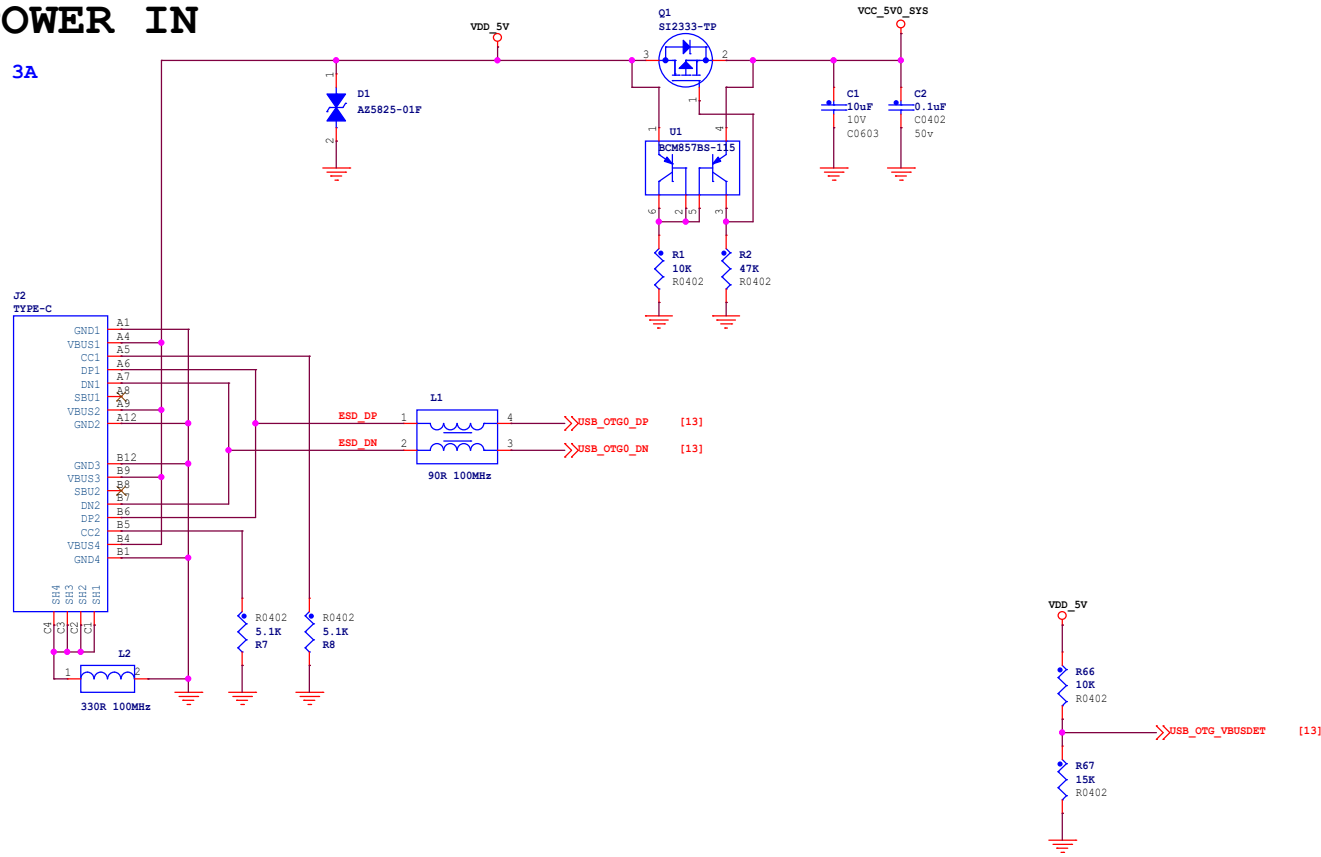
POWER DIAGRAM



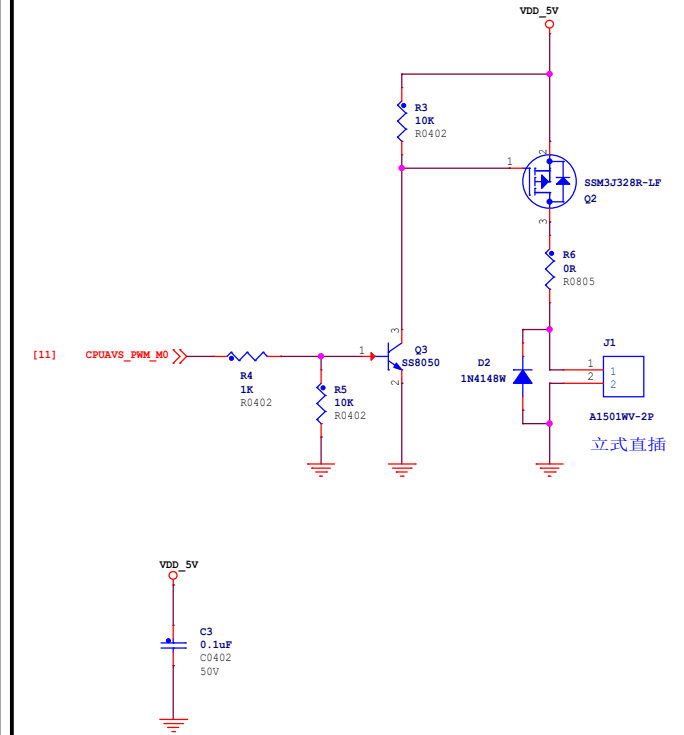
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POWER IN

5V 3A



Active Cooling

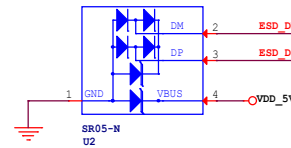


机械定位孔

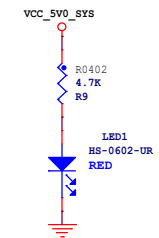
4*M3



USB ESD

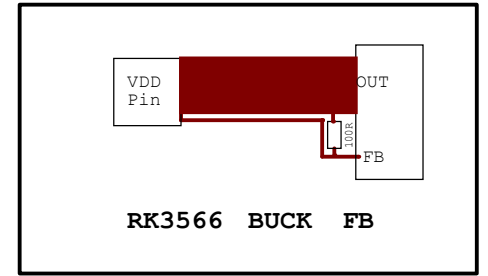
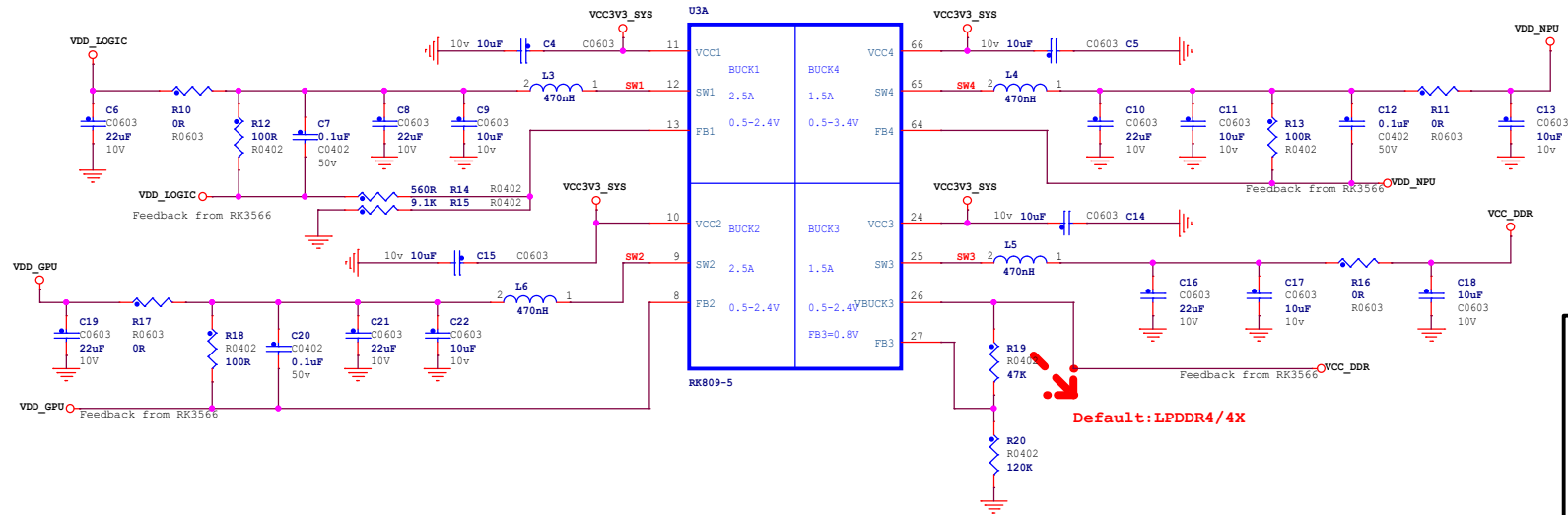


PWR_LED

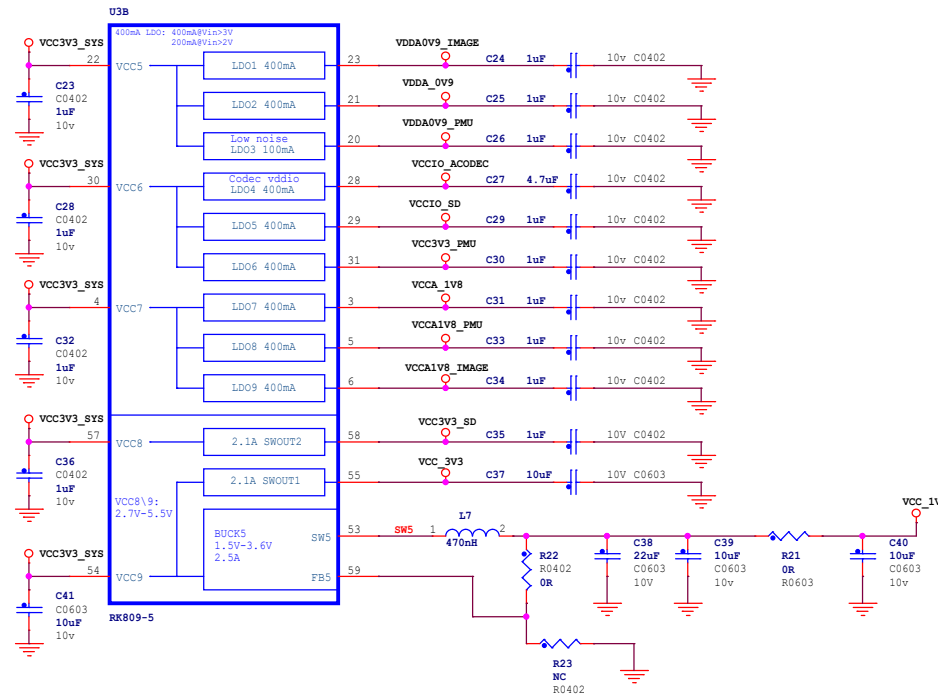


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PMIC RK809 DCDC

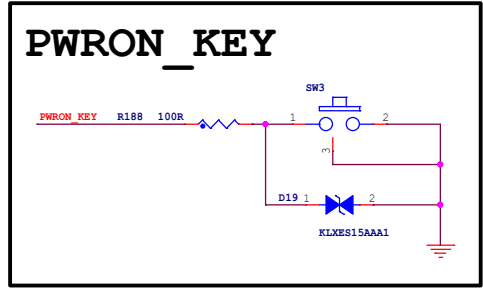
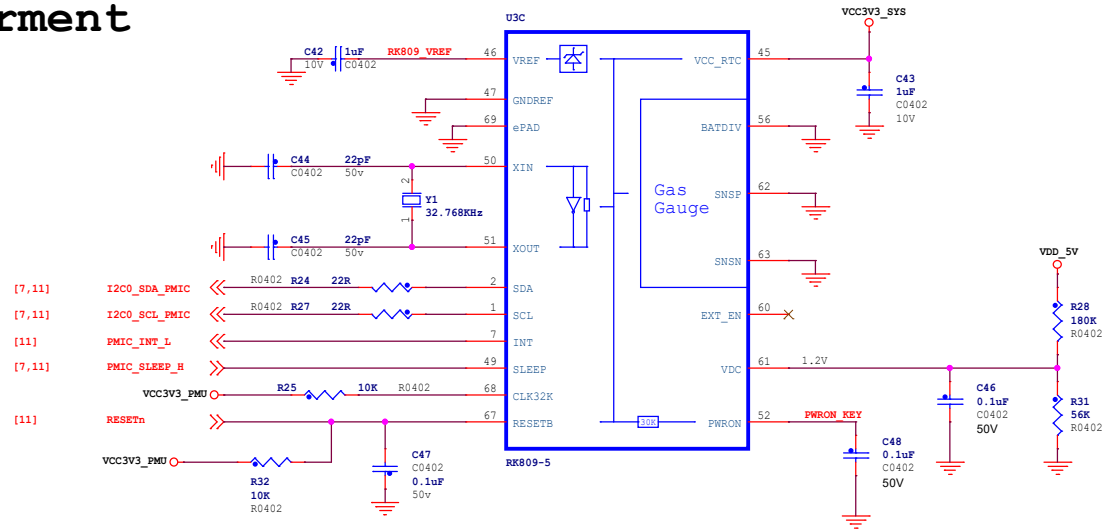


PMIC RK809 LDO

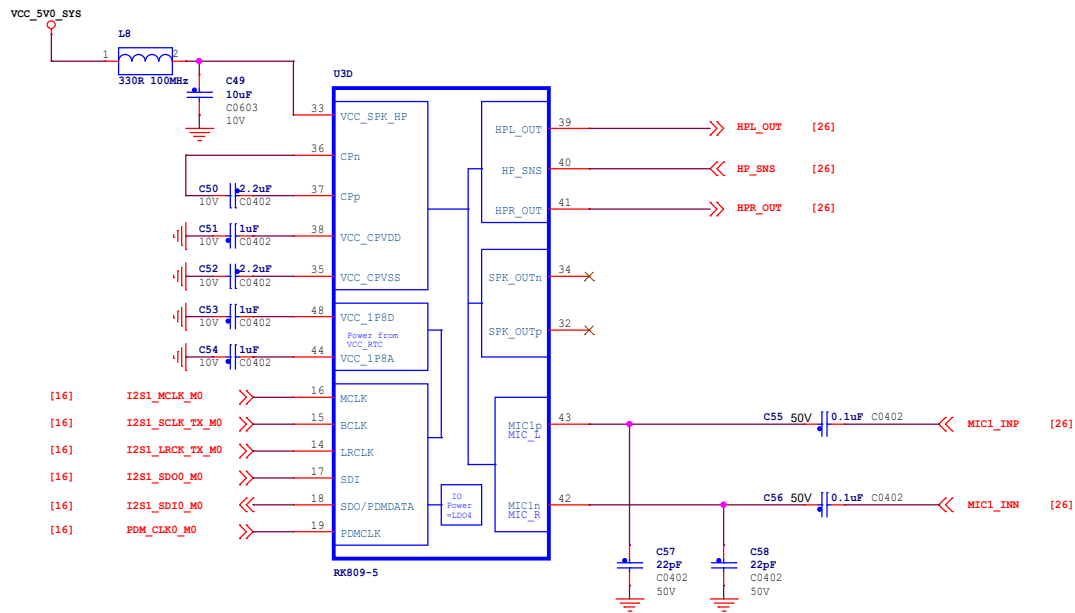


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PMIC RK809 Managerment

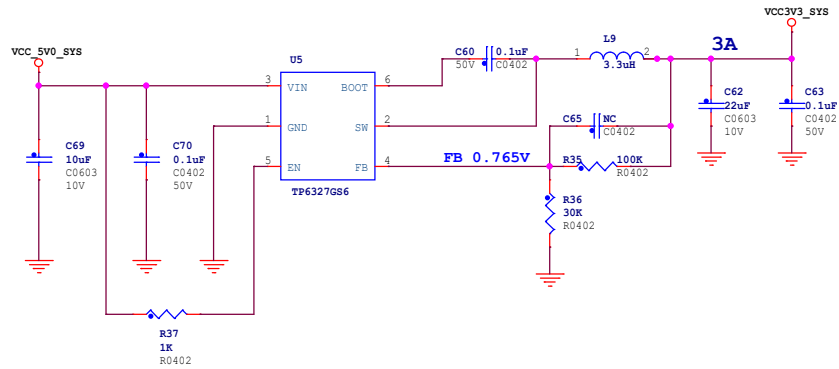


PMIC RK809 CODEC

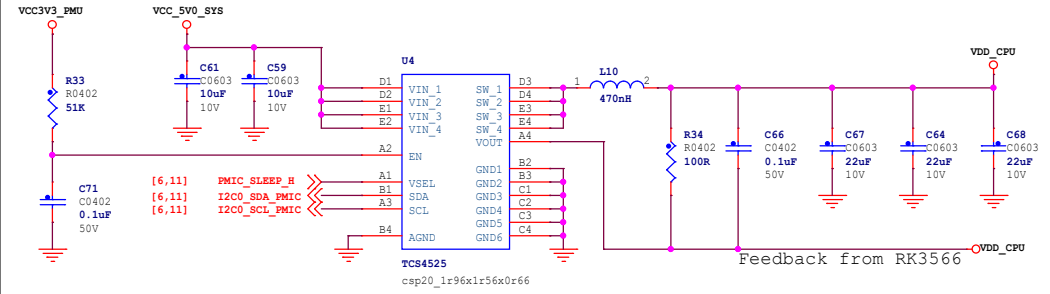


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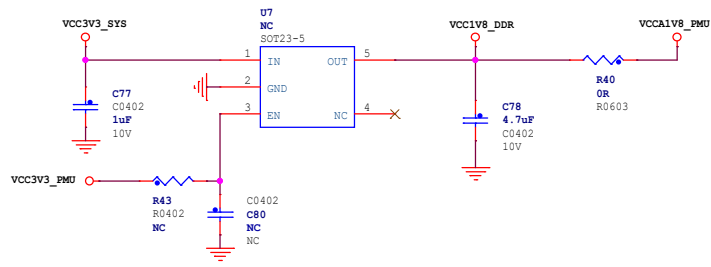
SYS_Power



RK3566 CPU Power VDD_CPU_EXT

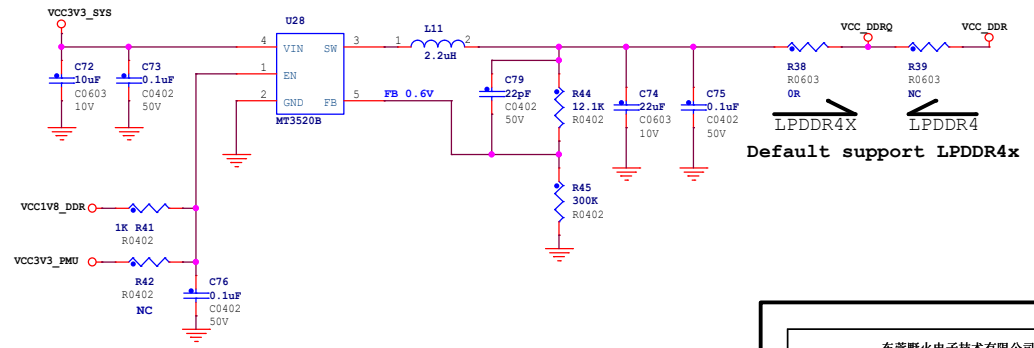


Auxiliary power supply LPDDR4_VCC1V8_DDR



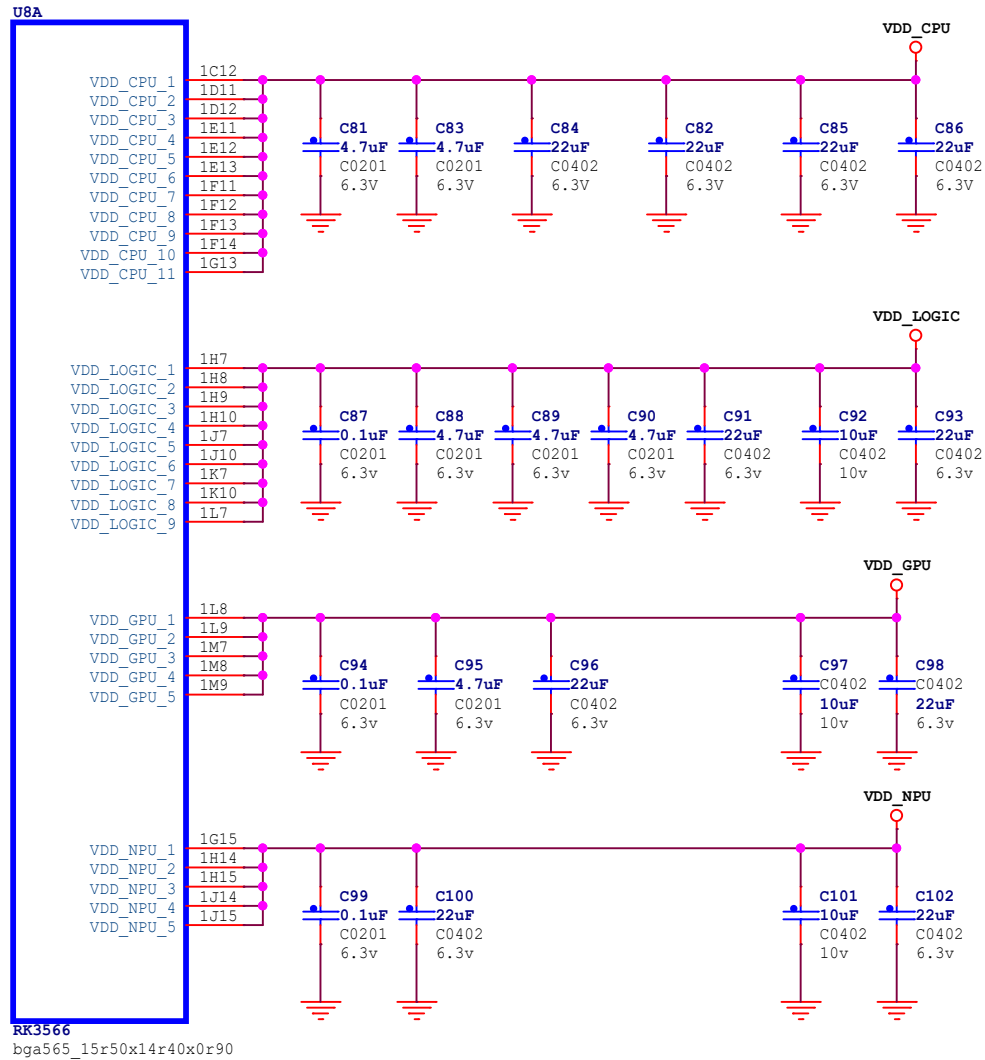
LPDDR4X Power

output: 0.6V

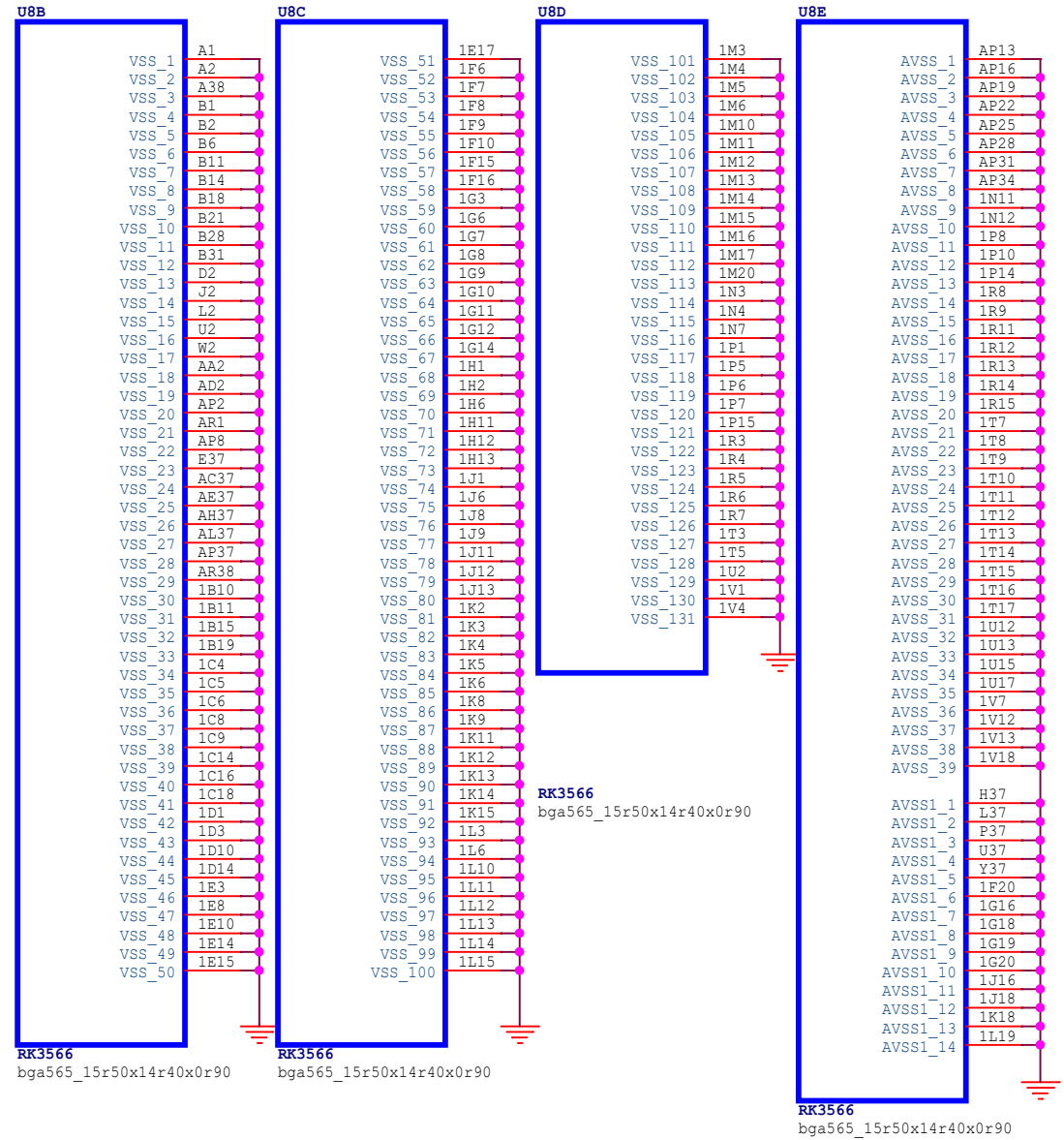


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RK3566_ABCDE (Power&GND)



RK3566
bga565_15r50x14r40x0r90



RK3566
bga565_15r50x14r40x0r90

RK3566
bga565_15r50x14r40x0r90

RK3566
bga565_15r50x14r40x0r90

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RK3566 (DDR PHY)

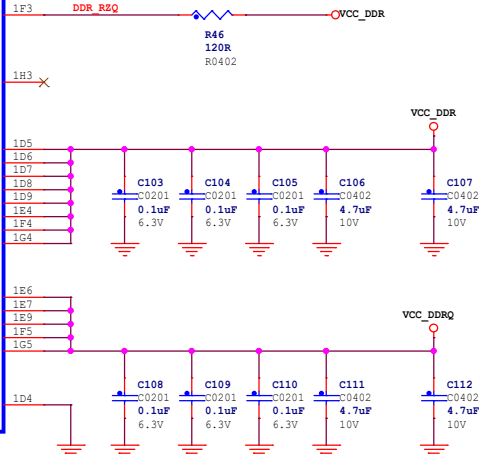
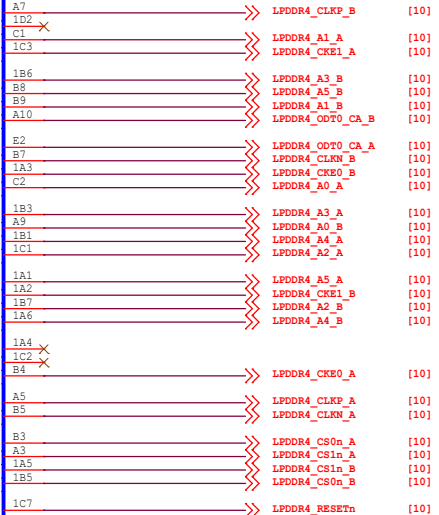
DBF



Signal	DDR4	LPDDR4	DDR3	LPDDR3	Signal	DDR4	LPDDR4	DDR3	LPDDR3
DDR DQ0 A	DDR4 DQ0 A	LPDDR4 DQ0 A	DDR3 DQ0	LPDDR3 DQ15	DDR4 A0	LPDDR4 CLKP B	DDR3 A9	---	---
DDR DQ1 A	DDR4 DQ1 A	LPDDR4 DQ1 A	DDR3 DQ1	LPDDR3 DQ14	DDR4 A1	---	DDR3 A7	---	---
DDR DQ2 A	DDR4 DQ2 A	LPDDR4 DQ2 A	DDR3 DQ2	LPDDR3 DQ13	DDR4 A2	LPDDR4 A1 A	DDR3 A5	LPDDR3 A6	---
DDR DQ3 A	DDR4 DQ3 A	LPDDR4 DQ3 A	DDR3 DQ3	LPDDR3 DQ12	DDR4 A3	LPDDR4 CKEL A	DDR3 A3	---	---
DDR DQ4 A	DDR4 DQ4 A	LPDDR4 DQ4 A	DDR3 DQ4	LPDDR3 DQ11	DDR4 A4	LPDDR4 A3 B	DDR3 BA1	LPDDR3 A3	---
DDR DQ5 A	DDR4 DQ5 A	LPDDR4 DQ5 A	DDR3 DQ5	LPDDR3 DQ10	DDR4 A5	LPDDR4 A3 B	DDR3 A11	LPDDR3 A2	---
DDR DQ6 A	DDR4 DQ6 A	LPDDR4 DQ6 A	DDR3 DQ6	LPDDR3 DQ9	DDR4 A6	LPDDR4 A1 B	DDR3 A10	LPDDR3 A1	---
DDR DQ7 A	DDR4 DQ7 A	LPDDR4 DQ7 A	DDR3 DQ7	LPDDR3 DQ8	DDR4 A7	LPDDR4 ODTO CA B	DDR3 A8	---	---
DDR DM0 A	DDR4 DML A	LPDDR4 DM0 A	DDR3 DM0	LPDDR3 DM1	DDR4 A8	LPDDR4 ODTO CA A	DDR3 A6	LPDDR3 A9	---
DDR DQS0P A	DDR4 DQSL P A	LPDDR4 DQS0P A	DDR3 DQS0P	LPDDR3 DQS1P	DDR4 A9	LPDDR4 CLKN B	DDR3 A5	---	---
DDR DQS0N A	DDR4 DQSL N A	LPDDR4 DQS0N A	DDR3 DQS0N	LPDDR3 DQS1N	DDR4 A10	LPDDR4 CKEL B	DDR3 A10	---	---
DDR DQ8 A	DDR4 DQ8 A	LPDDR4 DQ8 A	DDR3 DQ8	LPDDR3 DQ25	DDR4 A11	---	DDR3 A7	LPDDR3 A8	---
DDR DQ9 A	DDR4 DQ9 A	LPDDR4 DQ9 A	DDR3 DQ9	LPDDR3 DQ24	DDR4 A12	LPDDR4 A3 A	DDR3 BA2	---	---
DDR DQ10 A	DDR4 DQ10 A	LPDDR4 DQ10 A	DDR3 DQ10	LPDDR3 DQ23	DDR4 A13	LPDDR4 A0 B	DDR3 A14	LPDDR3 A0	---
DDR DQ11 A	DDR4 DQ11 A	LPDDR4 DQ11 A	DDR3 DQ11	LPDDR3 DQ22	DDR4 A14 WE#	LPDDR4 A4 A	DDR3 A15	LPDDR3 A5	---
DDR DQ12 A	DDR4 DQ12 A	LPDDR4 DQ12 A	DDR3 DQ12	LPDDR3 DQ21	DDR4 A15 CAS#	LPDDR4 A2 A	DDR3 A0	---	---
DDR DQ13 A	DDR4 DQ13 A	LPDDR4 DQ13 A	DDR3 DQ13	LPDDR3 DQ20	DDR4 A16 RAS#	LPDDR4 A5 A	DDR3 RAS#	LPDDR3 A7	---
DDR DQ14 A	DDR4 DQ14 A	LPDDR4 DQ14 A	DDR3 DQ14	LPDDR3 DQ19	DDR4 A17 ACEN	LPDDR4 CKEL B	DDR3 CAS#	---	---
DDR DQ15 A	DDR4 DQ15 A	LPDDR4 DQ15 A	DDR3 DQ15	LPDDR3 DQ18	DDR4 BA0	LPDDR4 A2 B	DDR3 A1	---	---
DDR DM1 A	DDR4 DMU A	LPDDR4 DM1 A	DDR3 DM1	LPDDR3 DM3	DDR4 BA1	LPDDR4 A4 B	DDR3 A12	LPDDR3 A4	---
DDR DQS1P A	DDR4 DQSU P A	LPDDR4 DQS1P A	DDR3 DQS1P	LPDDR3 DQS1P	DDR4 BQ0	LPDDR4 ODTO CA B	DDR3 WE#	---	---
DDR DQS1N A	DDR4 DQSU N A	LPDDR4 DQS1N A	DDR3 DQS1N	LPDDR3 DQS1N	DDR4 BQ1	LPDDR4 ODTO CA A	DDR3 BA0	---	---
DDR DQ0 B	DDR4 DQ0 B	LPDDR4 DQ0 B	DDR3 DQ16	LPDDR3 DQ1	DDR4 BQ2	LPDDR4 CKEL A	DDR3 WE#	---	---
DDR DQ1 B	DDR4 DQ1 B	LPDDR4 DQ1 B	DDR3 DQ17	LPDDR3 DQ2	DDR4 BQ3	LPDDR4 CKEL B	DDR3 WE#	---	---
DDR DQ2 B	DDR4 DQ2 B	LPDDR4 DQ2 B	DDR3 DQ18	LPDDR3 DQ3	DDR4 BQ4	---	---	---	---
DDR DQ3 B	DDR4 DQ3 B	LPDDR4 DQ3 B	DDR3 DQ19	LPDDR3 DQ4	DDR4 BQ5	---	---	---	---
DDR DQ4 B	DDR4 DQ4 B	LPDDR4 DQ4 B	DDR3 DQ20	LPDDR3 DQ5	DDR4 BQ6	---	---	---	---
DDR DQ5 B	DDR4 DQ5 B	LPDDR4 DQ5 B	DDR3 DQ21	LPDDR3 DQ6	DDR4 BQ7	---	---	---	---
DDR DQ6 B	DDR4 DQ6 B	LPDDR4 DQ6 B	DDR3 DQ22	LPDDR3 DQ7	DDR4 BQ8	---	---	---	---
DDR DQ7 B	DDR4 DQ7 B	LPDDR4 DQ7 B	DDR3 DQ23	LPDDR3 DQ8	DDR4 BQ9	---	---	---	---
DDR DM0 B	DDR4 DMU B	LPDDR4 DM0 B	DDR3 DM2	LPDDR3 DM0	DDR4 BQ10	---	---	---	---
DDR DQS0P B	DDR4 DQSU P B	LPDDR4 DQS0P B	DDR3 DQS2P	LPDDR3 DQS0P	DDR4 BQ11	---	---	---	---
DDR DQS0N B	DDR4 DQSU N B	LPDDR4 DQS0N B	DDR3 DQS2N	LPDDR3 DQS0N	DDR4 BQ12	---	---	---	---
DDR DQ8 B	DDR4 DQ8 B	LPDDR4 DQ8 B	DDR3 DQ24	LPDDR3 DQ19	DDR4 BQ13	---	---	---	---
DDR DQ9 B	DDR4 DQ9 B	LPDDR4 DQ9 B	DDR3 DQ25	LPDDR3 DQ18	DDR4 BQ14	---	---	---	---
DDR DQ10 B	DDR4 DQ10 B	LPDDR4 DQ10 B	DDR3 DQ26	LPDDR3 DQ17	DDR4 BQ15	---	---	---	---
DDR DQ11 B	DDR4 DQ11 B	LPDDR4 DQ11 B	DDR3 DQ27	LPDDR3 DQ16	DDR4 BQ16	---	---	---	---
DDR DQ12 B	DDR4 DQ12 B	LPDDR4 DQ12 B	DDR3 DQ28	LPDDR3 DQ15	DDR4 BQ17	---	---	---	---
DDR DQ13 B	DDR4 DQ13 B	LPDDR4 DQ13 B	DDR3 DQ29	LPDDR3 DQ14	DDR4 BQ18	---	---	---	---
DDR DQ14 B	DDR4 DQ14 B	LPDDR4 DQ14 B	DDR3 DQ30	LPDDR3 DQ13	DDR4 BQ19	---	---	---	---
DDR DQ15 B	DDR4 DQ15 B	LPDDR4 DQ15 B	DDR3 DQ31	LPDDR3 DQ12	DDR4 BQ20	---	---	---	---
DDR DM1 B	DDR4 DML B	LPDDR4 DM1 B	DDR3 DM3	LPDDR3 DM2	DDR4 BQ21	---	---	---	---
DDR DQS1P B	DDR4 DQSL P B	LPDDR4 DQS1P B	DDR3 DQS3P	LPDDR3 DQS2P	DDR4 BQ22	---	---	---	---
DDR DQS1N B	DDR4 DQSL N B	LPDDR4 DQS1N B	DDR3 DQS3N	LPDDR3 DQS2N	DDR4 BQ23	---	---	---	---

Note:
Except DDR3, other DQ sequences
can not be swap

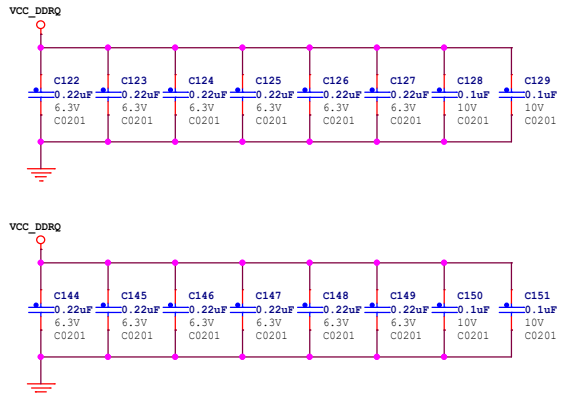
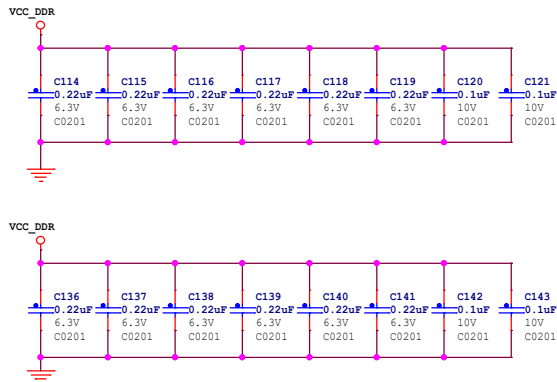
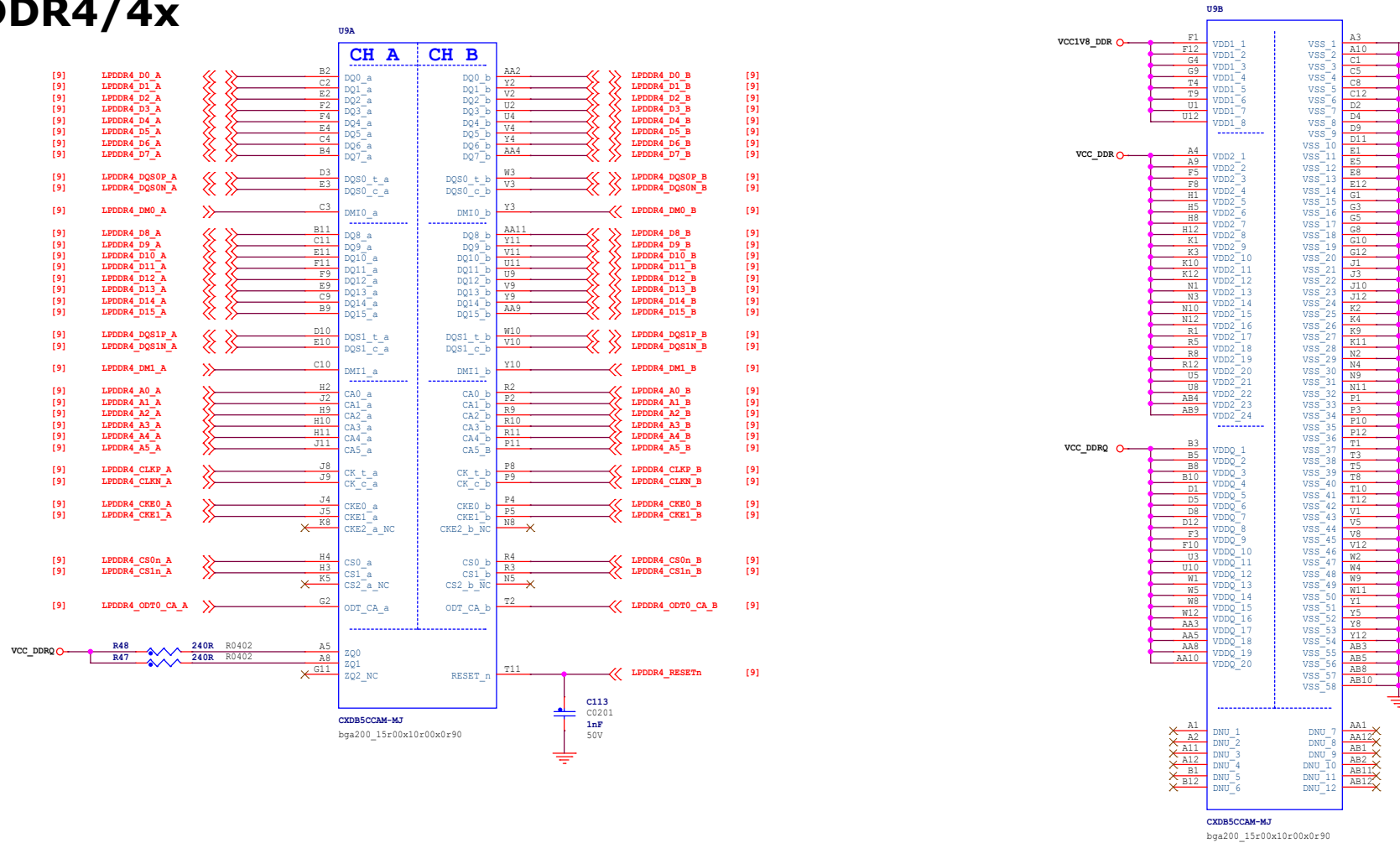
Note: Sequences can not be swap



	VDDQ	VDDQL
DDR3L	1.35V	1.35V
DDR3	1.50V	1.50V
DDR4	1.20V	1.20V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	0.60V

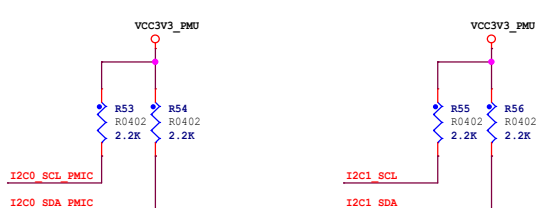
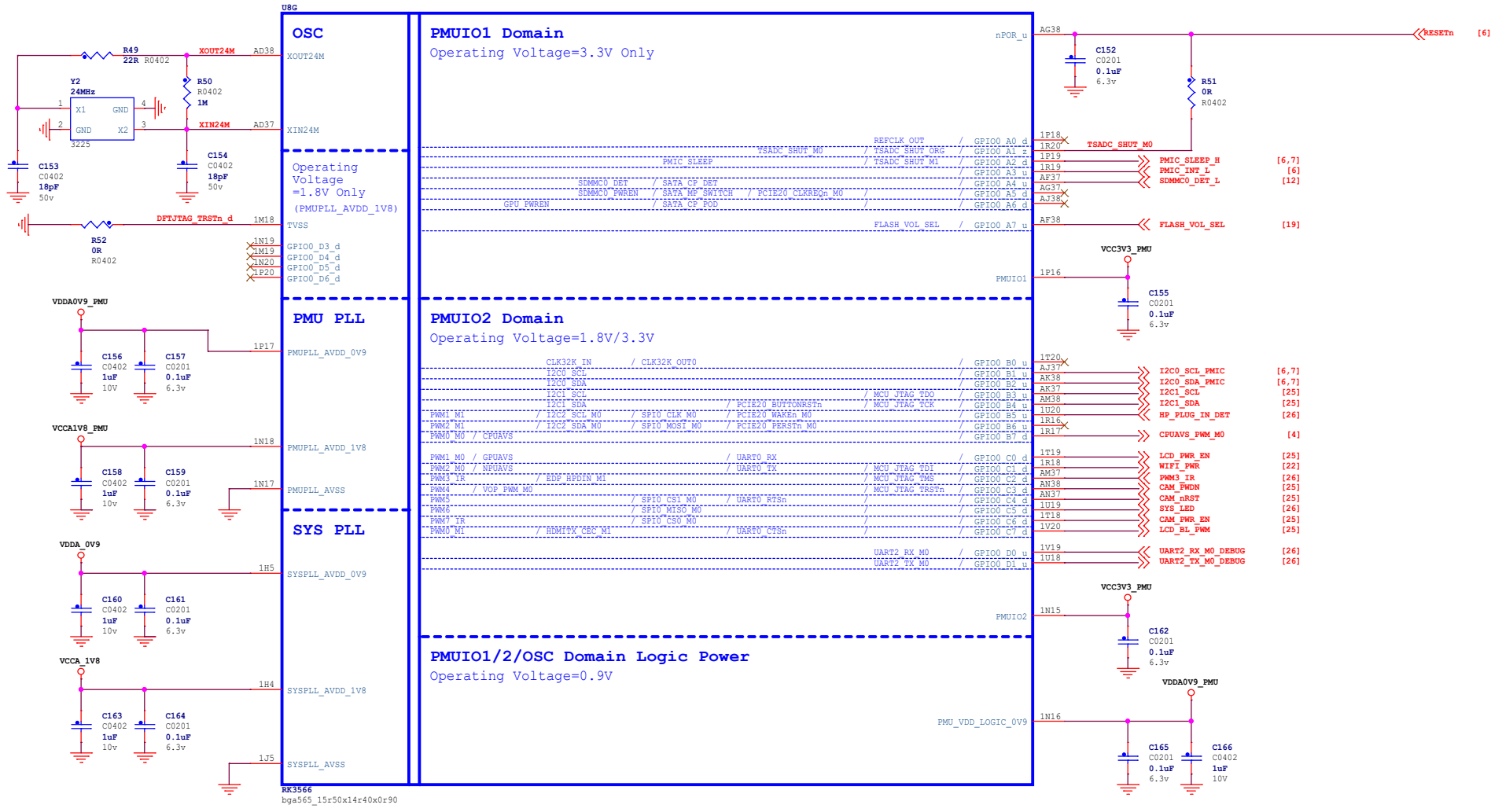
RK3566
bga565_15x50x14r40x0r90

LPDDR4/4x



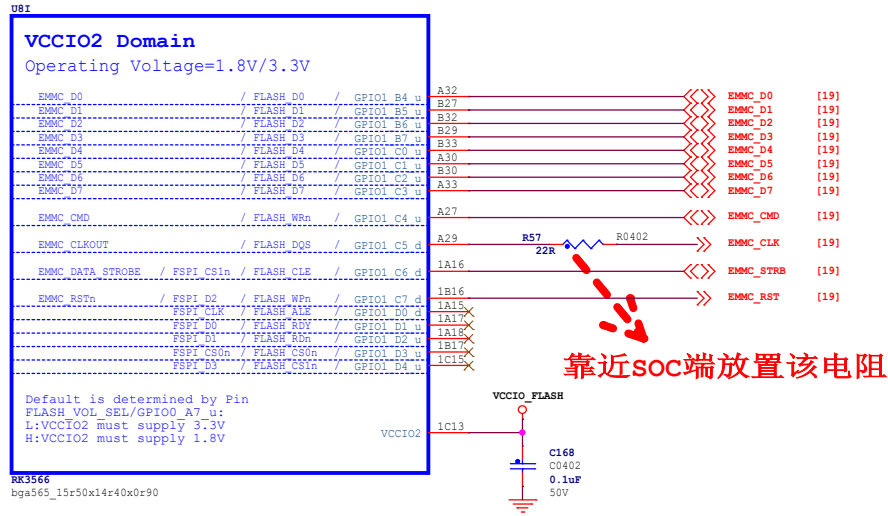
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RK3566_G (OSC/PLL/PMUIO1/2)

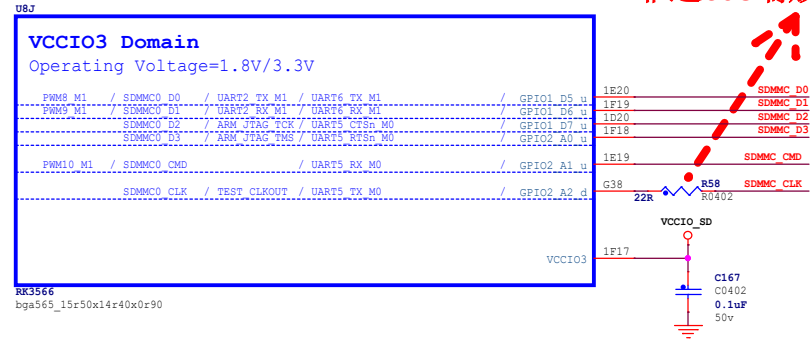


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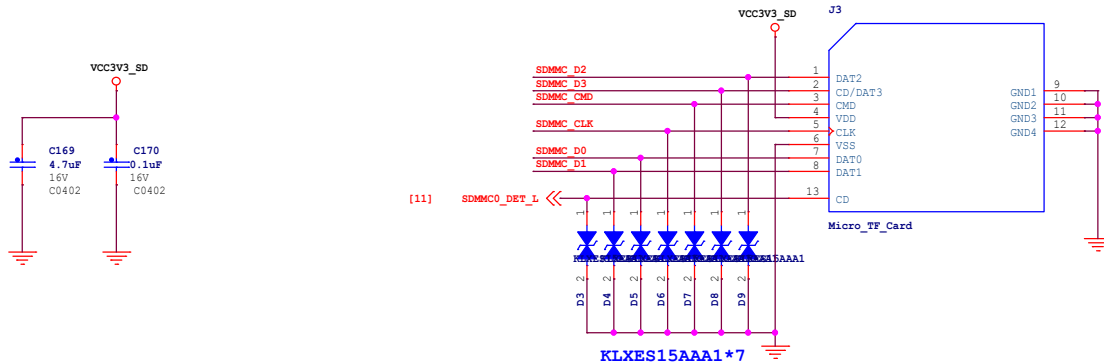
RK3566_I (VCCIO2 Domain) EMMC_IO



RK3566_J (VCCIO3 Domain) SDMMC_IO

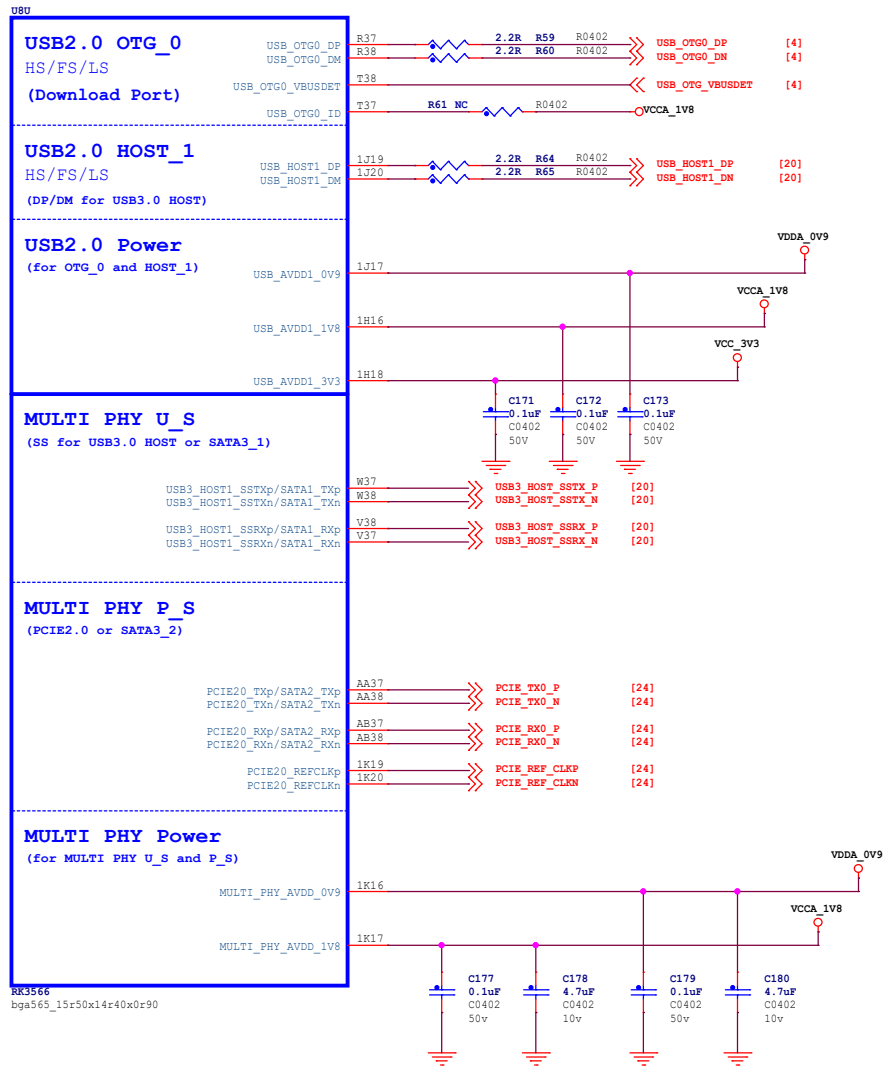


TF_CARD

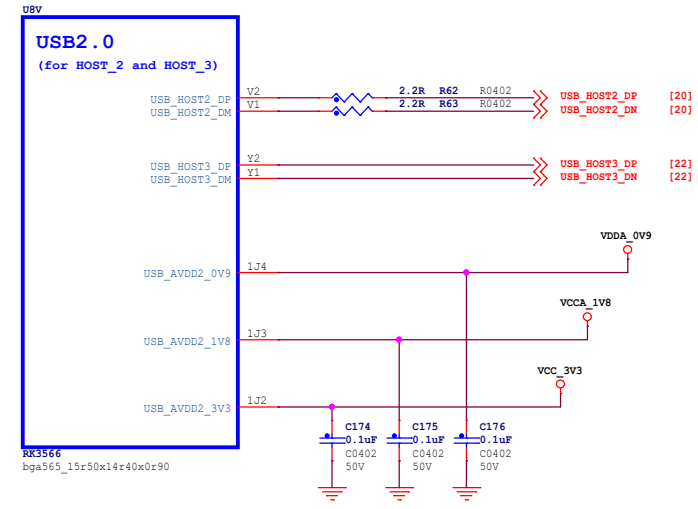


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RK3566_U (USB3.0/SATA/PCIE2.0 x1)



RK3566_V (USB2.0 HOST)

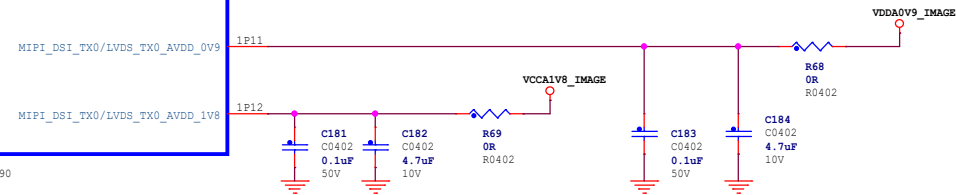


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RK3566_R (MIPI_DSI_TX0/LVDS_TX0)

MIPI DSI TX0/LVDS TX0

MIPI_DSI_TX0_D0p/LVDS_TX0_D0p	AP30	MIPI_DSI_TX0_D0P	[25]
MIPI_DSI_TX0_D0n/LVDS_TX0_D0n	AR30	MIPI_DSI_TX0_D0N	[25]
MIPI_DSI_TX0_D1p/LVDS_TX0_D1p	AR29	MIPI_DSI_TX0_D1P	[25]
MIPI_DSI_TX0_D1n/LVDS_TX0_D1n	AF29	MIPI_DSI_TX0_D1N	[25]
MIPI_DSI_TX0_D2p/LVDS_TX0_D2p	AR27	MIPI_DSI_TX0_D2P	[25]
MIPI_DSI_TX0_D2n/LVDS_TX0_D2n	AR27	MIPI_DSI_TX0_D2N	[25]
MIPI_DSI_TX0_D3p/LVDS_TX0_D3p	AR26	MIPI_DSI_TX0_D3P	[25]
MIPI_DSI_TX0_D3n/LVDS_TX0_D3n	AF26	MIPI_DSI_TX0_D3N	[25]
MIPI_DSI_TX0_CLKp/LVDS_TX0_CLKp	1V16	MIPI_DSI_TX0_CLKP	[25]
MIPI_DSI_TX0_CLKn/LVDS_TX0_CLKn	1V15	MIPI_DSI_TX0_CLKN	[25]

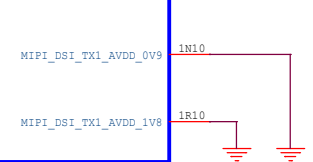


RR3566
bga565_15r50x14r40x0r90

RK3566_S (MIPI_DSI_TX1)

MIPI DSI TX1

MIPI_DSI_TX1_D0p	AP24		
MIPI_DSI_TX1_D0n	AR24		
MIPI_DSI_TX1_D1p	AR21		
MIPI_DSI_TX1_D1n	AF21		
MIPI_DSI_TX1_D2p	AP21		
MIPI_DSI_TX1_D2n	AR21		
MIPI_DSI_TX1_D3p	AR20		
MIPI_DSI_TX1_D3n	AF20		
MIPI_DSI_TX1_CLKp	1V11		
MIPI_DSI_TX1_CLKn	1U11		

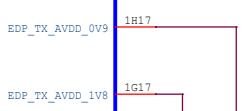


RR3566
bga565_15r50x14r40x0r90

RK3566_T (eDP/DP TX)

eDP_TX

EDP_TX_D0p	J37		
EDP_TX_D0n	J38		
EDP_TX_D1p	K38		
EDP_TX_D1n	K37		
EDP_TX_D2p	M37		
EDP_TX_D2n	M38		
EDP_TX_D3p	N37		
EDP_TX_D3n	N38		
EDP_TX_AUXp	1H19		
EDP_TX_AUXn	1H20		

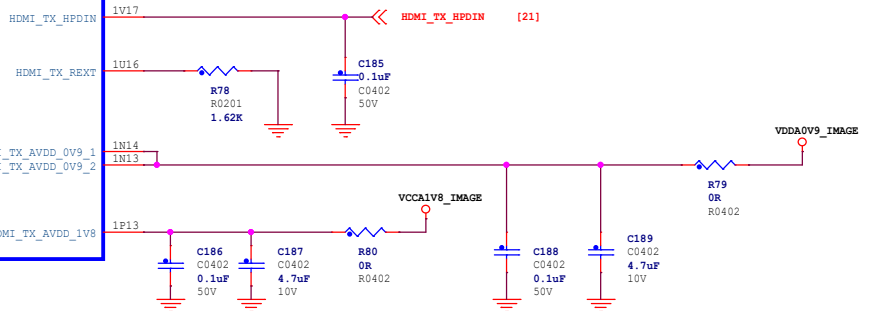


RR3566
bga565_15r50x14r40x0r90

RK3566_Q (HDMI2.0 TX)

HDMI2.0 TX

HDMI_TX_D2p	AP36	2.2R	R70	R0402	HDMI_TX_D2P	[21]
HDMI_TX_D2n	AR36	2.2R	R71	R0402	HDMI_TX_D2N	[21]
HDMI_TX_D1p	AR35	2.2R	R72	R0402	HDMI_TX_D1P	[21]
HDMI_TX_D1n	AP35	2.2R	R73	R0402	HDMI_TX_D1N	[21]
HDMI_TX_D0p	AP33	2.2R	R74	R0402	HDMI_TX_D0P	[21]
HDMI_TX_D0n	AR33	2.2R	R75	R0402	HDMI_TX_D0N	[21]
HDMI_TX_CLKp	AR32	2.2R	R76	R0402	HDMI_TX_CLKP	[21]
HDMI_TX_CLKn	AP32	2.2R	R77	R0402	HDMI_TX_CLKN	[21]



RR3566
bga565_15r50x14r40x0r90

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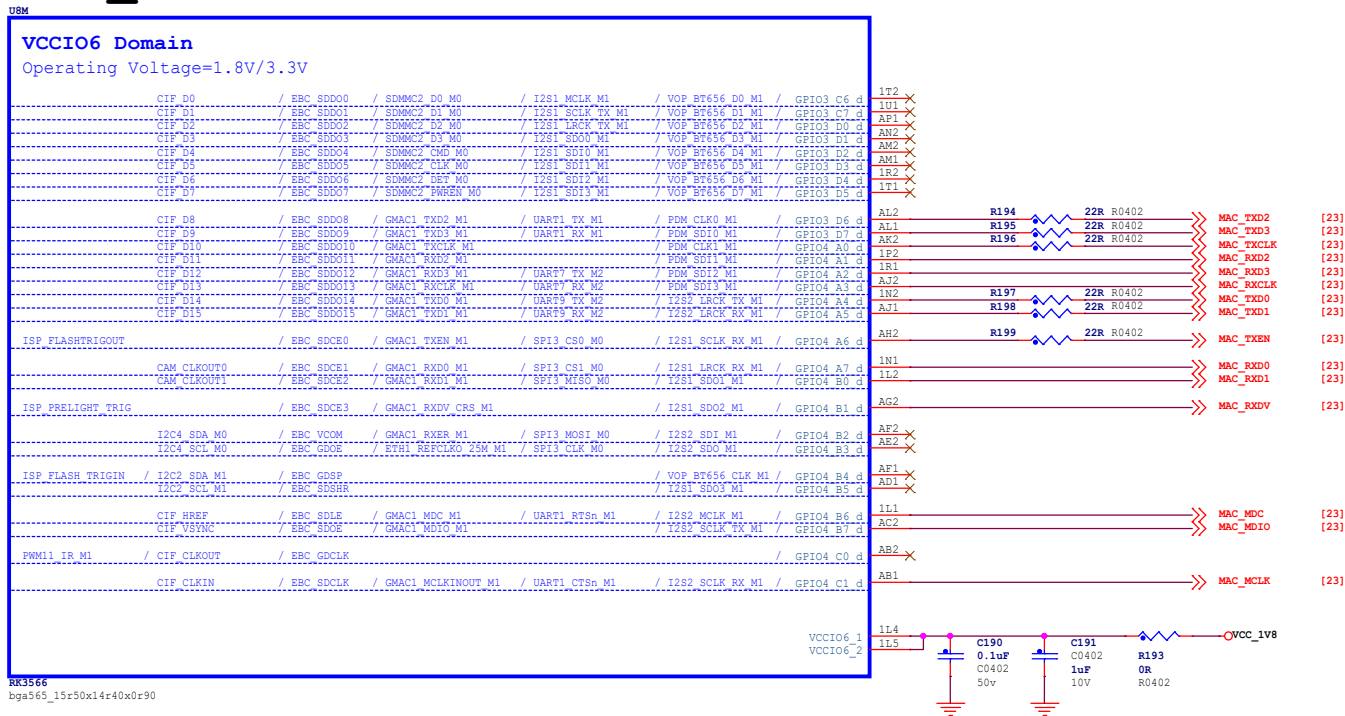
Title
野火_RK3566 LubanCat 1 N_原理图

Size A3	Document Number MIPI_DSI/EDP/HDMI_Controller	Rev V1.0
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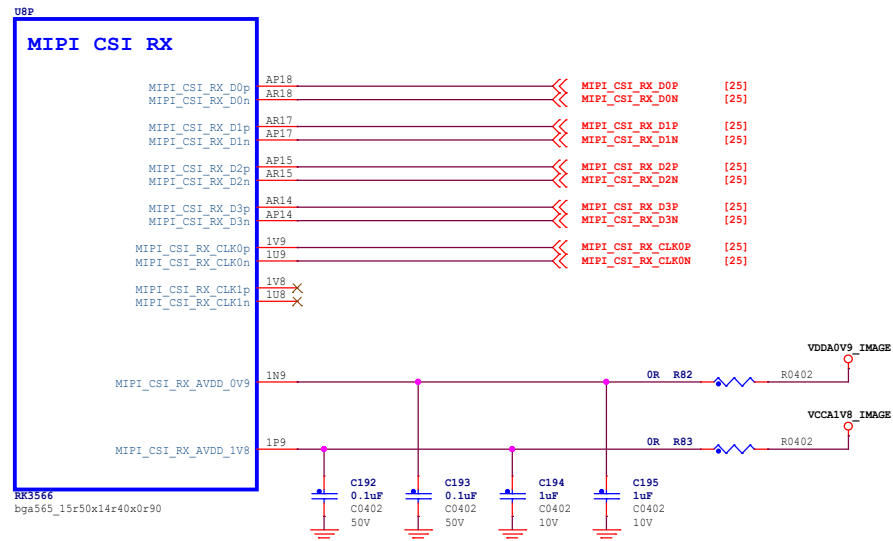
Date: Monday, December 12, 2022 Sheet 14 of 26

RK3566_M (VCCIO6 Domain)

GMAC_Controller



RK3566_P (MIPI_CSI_RX)

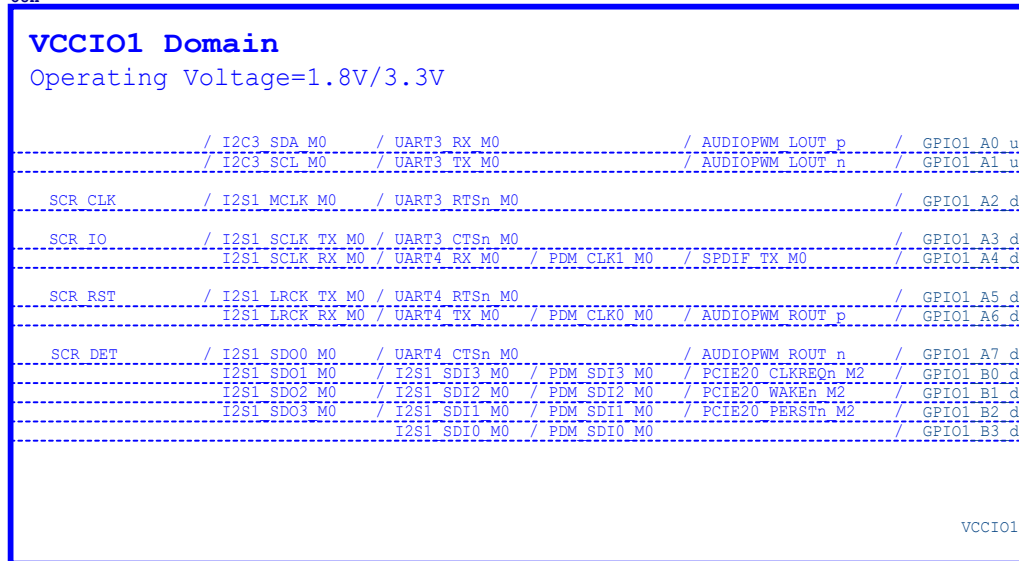


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野火_RK3566 LubanCat 1 N_原理图		
Size	Document Number	Rev
A3	MIPI_CSI/GMAC_Controller	V1.0
Date:	Monday, December 12, 2022	Sheet 15 of 26

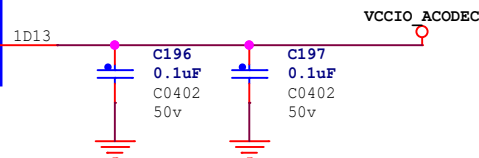
RK3566_H (VCCIO1 Domain)

U8H



RK3566
bga565_15r50x14r40x0r90

VCCIO1



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Title
野火_RK3566 LubanCat 1 N_原理图

Size A4	Document Number RK3566_Audio Interface	Rev V1.0
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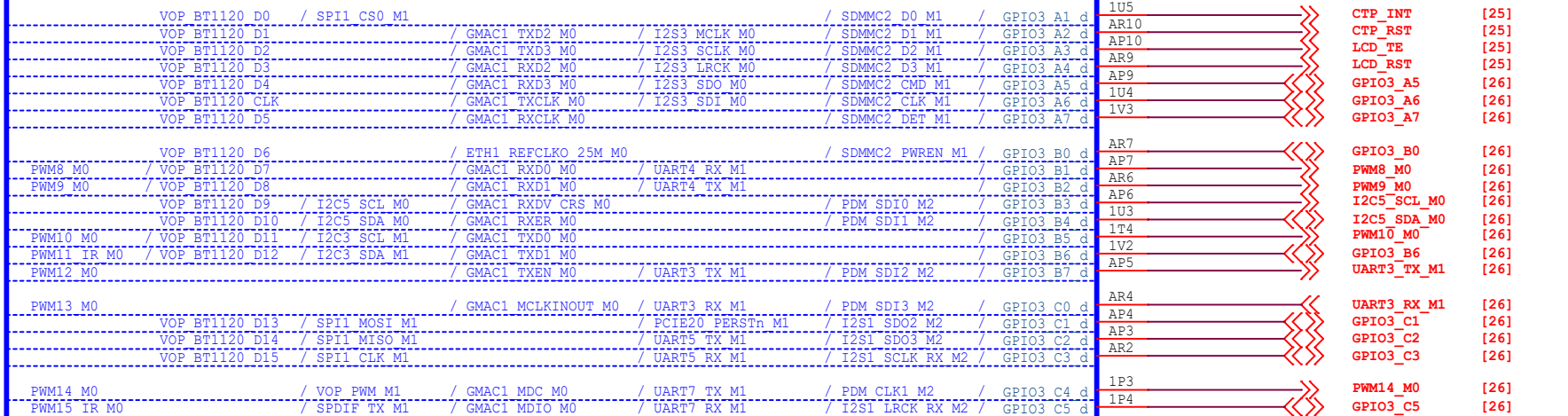
Date: Monday, December 12, 2022 Sheet 16 of 26

RK3566_L (VCCIO5 Domain)

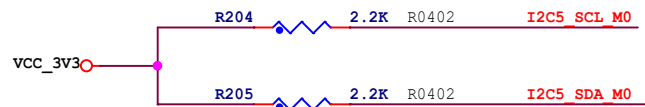
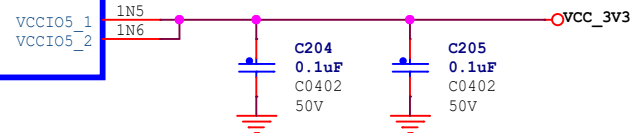
U8L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V



RR3566
bga565_15r50x14r40x0r90



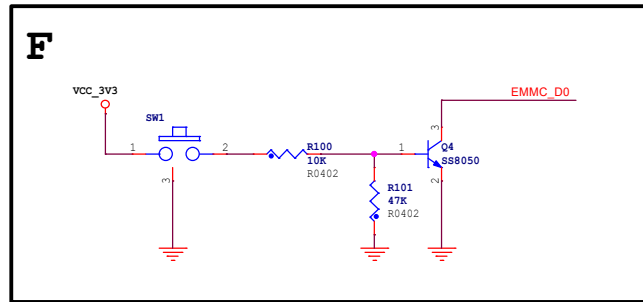
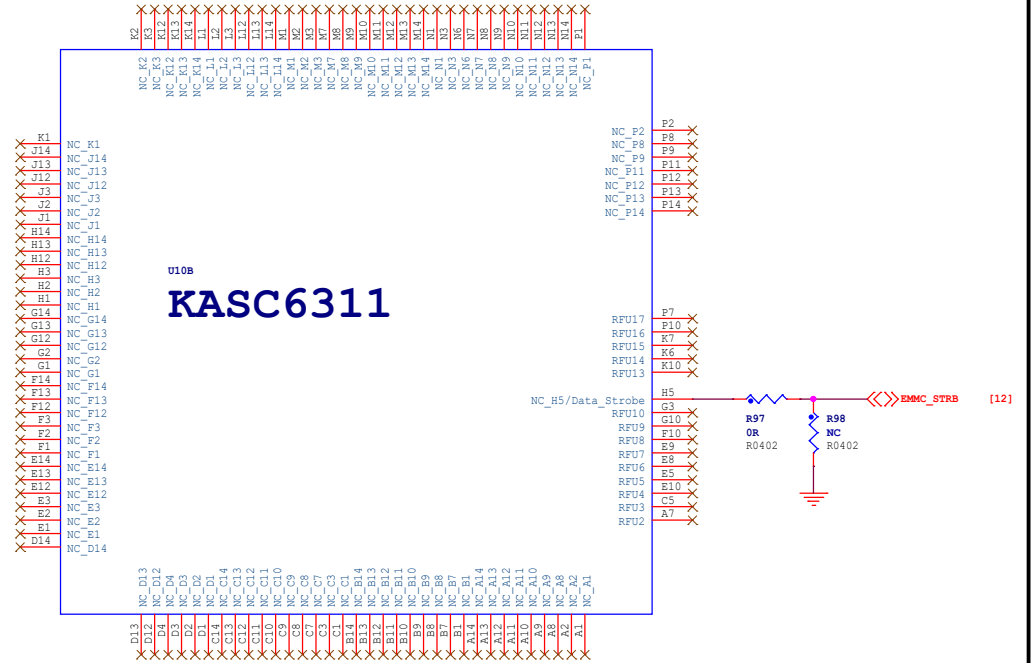
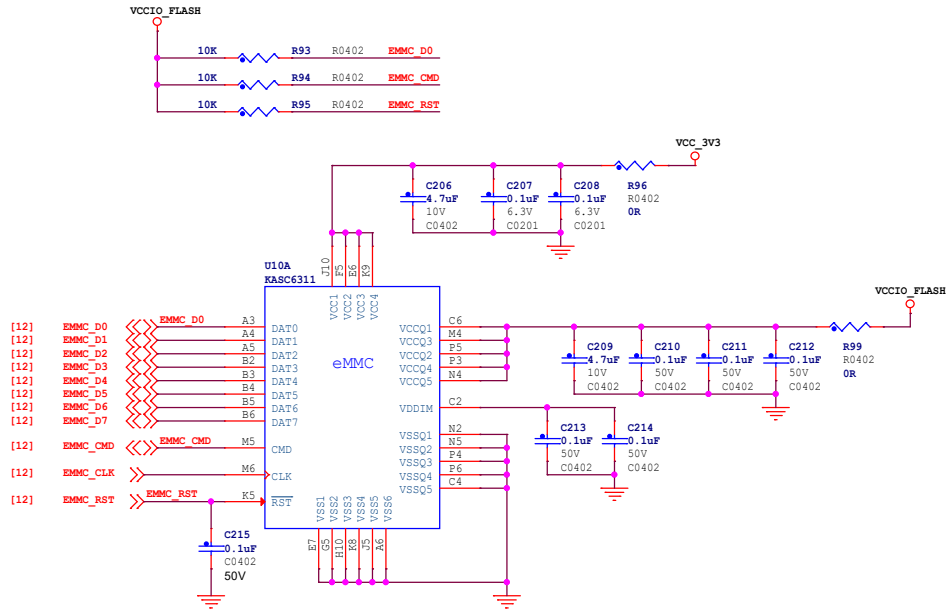
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Title 野火_RK3566 LubanCat 1 N_原理图

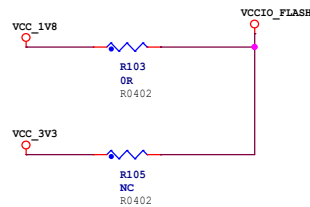
Size A4	Document Number RK3566_VO Interface	Rev V1.0
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Date: Monday, December 12, 2022 Sheet 18 of 26

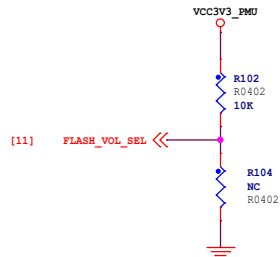
EMMC FLASH



EMMC_IO_Toggle



FLASH_VOL_SEL



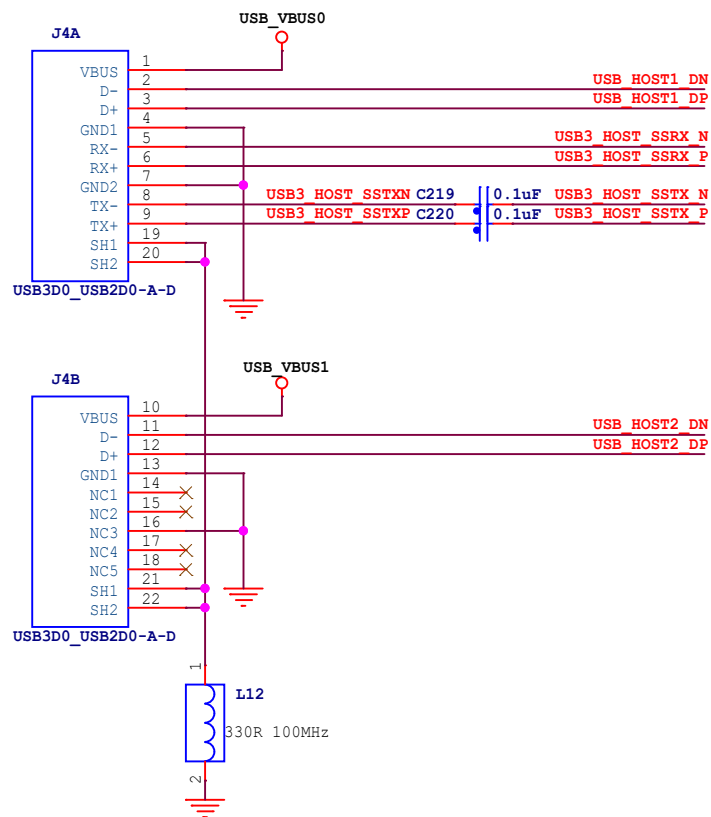
Note:

FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
 Logic=L: 3.3V IO driven
 Logic=H: 1.8V IO driven

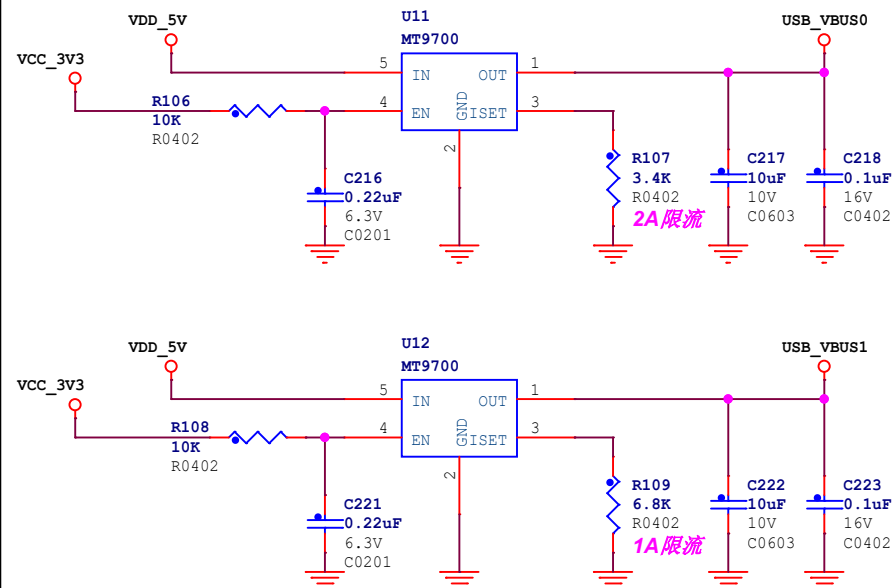
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Title	野火_RK3566 LubanCat 1 N_原理图	
Size	Document Number	Rev
A3	EMMC_FLASH	V1.0
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USB 3.0 HOST x1

USB 2.0 HOST x1

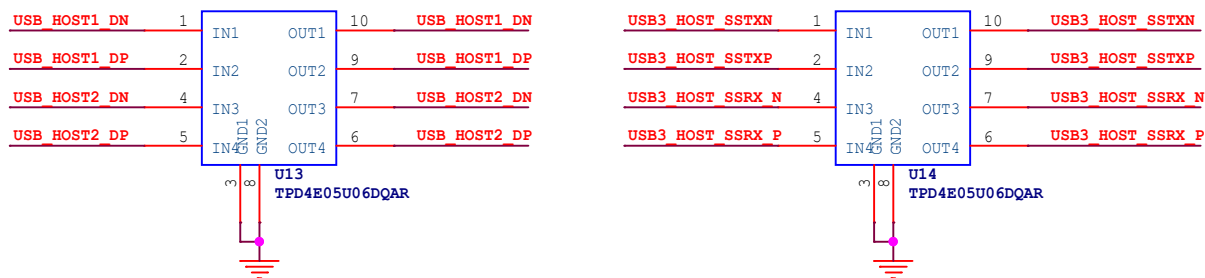


USB POWER



USB_HOST1_DN	→	USB_HOST1_DN	[13]
USB_HOST1_DP	→	USB_HOST1_DP	[13]
USB_HOST2_DN	→	USB_HOST2_DN	[13]
USB_HOST2_DP	→	USB_HOST2_DP	[13]
USB3_HOST_SSRX_N	→	USB3_HOST_SSRX_N	[13]
USB3_HOST_SSRX_P	→	USB3_HOST_SSRX_P	[13]
USB3_HOST_SSTX_N	→	USB3_HOST_SSTX_N	[13]
USB3_HOST_SSTX_P	→	USB3_HOST_SSTX_P	[13]

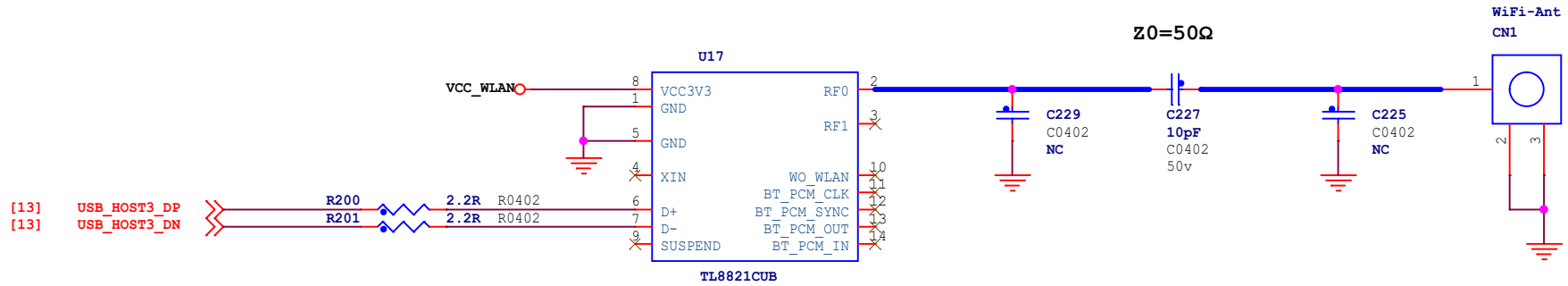
ESD



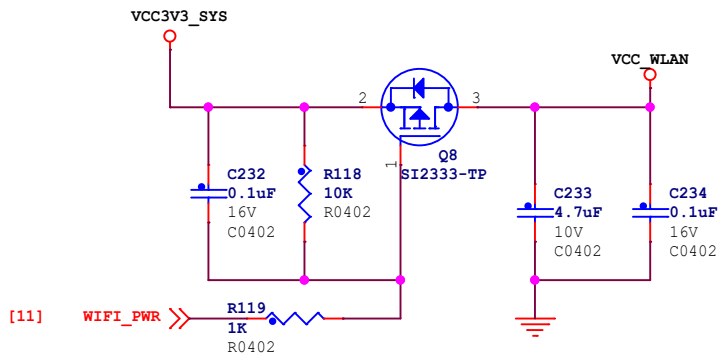
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Title		
野火_RK3566 LubanCat 1 N_原理图		
Size	Document Number	Rev
A4	USB_PORT	V1.0
Date:	Monday, December 12, 2022	Sheet 20 of 26

WLAN



WLAN_Power



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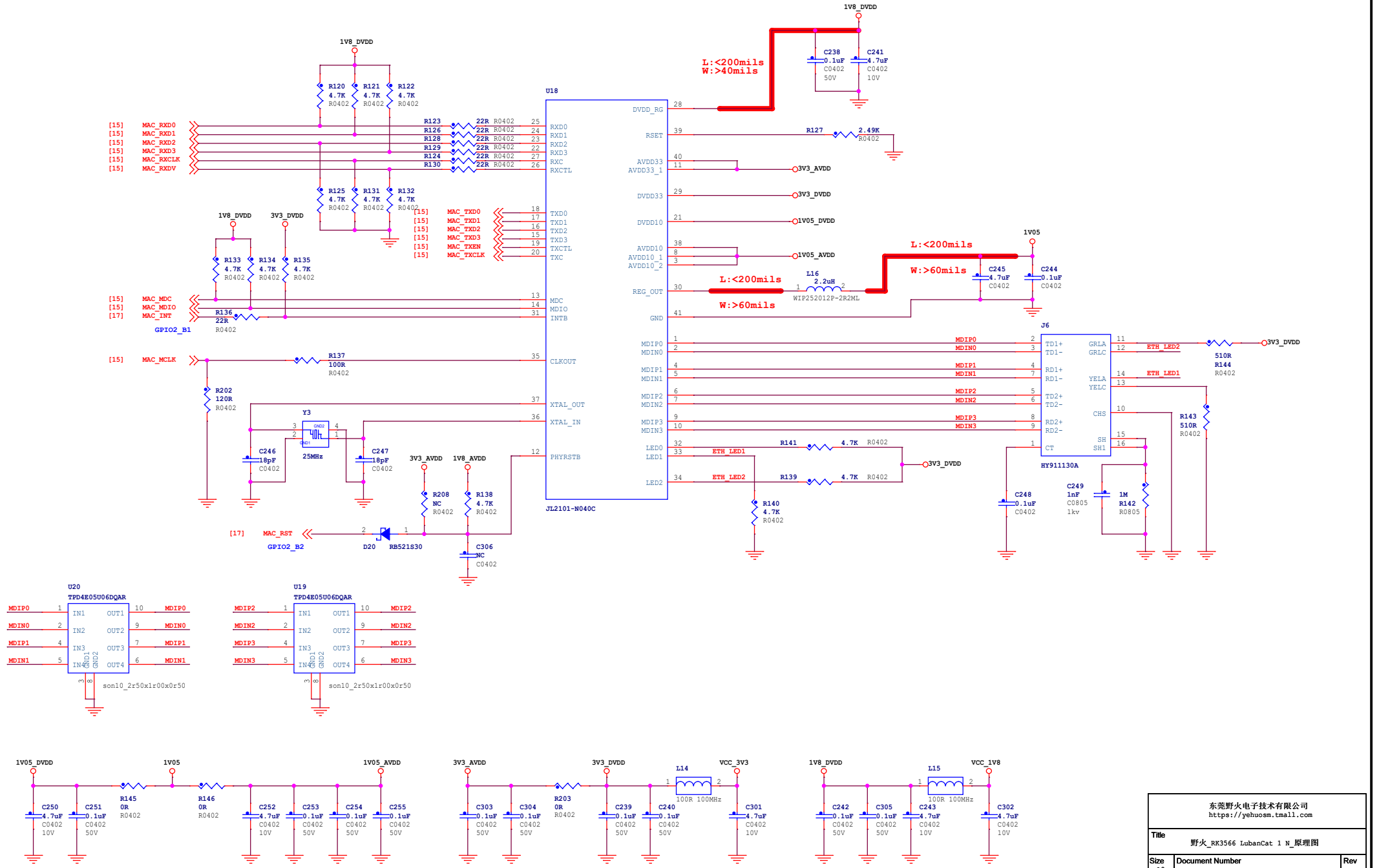
Title: 野火_RK3566 LubanCat 1 N_原理图

Size: A4	Document Number: WLAN	Rev: V1.0
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Date: Monday, December 12, 2022 Sheet 22 of 26

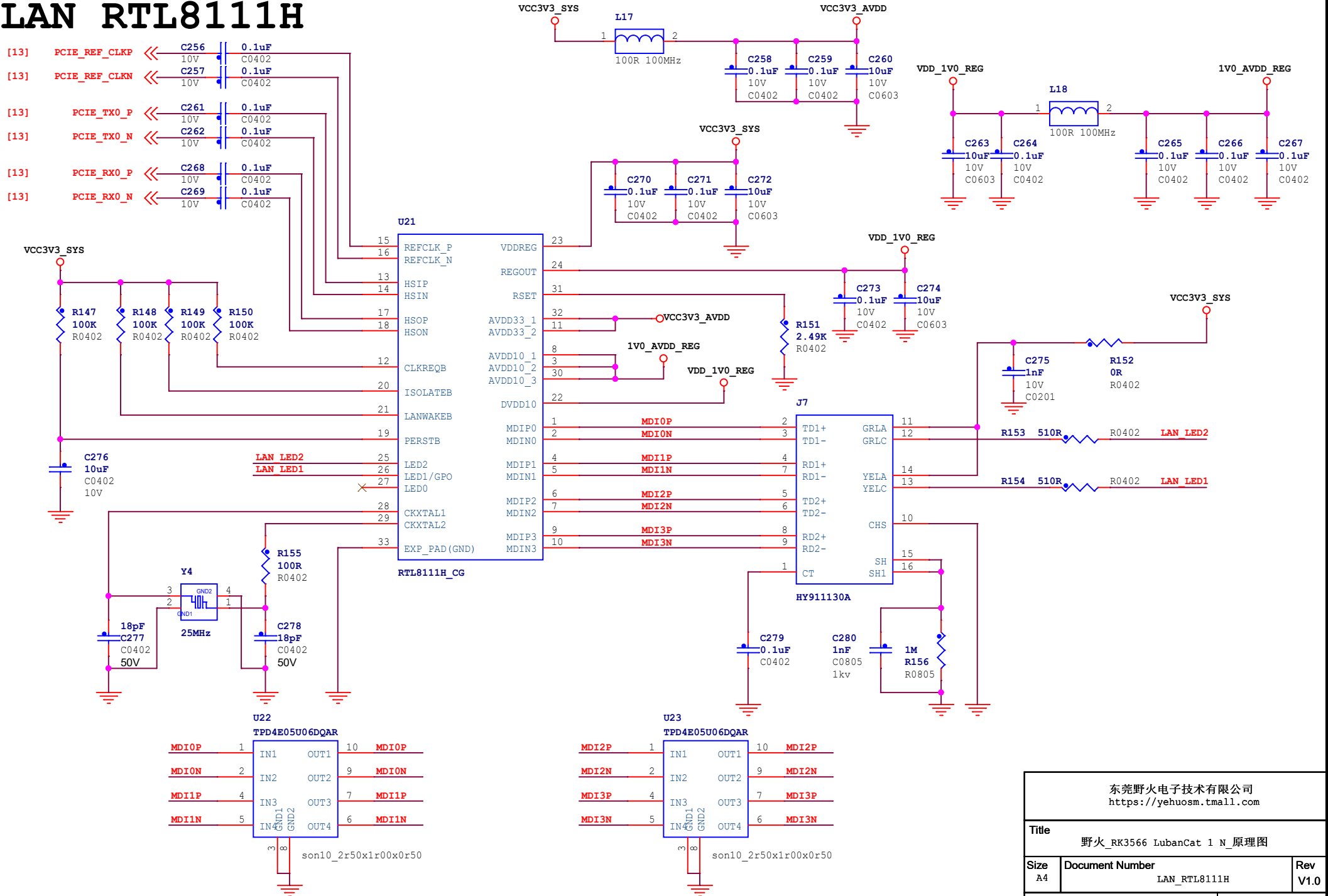
JL2101-N040C

TXC / RXC : delays 2ns
PHY Address : 001



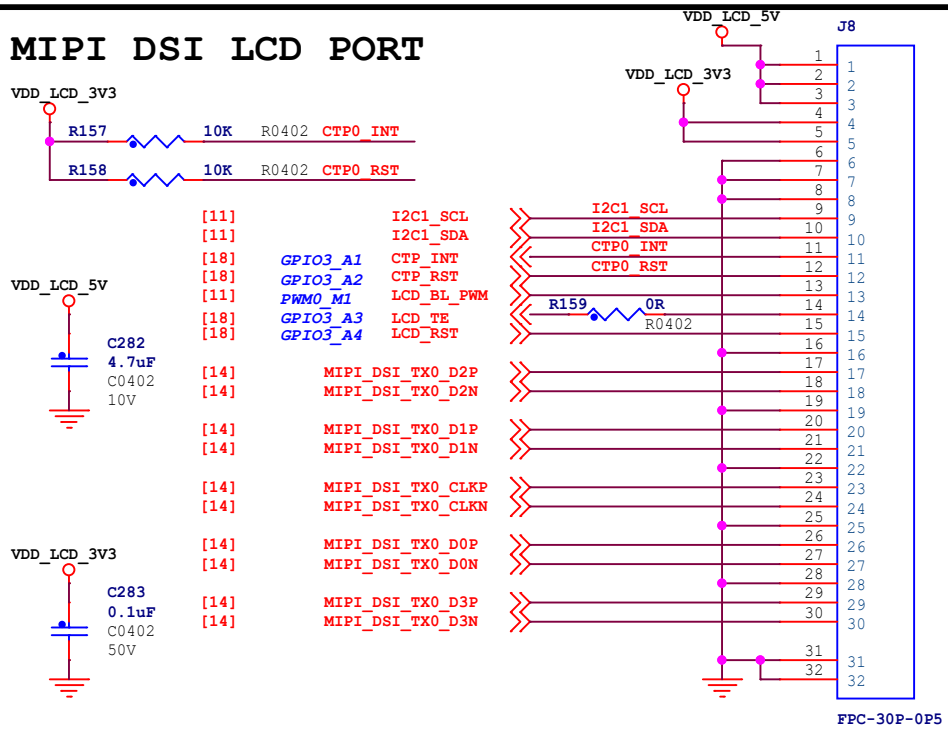
东莞野火电子有限公司 https://yehuosm.taobao.com		
Title 野火_RK3566 LubanCat 1 N_原理图		
Size A3	Document Number JL2101-N040C	Rev V1.0
Date Monday, December 12, 2022	Sheet 23	of 26

LAN RTL8111H

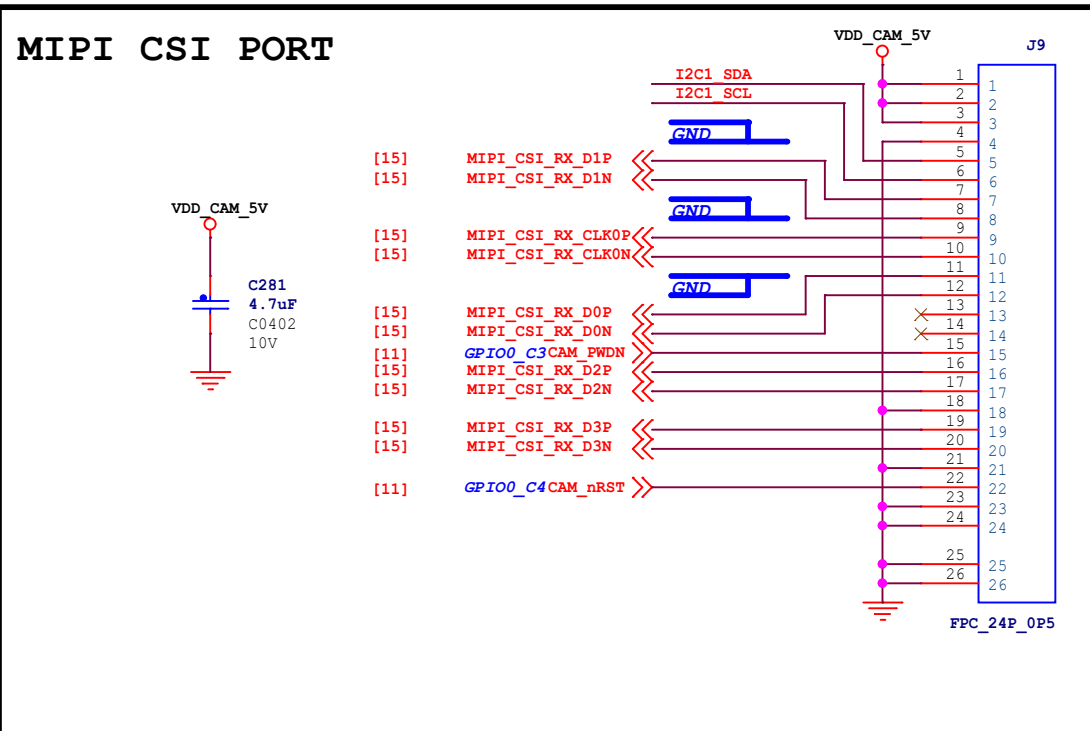


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Title 野火_RK3566 LubanCat 1 N_原理图		
Size A4	Document Number LAN_RTL8111H	Rev V1.0
Date: Monday, December 12, 2022 Sheet 24 of 26		

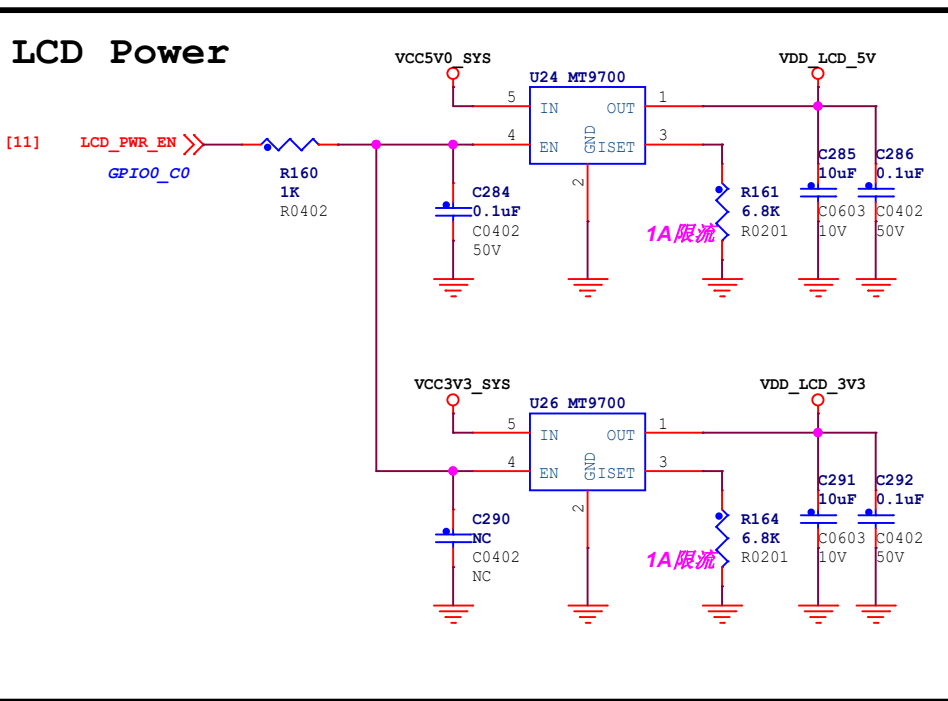
MIPI DSI LCD PORT



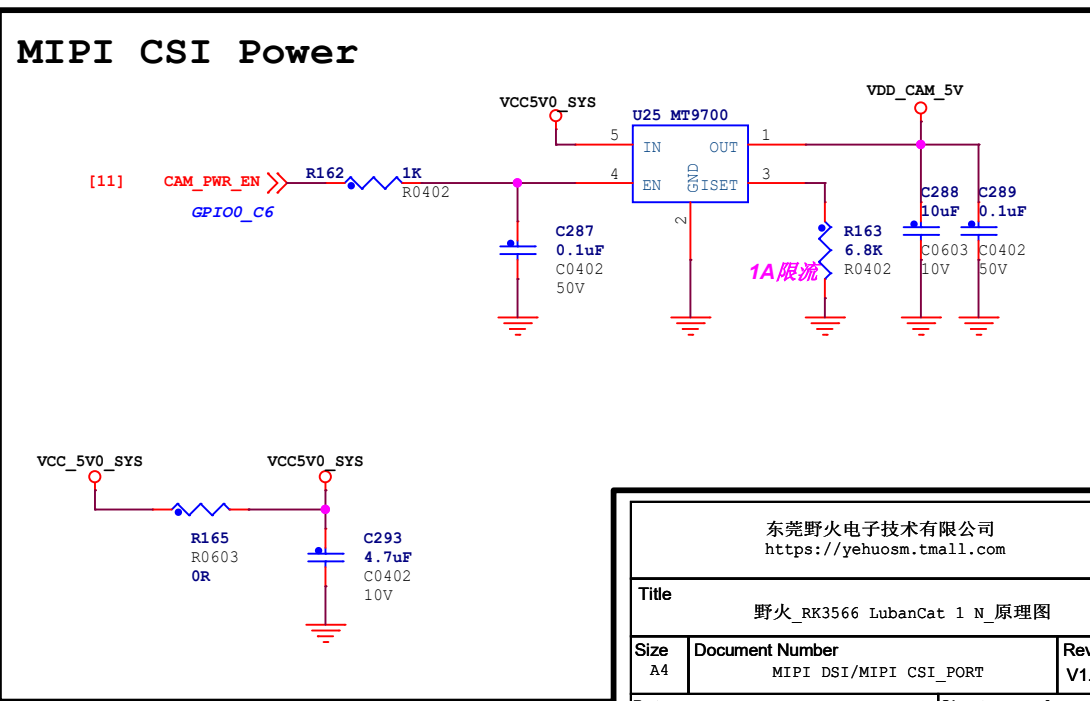
MIPI CSI PORT



LCD Power



MIPI CSI Power

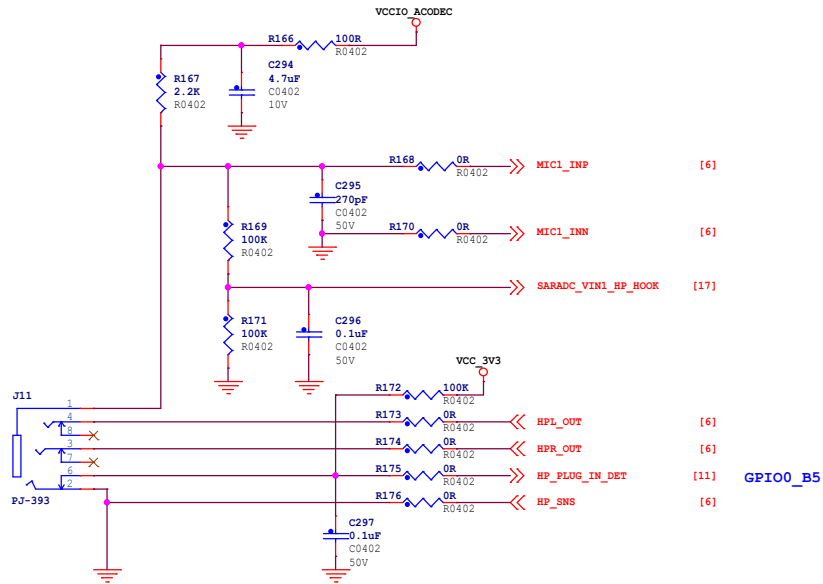


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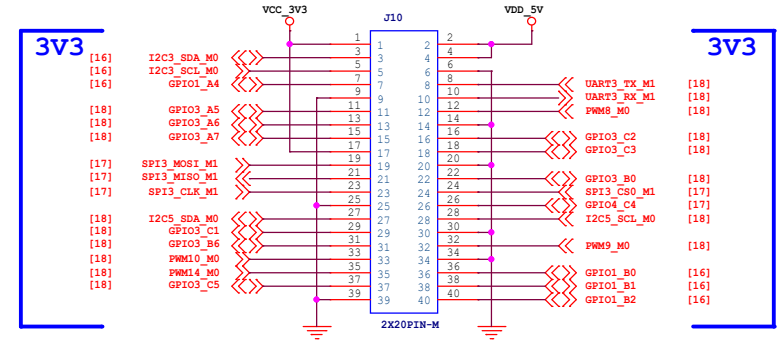
Title: 野火_RK3566 LubanCat 1 N_原理图

Size: A4	Document Number: MIPI DSI/MIPI CSI_PORT	Rev: V1.0
Date: Monday, December 12, 2022	Sheet 25 of 26	

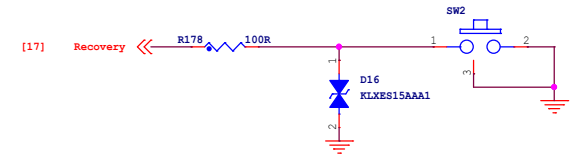
Earphone



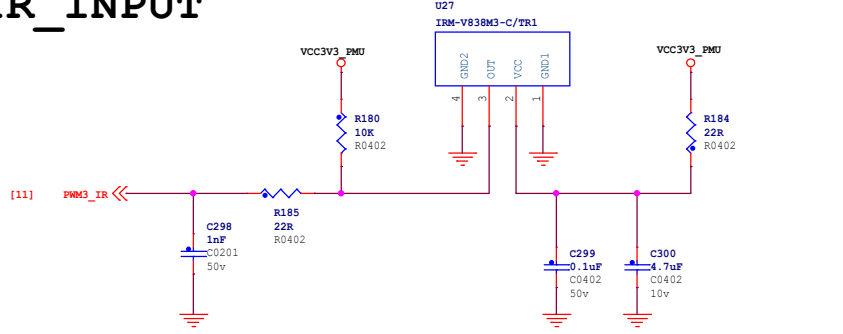
Pin Out



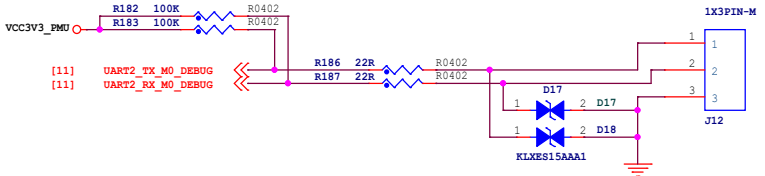
REC KEY



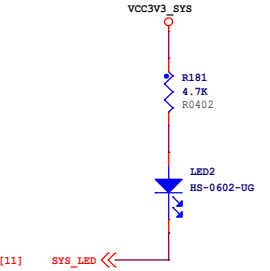
IR_INPUT



Debug UART2



SYS_LED



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Title	野火_RK3566 LubanCat 1 N 原理图	
Size	Document Number	Rev
A3	DEBUG/KEY/LED/IR_IN/PIN_OUT	V1.0
Date:	Monday, December 12, 2022	Sheet 26 of 26