

野火_RK3566 LUBANCAT_1_原理图

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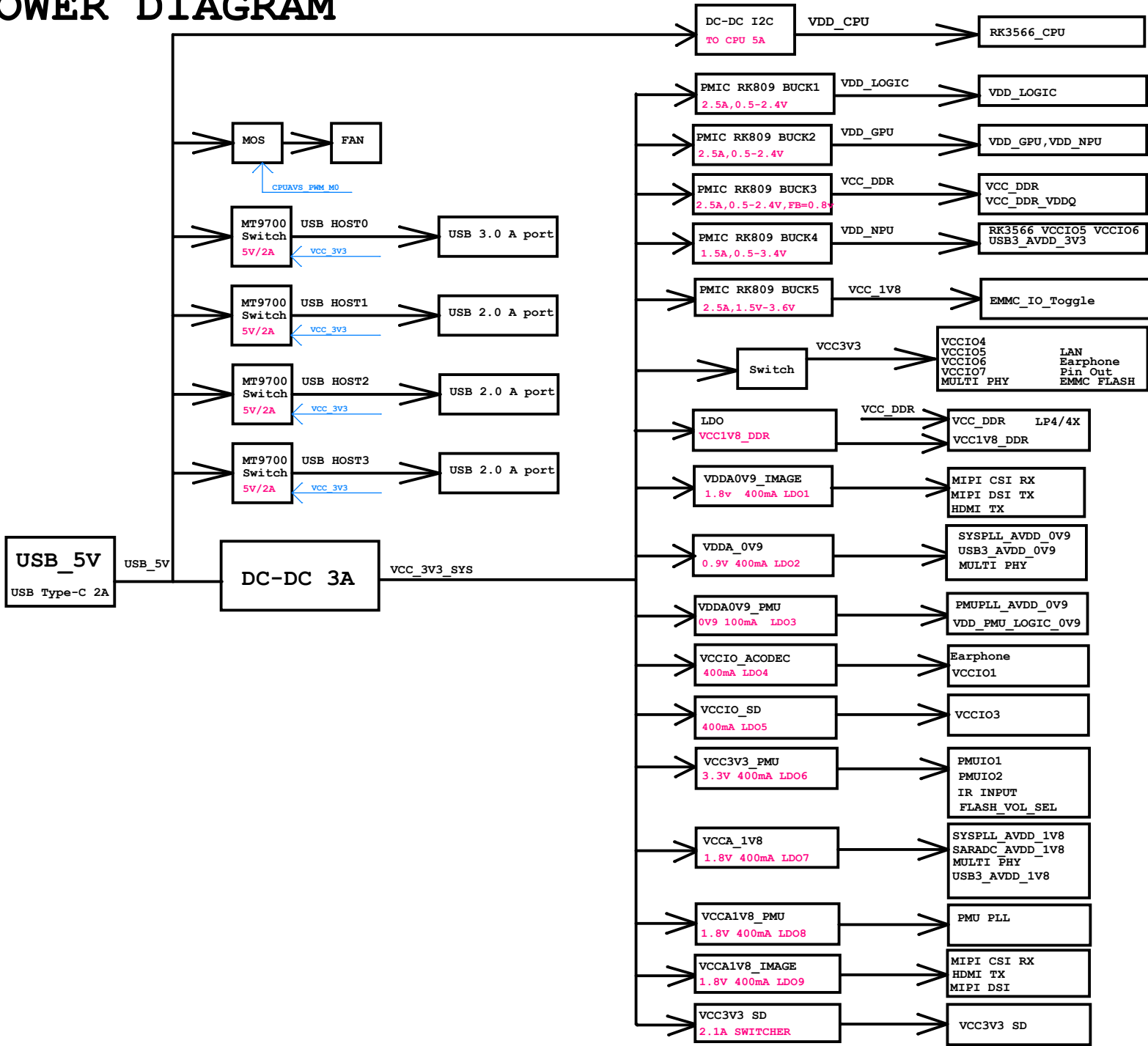
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历史版本

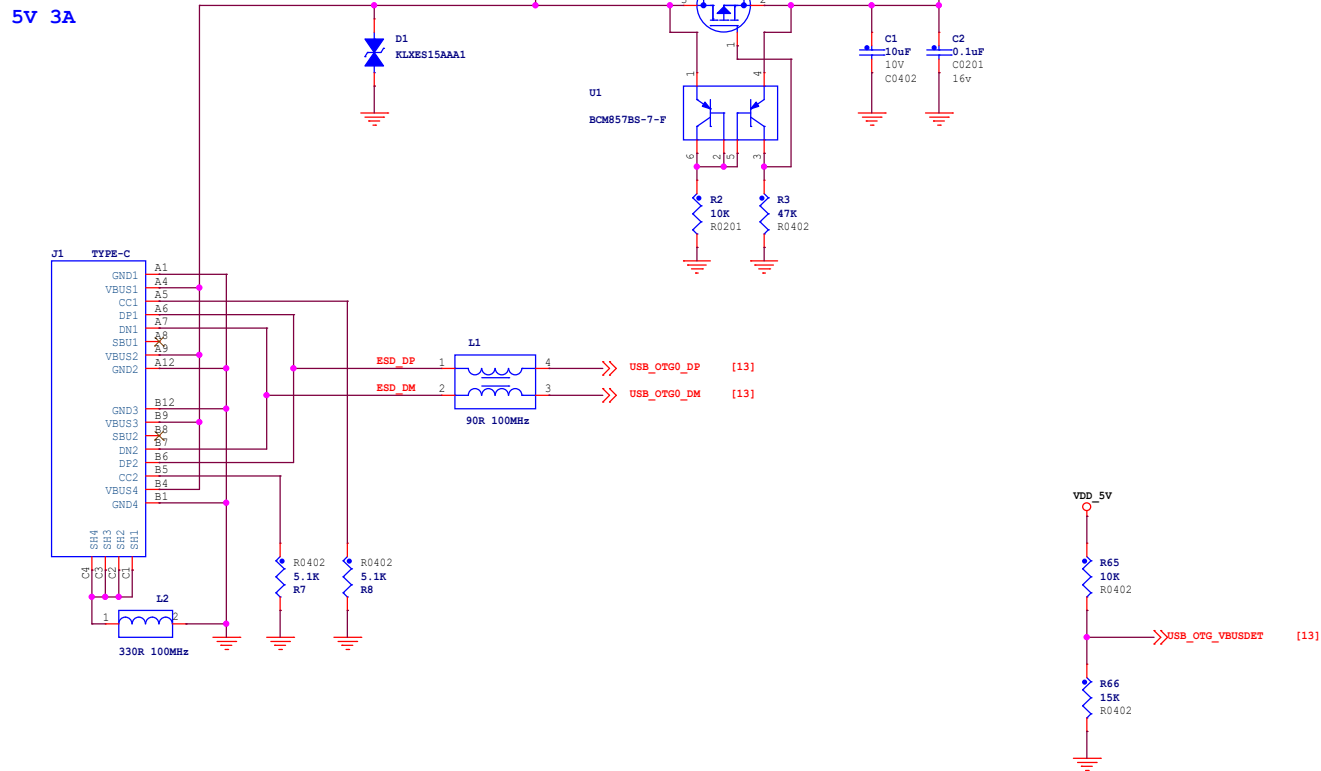
版本号	日期	设计	描述
V0.1	2022-03-18	ghs	初始版本
V1.0	2022-12-12	ghs	修正PHY芯片的RST引脚复位电平不匹配问题
V1.1	2023-04-17	ghs	新增一个BTB的2lane 的mipi csi接口
V2R2	2023-03-09	ghs	将两个MIPI CSI接口的连接器更换为BTB类型，mini PCIE接口处增加钽电容保证稳定性
V2R3	2023-03-22	ghs	由于PMIC内置RTC电路功耗大，由此停用内置的RTC电路，增加外挂RTC模块电路并增加了RTC_INT唤醒的电路与器件

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Title			
野火_RK3566 LUBANCAT_1_原理图			
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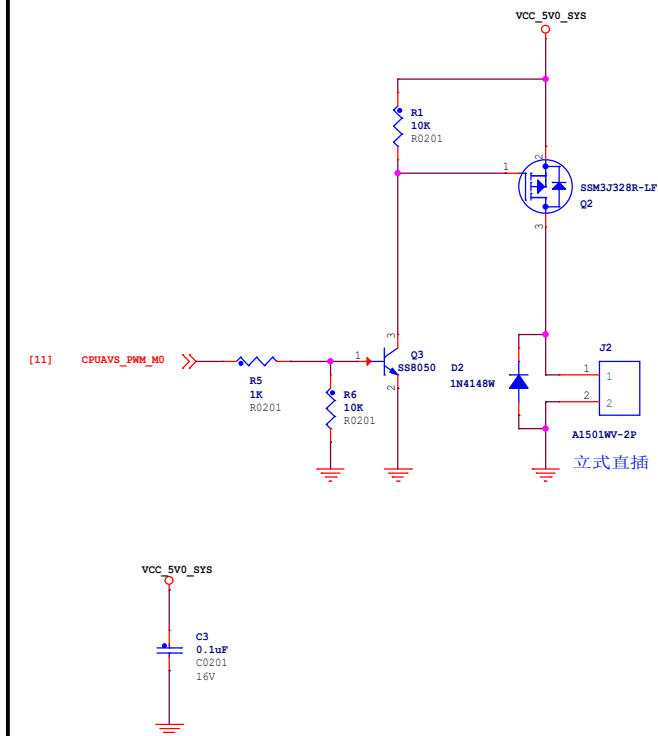
POWER DIAGRAM



POWER IN

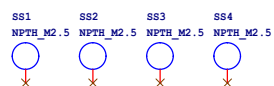


Active Cooling

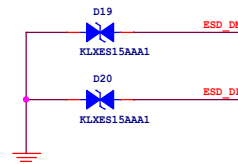


机械定位孔

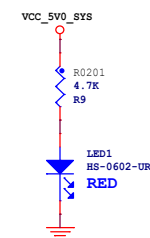
4*M3



USB ESD



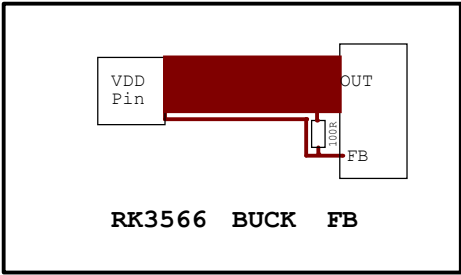
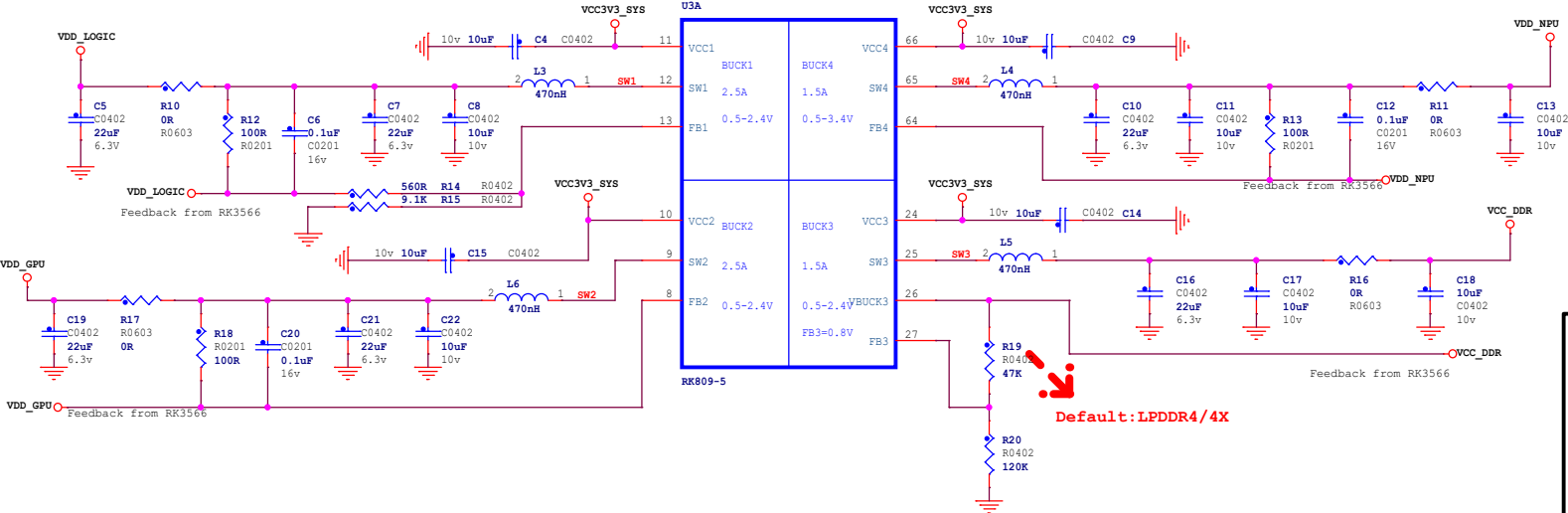
PWR_LED



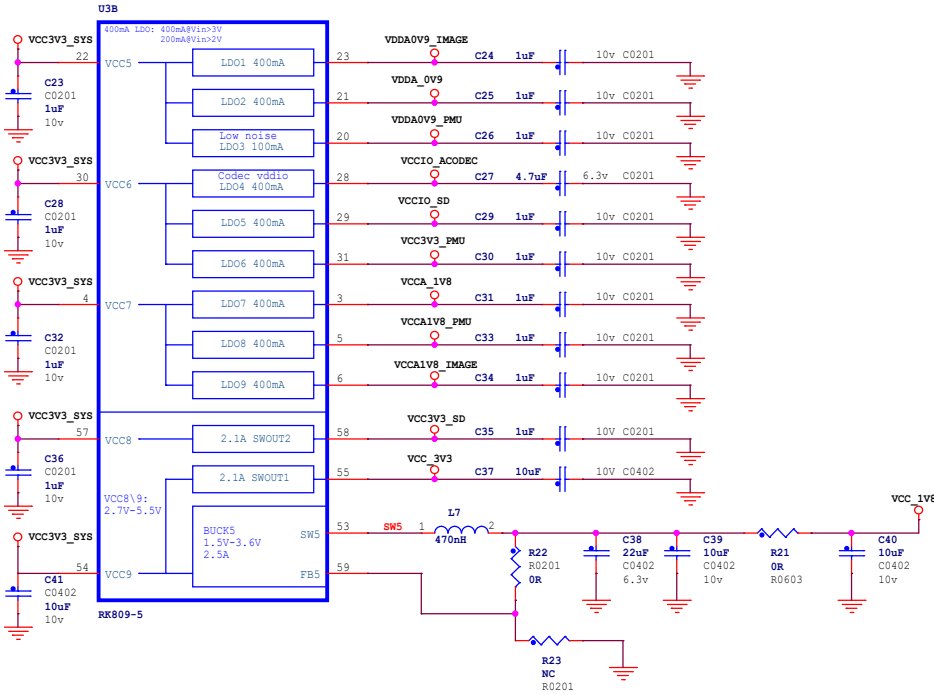
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PMIC RK809 DCDC

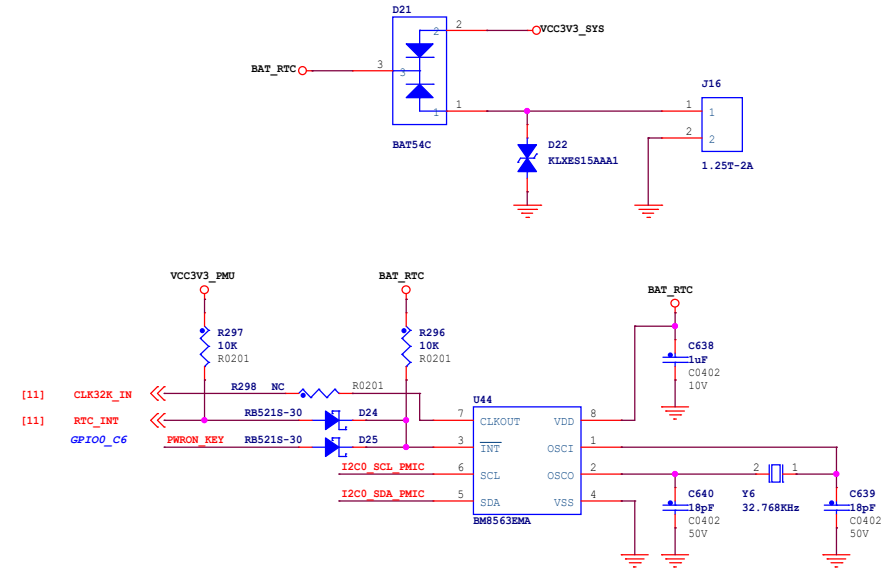
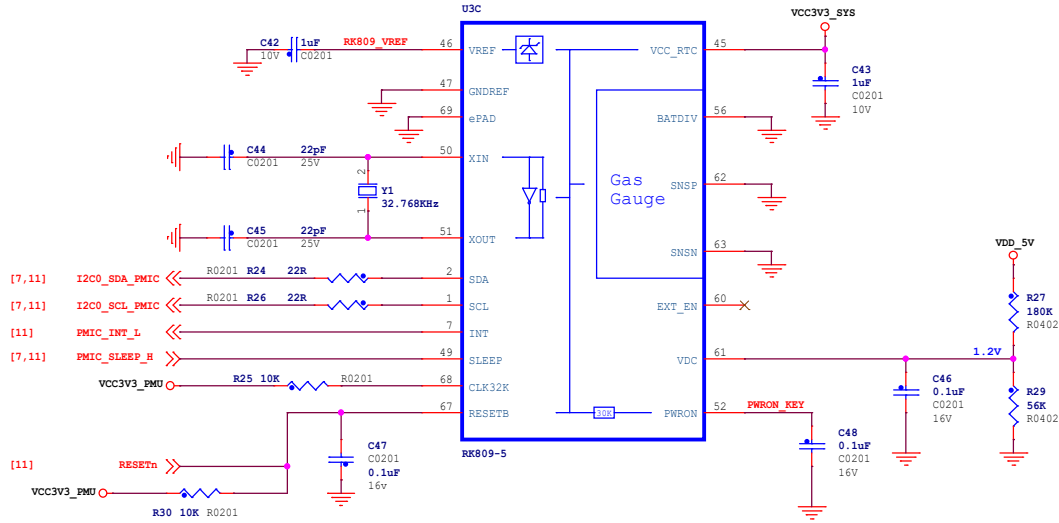


PMIC RK809 LDO

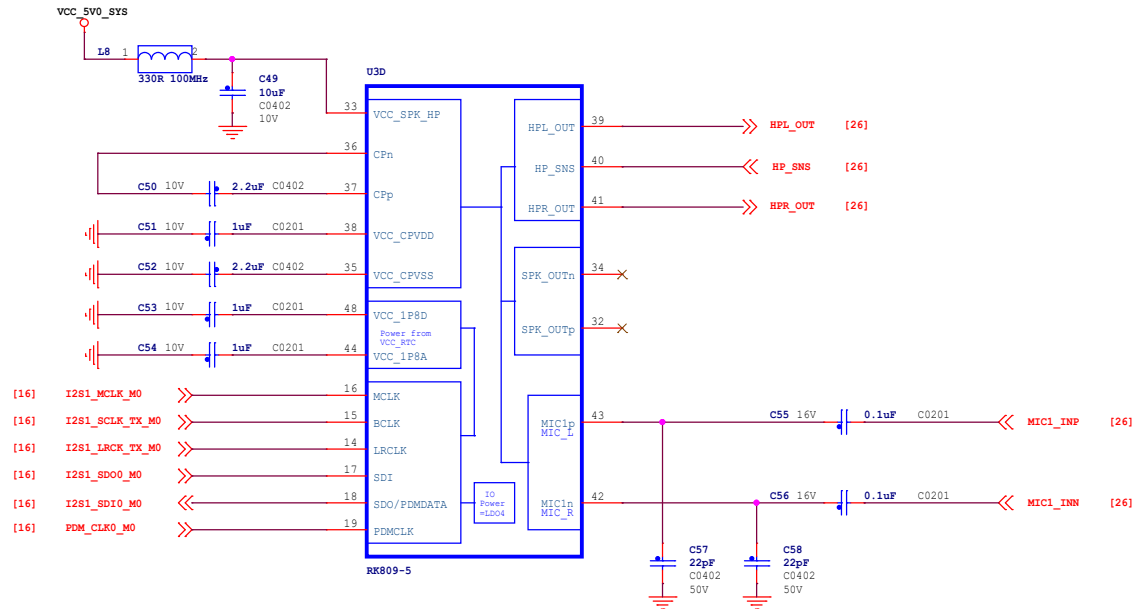


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A3	PMIC_DCDC/LDO	V2R3
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PMIC RK809 Managerment

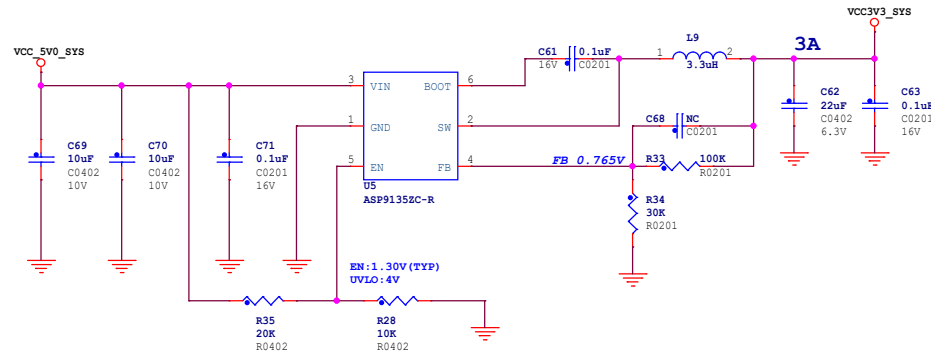


PMIC RK809 CODEC



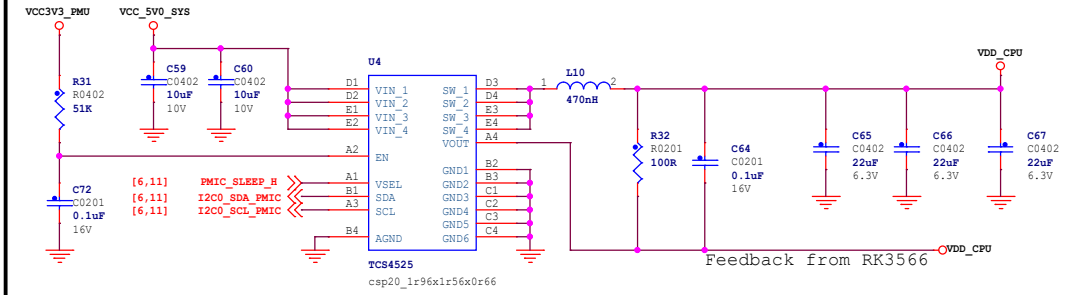
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SYS_Power



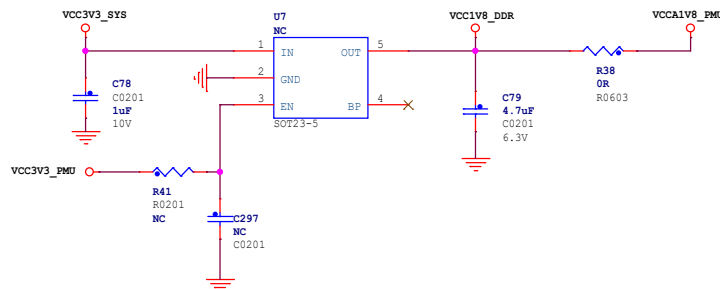
RK3566 CPU Power

VDD_CPU_EXT



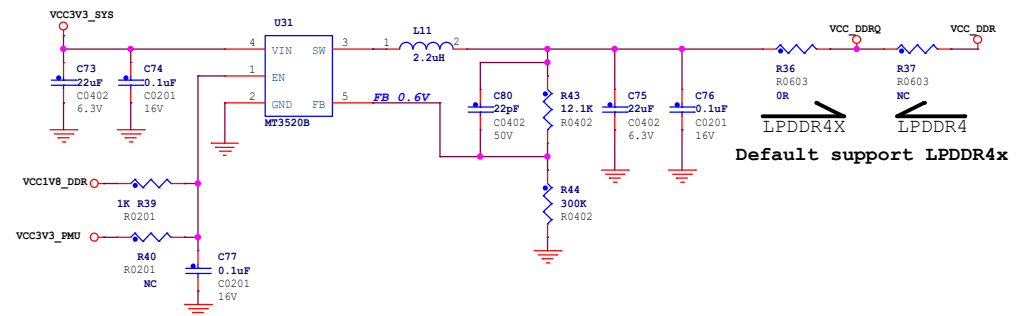
Auxiliary power supply

LPDDR4_VCC1V8_DDR



LPDDR4X Power

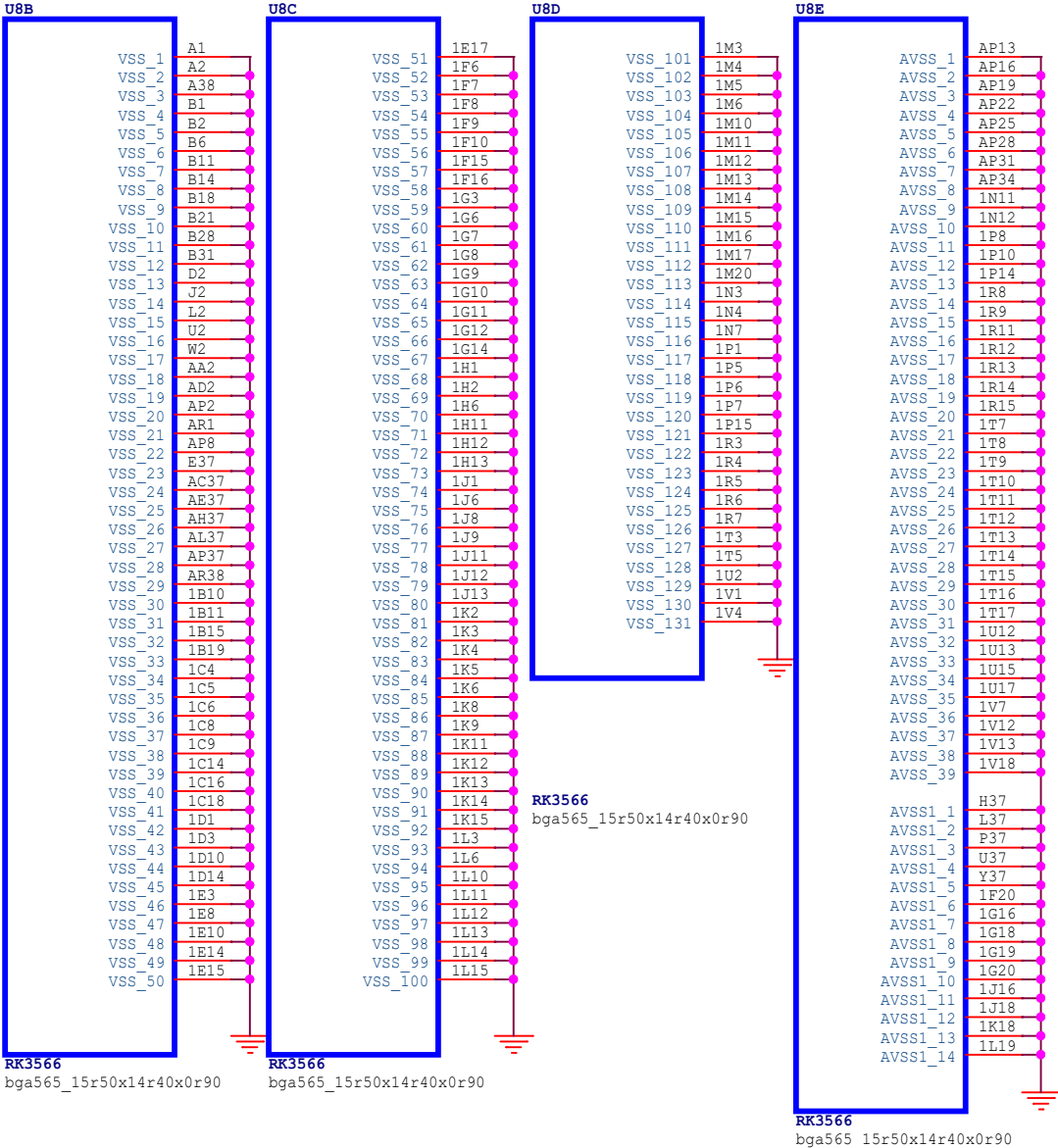
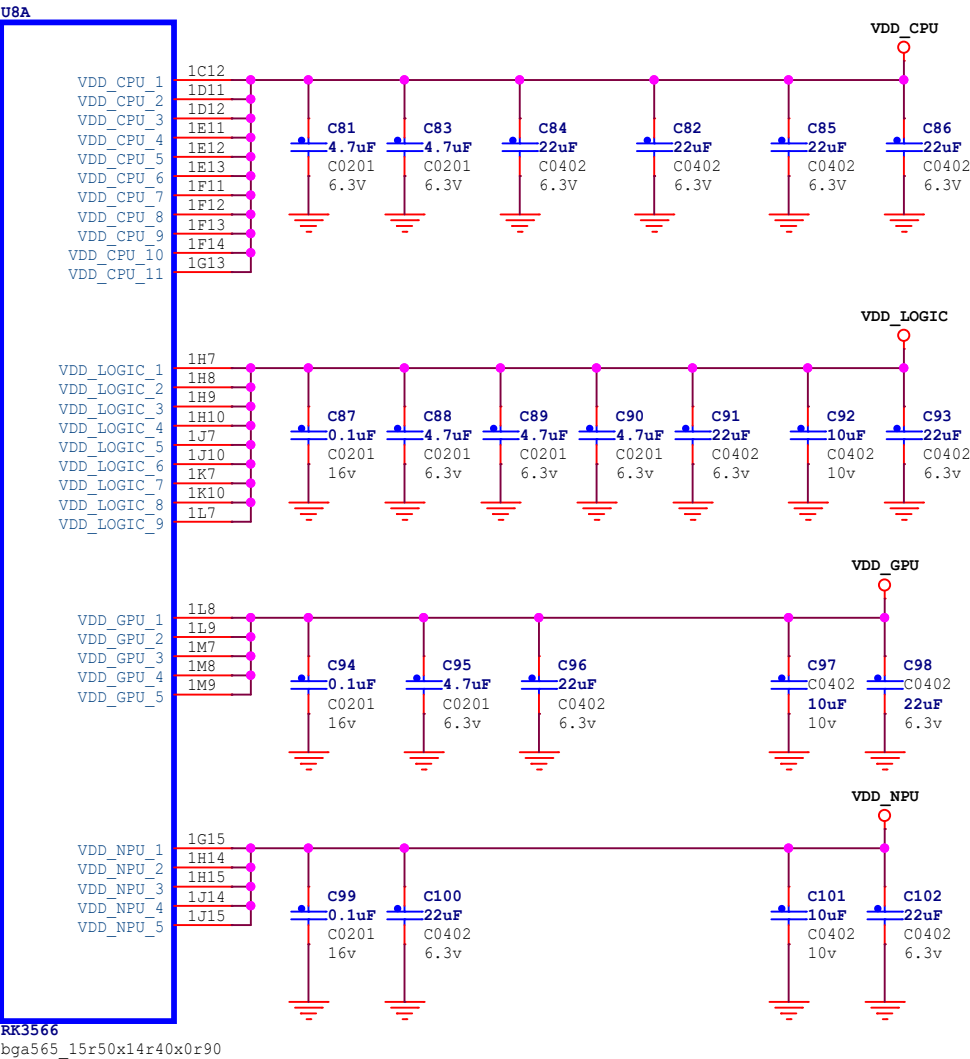
output: 0.6V



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RK3566_ABCDE

(Power&GND)



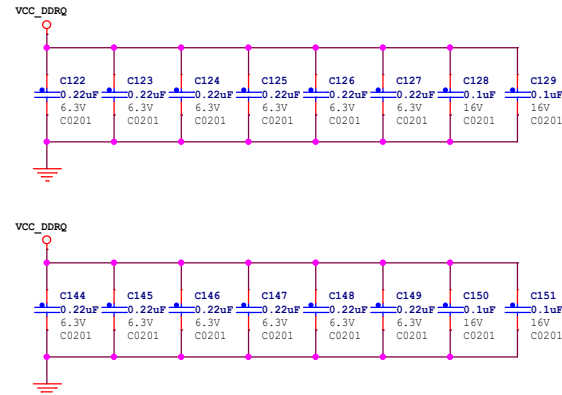
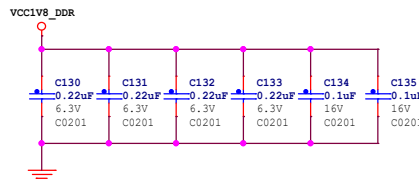
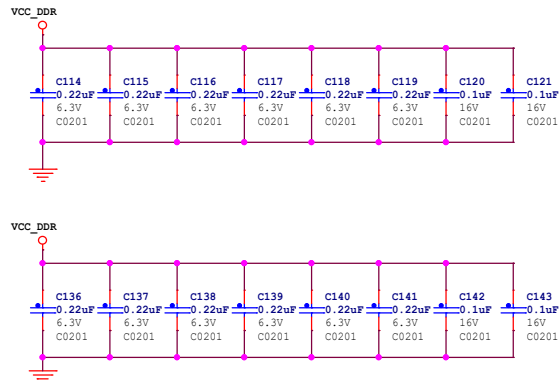
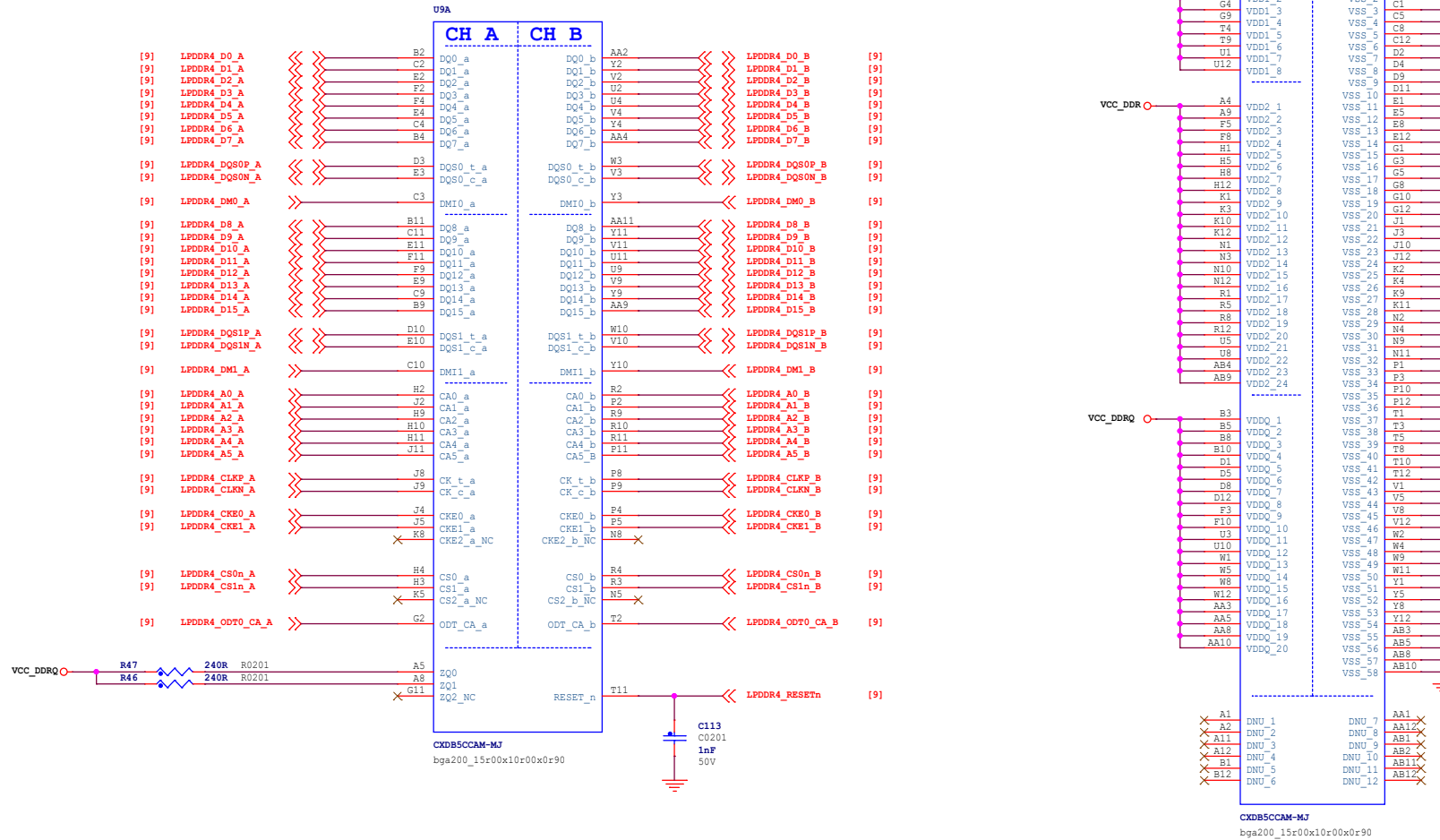
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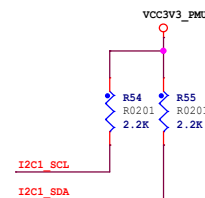
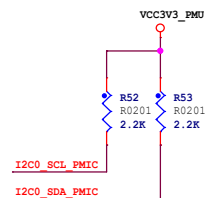
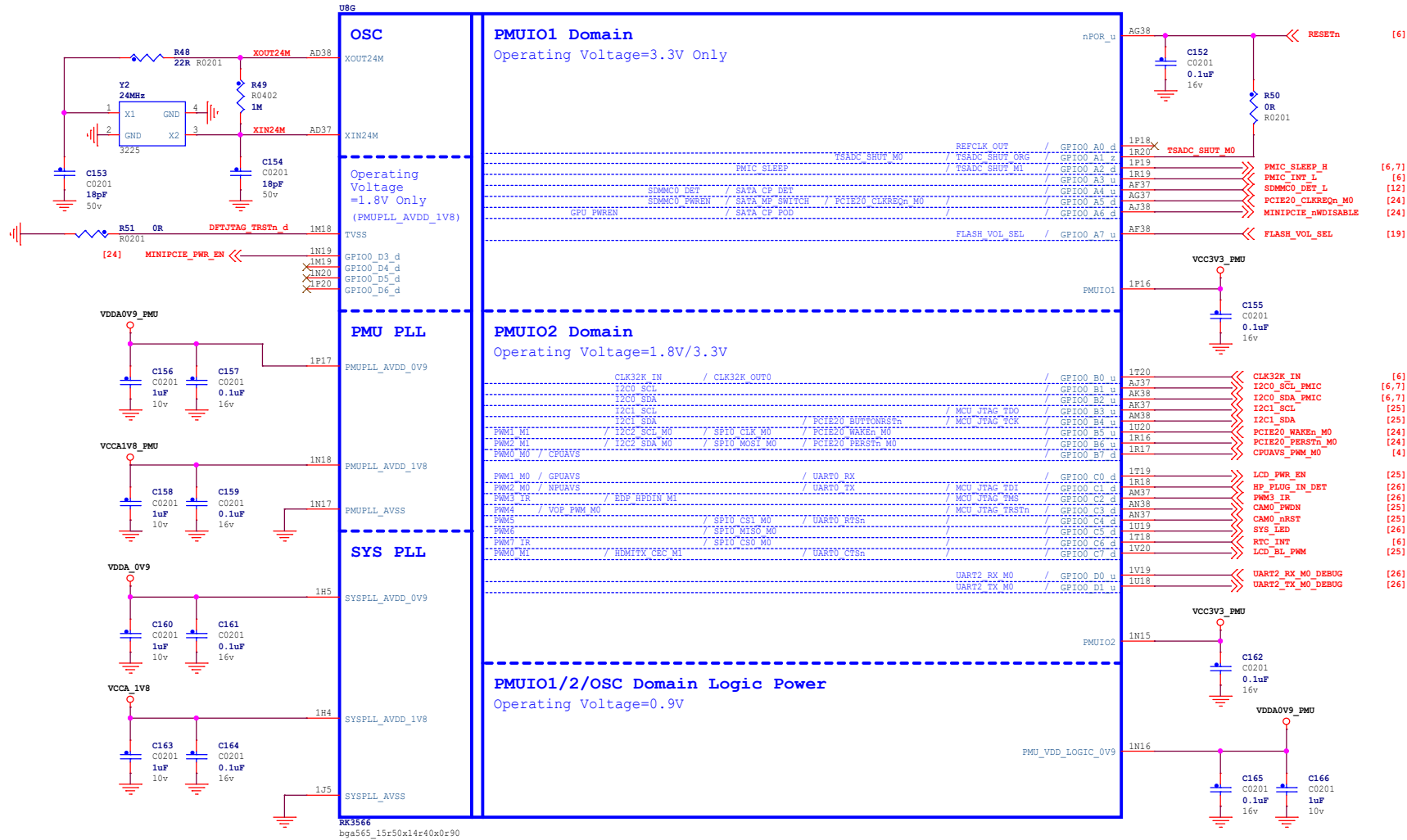


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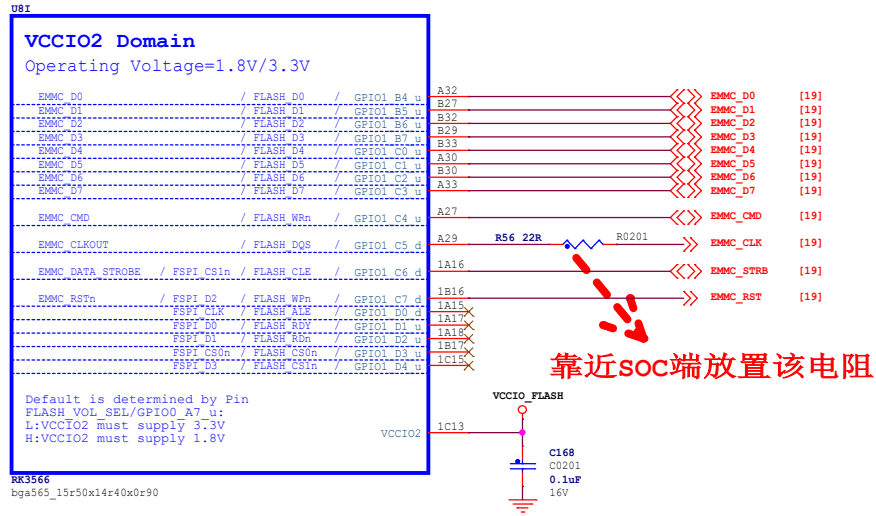
LPDDR4/4X



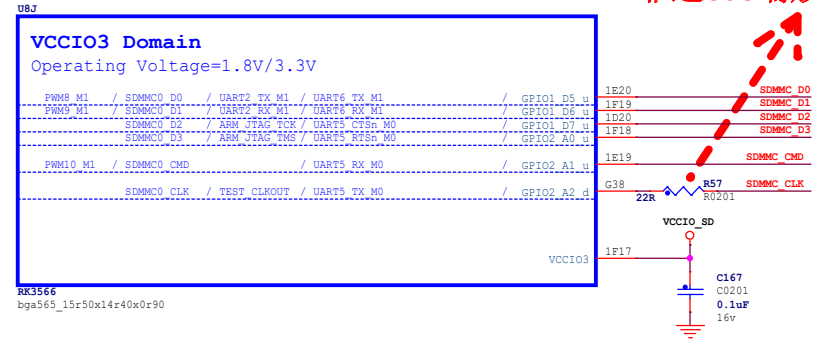
RK3566_G (OSC/PLL/PMUIO1/2)



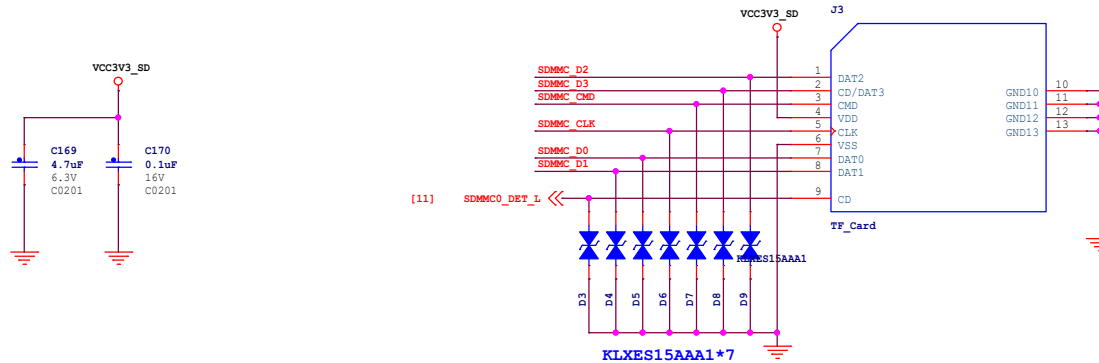
RK3566_I (VCCIO2 Domain) EMMC_IO



RK3566_J (VCCIO3 Domain) SDMMC_IO

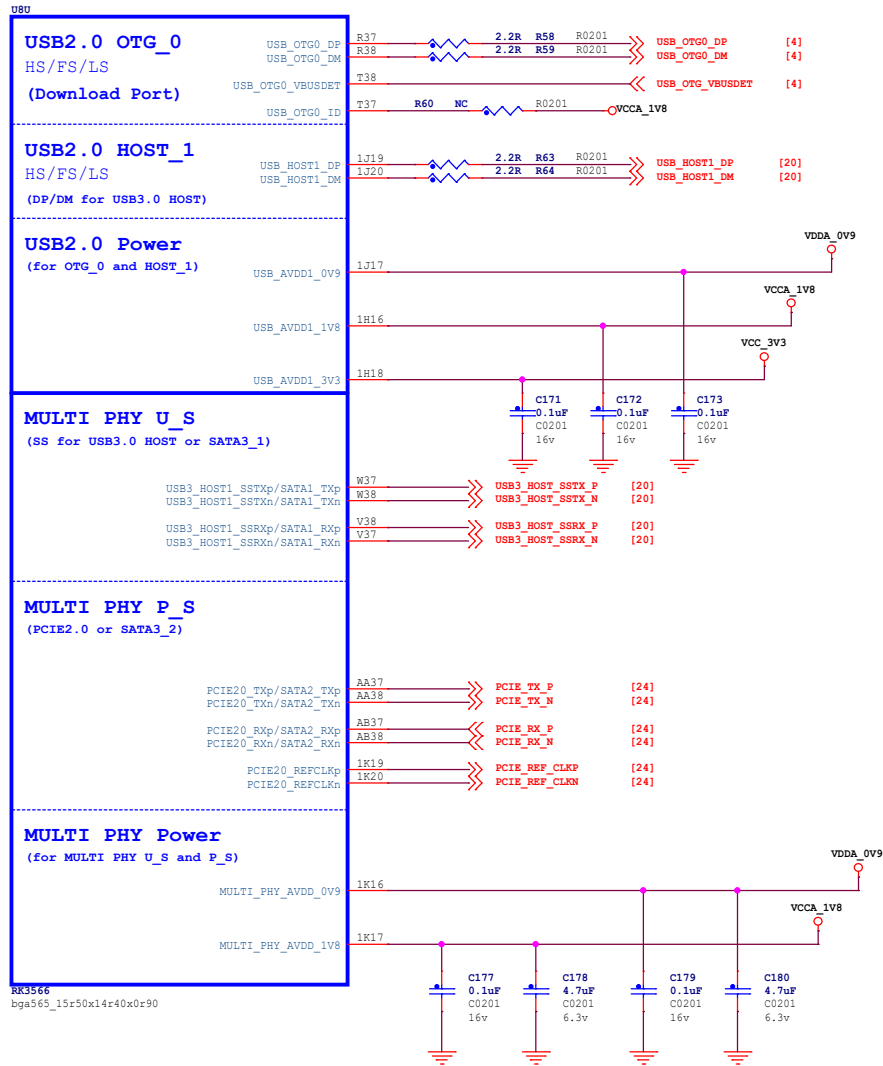


TF_CARD

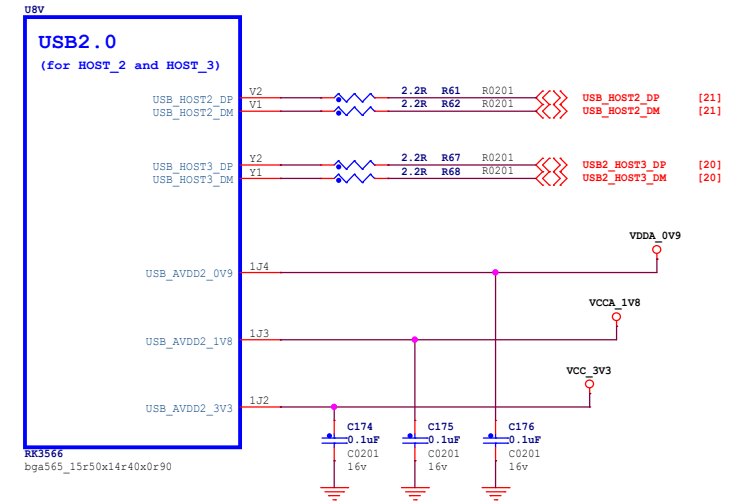


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RK3566_U (USB3.0/SATA/PCIE2.0 x1)



RK3566_V (USB2.0 HOST)

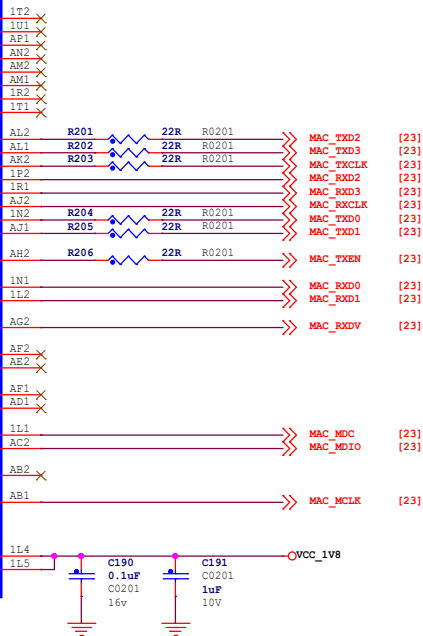


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VCCIO6 Domain										
Operating Voltage=1.8V/3.3V										
CIF D0	/	EBG SDD00	/	SDMMC2 D0 M0	/	I2S1 MCLK M1	/	VOP BT656 D0 M1	/	GPIO3 C6 d
CIF D1	/	EBG SDD01	/	SDMMC2 D1 M0	/	I2S1 SCLK TX M1	/	VOP BT656 D1 M1	/	GPIO3 C7 d
CIF D2	/	EBG SDD02	/	SDMMC2 D2 M0	/	I2S1 LCLK TX M1	/	VOP BT656 D2 M1	/	GPIO3 D0
CIF D3	/	EBG SDD03	/	SDMMC2 D3 M1	/	I2S1 SDIOV M1	/	VOP BT656 D3 M1	/	GPIO3 D1 d
CIF D4	/	EBG SDD04	/	SDMMC2 CMD M0	/	I2S1 SDIO M1	/	VOP BT656 D4 M1	/	GPIO3 D2 d
CIF D5	/	EBG SDD05	/	SDMMC2 CLK M0	/	I2S1 S0B1 M1	/	VOP BT656 D5 M1	/	GPIO3 D3 d
CIF D6	/	EBG SDD06	/	SDMMC2 CS0 M0	/	I2S1 S0B2 M1	/	VOP BT656 D6 M1	/	GPIO3 D4 d
CIF D7	/	EBG SDD07	/	SDMMC2 PARKED M0	/	I2S1 S0B3 M1	/	VOP BT656 D7 M1	/	GPIO3 D5 d
CIF D8	/	EBG SDD08	/	GMAC1 TXD2 M1	/	UART1 TX M1	/	PD0 CLK0 M1	/	GPIO3 D6 d
CIF D9	/	EBG SDD09	/	GMAC1 TXD3 M1	/	UART1 RX M1	/	PD0 SDIO M1	/	GPIO3 D7 d
CIF D10	/	EBG SDD010	/	GMAC1 TXCLK M1	/	PD0 CLRI M1	/	PD0 CLRI M1	/	GPIO4 A0 d
CIF D11	/	EBG SDD011	/	GMAC1 TXD0 M1	/	PD0 S0B1 M1	/	PD0 S0B1 M1	/	GPIO4 A1 d
CIF D12	/	EBG SDD012	/	GMAC1 TXD1 M1	/	UART4 TX M2	/	PD0 S0B2 M1	/	GPIO4 A2 d
CIF D13	/	EBG SDD013	/	GMAC1 RXCLK M1	/	UART4 RX M2	/	PD0 S0B3 M1	/	GPIO4 A3 d
CIF D14	/	EBG SDD014	/	GMAC1 RXD0 M1	/	UART9 TX M2	/	I2S2 LCLK TX M1	/	GPIO4 A4 d
CIF D15	/	EBG SDD015	/	GMAC1 RXD1 M1	/	UART9 RX M2	/	I2S2 LCLK RX M1	/	GPIO4 A5 d
ISP FLASHTRIGOUT	/	EBG SDCE0	/	GMAC1 RXEN M1	/	SP13 CS0 M0	/	I2S1 SCLK RX M1	/	GPIO4 A6 h
CAM CLKOUT0	/	EBG SDCE1	/	GMAC1 RXD0 M1	/	SP13 CS1 M0	/	I2S1 LCLK RX M1	/	GPIO4 A7 d
CAM CLKOUT1	/	EBG SDCE2	/	GMAC1 RXD1 M1	/	SP13 MISO M0	/	I2S1 SDIO M1	/	GPIO4 B0 d
ISP PRELIGHT TRIG	/	EBG SDCE3	/	GMAC1 RXDV CRS M1	/		/	I2S1 SDIO2 M1	/	GPIO4 B1 d
I2C0 SDA M0	/	EBG VCOM	/	GMAC1 RXER M1	/	SP13 MOSI M0	/	I2S2 SDI M1	/	GPIO4 B2 d
I2C4 SCL M0	/	EBG GROE	/	EW41 REFCLK0 ZSW M1	/	SP13 CLK M0	/	I2S2 SDO M1	/	GPIO4 B3 d
ISP FLASH TRIGIN	/	I2C2 SDA M1	/	EBG GRDP				VOP BT656 CLK M1	/	GPIO4 B4 d
I2C2 SCL M1	/	EBG SDSHR						I2S1 SDOB M1	/	GPIO4 B5 d
CIF HREF	/	EBG SDLE	/	GMAC1 MDC M1	/	UART1 RTS0 M1	/	I2S2 MCLK M1	/	GPIO4 B6 d
CIF VSYNC	/	EBG SDOE	/	GMAC1 MDIO M1	/			I2S1 SCLK RX M1	/	GPIO4 B7 d
PWM11 IR M1	/	CIF CLKOUT	/	EBG GDCLK					/	GPIO4 C0 d
CIF CLAIN	/	EBG SDCLK	/	GMAC1 MCLKINOUT M1	/	UART1 CTS0 M1	/	I2S2 SCLK RX M1	/	GPIO4 C1 d

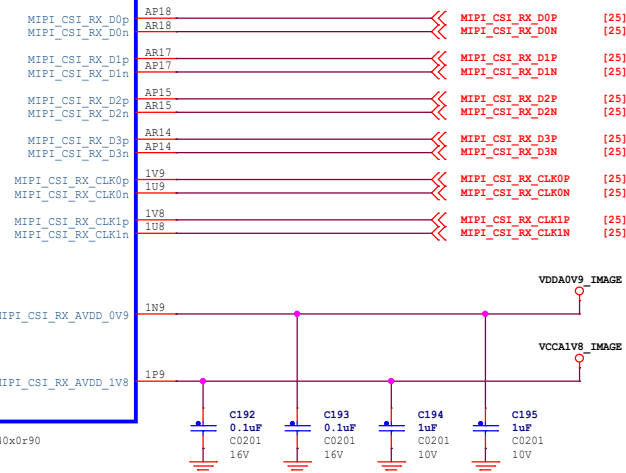
VCCIO6 1
VCCIO6 2



```

MIPI_CSI_RX_D0p
MIPI_CSI_RX_D0n
MIPI_CSI_RX_D1p
MIPI_CSI_RX_D1n
MIPI_CSI_RX_D2p
MIPI_CSI_RX_D2n
MIPI_CSI_RX_D3p
MIPI_CSI_RX_D3n
MIPI_CSI_RX_CLK0p
MIPI_CSI_RX_CLK0n
MIPI_CSI_RX_CLK1p
MIPI_CSI_RX_CLK1n
MIPI_CSI_RX_AVDD_0V9
MIPI_CSI_RX_AVDD_1V8

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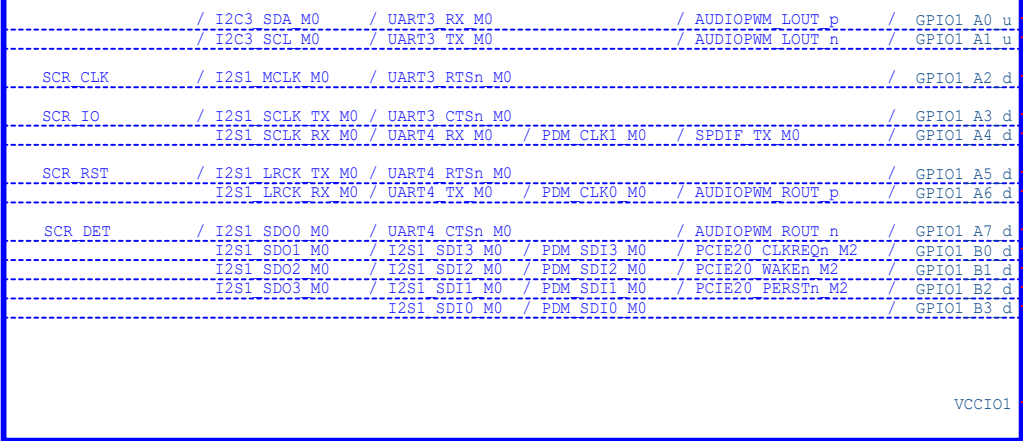
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A3	MIPI_CSI/GMAC_Controller	V2R3
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RK3566_H (VCCIO1 Domain)

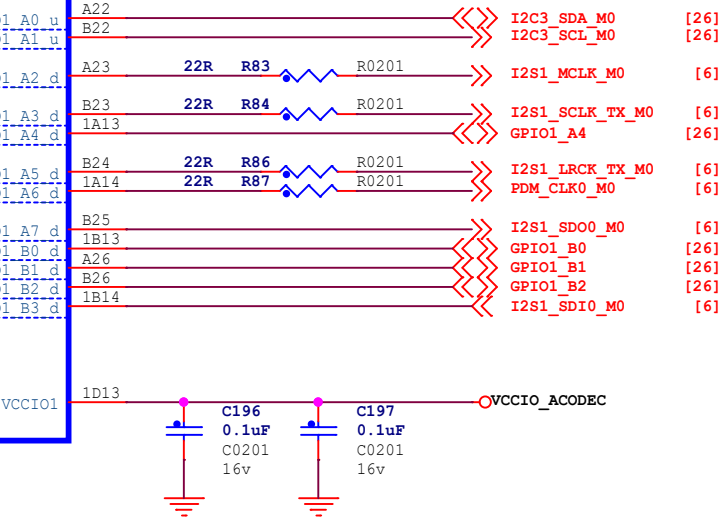
U8H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V



RK3566
bga565_15r50x14r40x0r90



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RK3566_K (VCCIO4 Domain)

USB

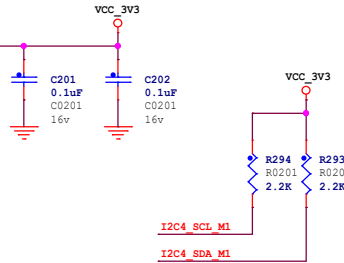
VCCIO4 Domain

Operating Voltage=1.8V/3.3V

UART6_RX_M0	/ SDMMC1_D0	/ GPIO2_A3_U	1C19		
UART6_TX_M0	/ SDMMC1_D1	/ GPIO2_A4_U	1E18		
UART7_RX_M0	/ SDMMC1_D2	/ GPIO2_A5_U	1D18		
UART7_TX_M0	/ SDMMC1_D3	/ GPIO2_A6_U	1A20		
UART9_RX_M0	/ SDMMC1_CMD	/ GPIO2_A7_U	B35	MAC_INT	[23]
UART9_TX_M0	/ SDMMC1_CLK	/ GPIO2_B0_d	B37	MAC_RST	[23]
UART8_RTSn_M0	/ I2C4_SDA_M1	/ SDMMC1_PWREN	A35	I2C4_SDA_M1	[25]
UART8_CTSn_M0	/ I2C4_SCL_M1	/ SDMMC1_DET	B34	I2C4_SCL_M1	[25]
UART6_RTSn_M0	/ SPI1_MOSI_M0	/ UART1_RX_M0	1C20	CAMI_PWDN	[25]
UART6_CTSn_M0	/ SPI1_MISO_M0	/ UART1_TX_M0	F38	CAMI_nRST	[25]
UART7_RTSn_M0	/ SPI2_MOSI_M0	/ UART1_RTSn_M0	F37	USB30_HOST_EN	[20]
UART7_CTSn_M0	/ SPI2_MISO_M0	/ UART1_CTSn_M0	G37	USB20_HOST_EN	[21]
UART8_RTSn_M0	/ SPI1_MOSI_M0	/ I2S2_SCLK_RX_M0	D38		
UART8_CTSn_M0	/ SPI1_MISO_M0	/ I2S2_SCLK_TX_M0	A37		
UART9_RTSn_M0	/ SPI2_MOSI_M0	/ I2S2_LCKn_TX_M0	B36		
UART9_CTSn_M0	/ SPI2_MISO_M0	/ I2S2_SDO_M0	C37		
UART6_RTSn_M0	/ SPI1_MOSI_M0	/ I2S2_SDO_M0	1D19		
UART6_CTSn_M0	/ SPI1_MISO_M0	/ I2S2_SDI_M0	1B20		
UART7_RTSn_M0	/ SPI2_MOSI_M0	/ I2S2_SDI_M0	D37		
UART7_CTSn_M0	/ SPI2_MISO_M0	/ CLK32K_OUT1	B38		

RK3566
bga565_15r50x14r40x0r90

VCCIO4



RK3566_O (SARADC/OTP)

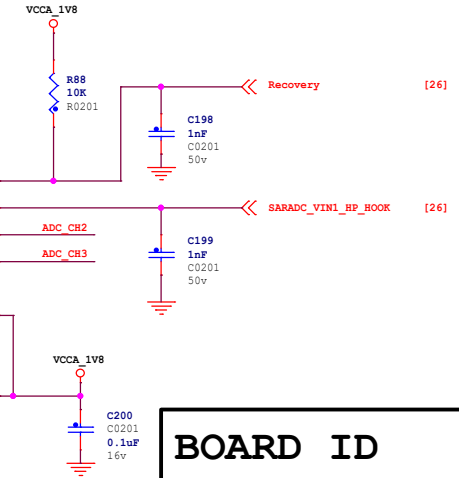
USB

SARADC

Recovery/

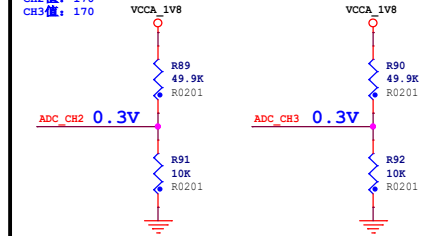
OTP

RK3566
bga565_15r50x14r40x0r90



BOARD ID

BOARD ID:01
CH2值: 170
CH3值: 170



RK3566_N (VCCIO7 Domain)

USB

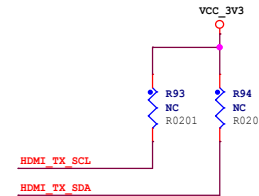
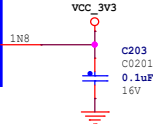
VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PM14_M1	/ SPI3_CLK_M1	/ I2S3_MCLK_M1	1U7	SPI3_CLK_M1	[26]
PM14_TX_M1	/ SPI3_MOSI_M1	/ I2S3_SCLK_M1	AP12	SPI3_MOSI_M1	[26]
PM14_RX_M1	/ SPI3_MISO_M1	/ I2S3_LCKn_M1	1V6	GPIO4_C4	[26]
PM14_TX_M1	/ SPI3_CS0_M1	/ I2S3_SDO_M1	1U6	SPI3_MISO_M1	[26]
PM14_RX_M1	/ SPI3_CS0_M1	/ I2S3_SDI_M1	1T6	SPI3_CS0_M1	[26]
HDMI_TX_SCL	/ I2C5_SCL_M1	/ GPIO4_C7_U	AR12	HDMI_TX_SCL	[22]
HDMI_TX_SDA	/ I2C5_SDA_M1	/ GPIO4_D0_U	AP11	HDMI_TX_SDA	[22]
HDMI_TX_CEC	/ SPI3_CS1_M1	/ GPIO4_D1_U	1V5	HDMI_TX_CEC	[22]

RK3566
bga565_15r50x14r40x0r90

VCCIO7



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RK3566_L (VCCIO5 Domain)

U8L

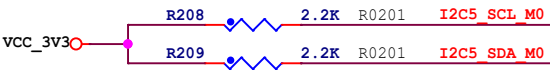
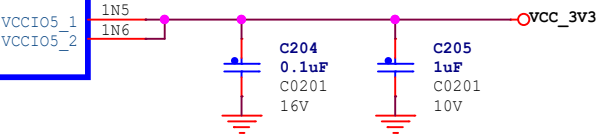
VCCIO5 Domain

Operating Voltage=1.8V/3.3V

VOP_BT1120_D0	/ SPI1_CS0_M1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D0_M1	/ GPIO3_A1_d
VOP_BT1120_D1		/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
VOP_BT1120_D2		/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
VOP_BT1120_D3		/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
VOP_BT1120_D4		/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
VOP_BT1120_D5		/ GMAC1_RXCLK_M0		/ SDMMC2_CLK_M1	/ GPIO3_A6_d
				/ SDMMC2_DET_M1	/ GPIO3_A7_d
VOP_BT1120_D6		ETH1_REFCLK0_25M_M0		SDMMC2_PWREN_M1	/ GPIO3_B0_d
PWM8_M0	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1		/ GPIO3_B1_d
PWM9_M0	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1		/ GPIO3_B2_d
VOP_BT1120_D9	/ I2C5_SCL_M0	/ GMAC1_RXDV_CRS_M0		PDM_SDI0_M2	/ GPIO3_B3_d
VOP_BT1120_D10	/ I2C5_SDA_M0	/ GMAC1_RXER_M0		PDM_SDI1_M2	/ GPIO3_B4_d
PWM10_M0	/ VOP_BT1120_D11	/ I2C3_SCL_M1	/ GMAC1_TXD0_M0		/ GPIO3_B5_d
PWM11_IR_M0	/ VOP_BT1120_D12	/ I2C3_SDA_M1	/ GMAC1_TXD1_M0		/ GPIO3_B6_d
PWM12_M0		/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
PWM13_M0		GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
VOP_BT1120_D13	/ SPI1_MOSI_M1		PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
VOP_BT1120_D14	/ SPI1_MISO_M1		/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
VOP_BT1120_D15	/ SPI1_CLK_M1		/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

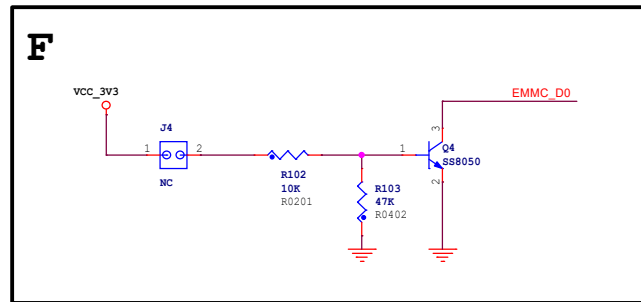
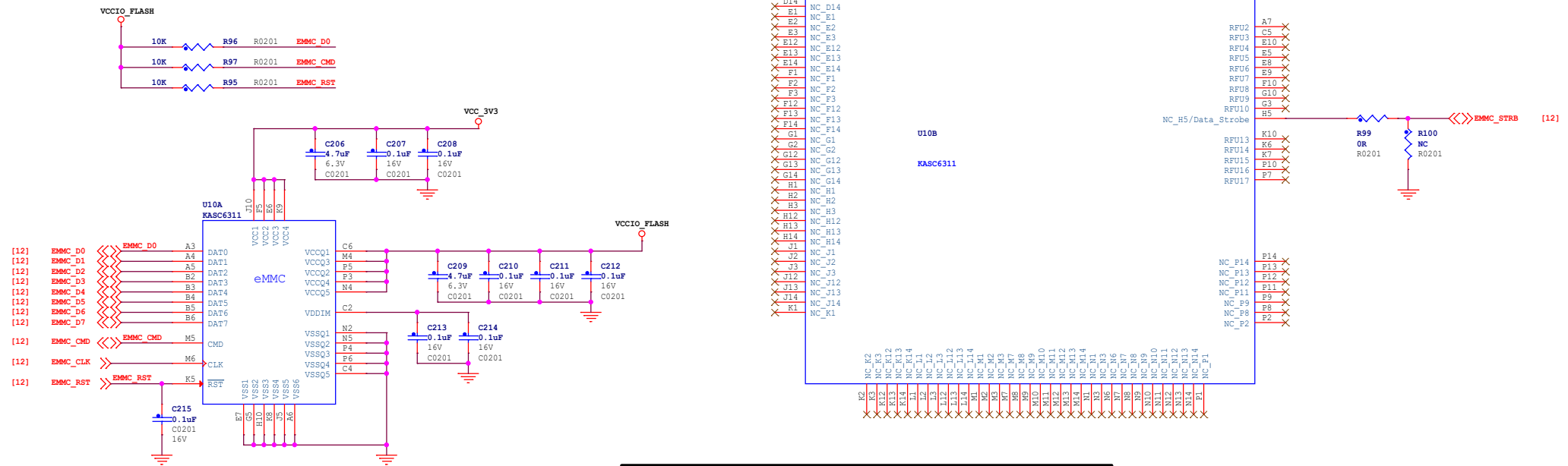
RK3566
bga565_15r50x14r40x0r90

1U5	CTP_INT	[25]
AR10	CTP_RST	[25]
AP10	LCD_TE	[25]
AR9	LCD_RST	[25]
AP9	GPIO3_A5	[26]
1U4	GPIO3_A6	[26]
1V3	GPIO3_A7	[26]
AR7	GPIO3_B0	[26]
AP7	PWM8_M0	[26]
AR6	PWM9_M0	[26]
AP6	I2C5_SCL_M0	[26]
1U3	I2C5_SDA_M0	[26]
1T4	PWM10_M0	[26]
1V2	GPIO3_B6	[26]
AP5	UART3_TX_M1	[26]
AR4	UART3_RX_M1	[26]
AP4	GPIO3_C1	[26]
AP3	GPIO3_C2	[26]
AR2	GPIO3_C3	[26]
1P3	PWM14_M0	[26]
1P4	GPIO3_C5	[26]

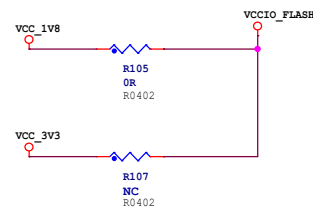


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Title 野火_RK3566 LUBANCAT_1 原理图		
Size A4	Document Number RK3566_VO Interface	Rev V2R3
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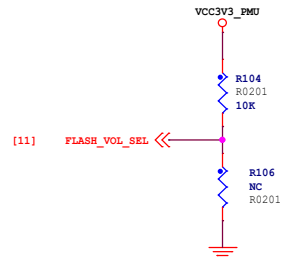
EMMC FLASH



EMMC_IO_Toggle



FLASH VOL SEL



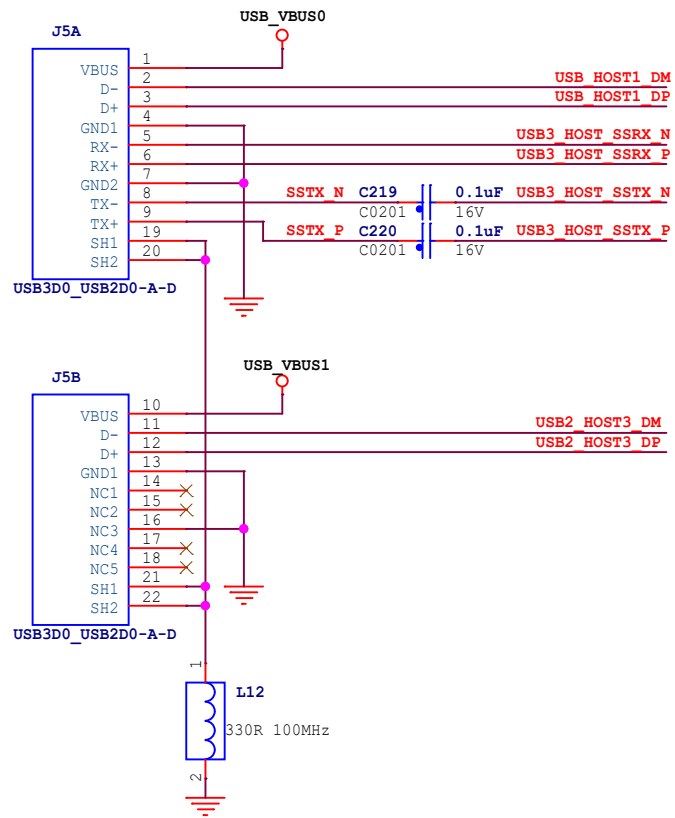
Note:

```
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven
```

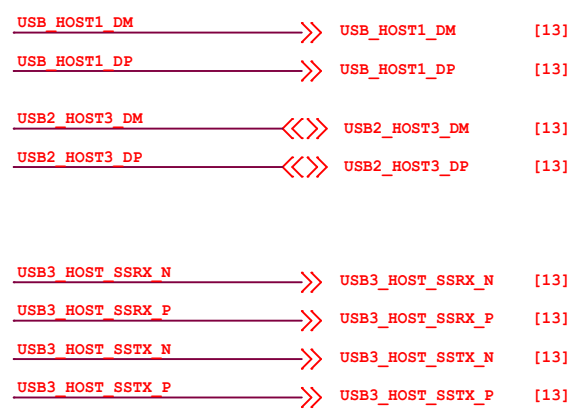
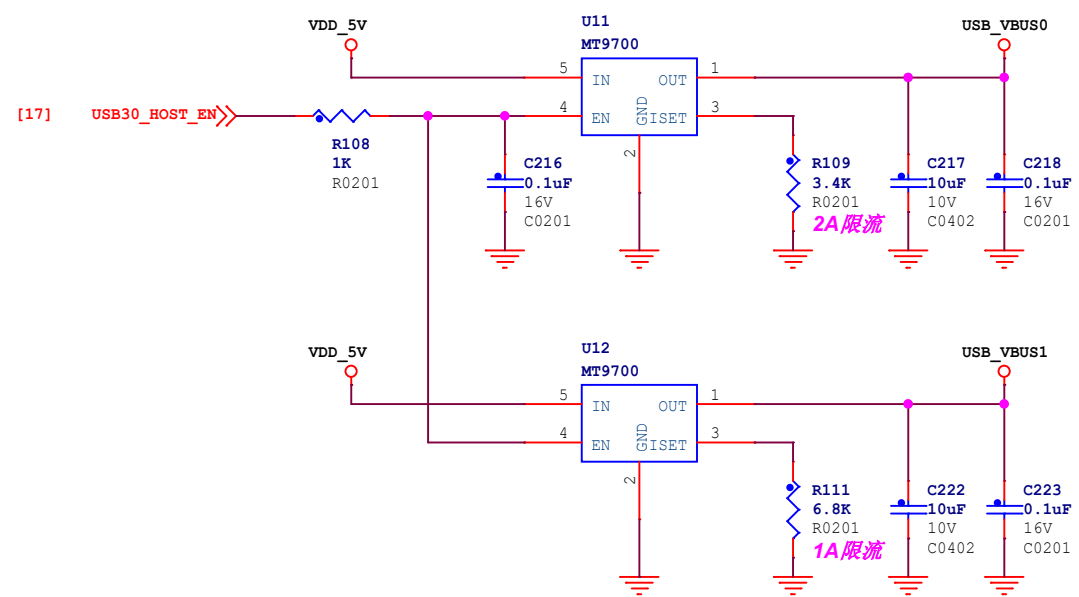
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Title 野火_RK3566_LUBANCAT_1_原理图		
Size A3	Document Number ENMC_FLASH	Rev V2R3
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USB 3.0 HOST x1

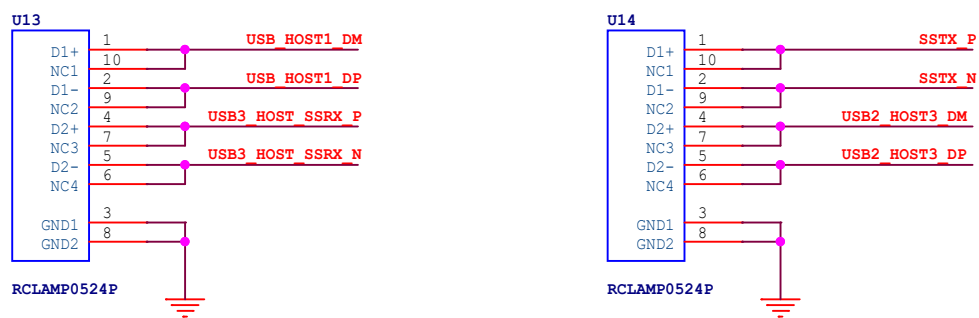
USB 2.0 HOST x1



USB POWER

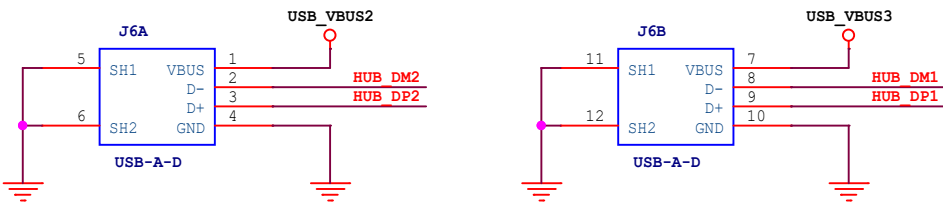


ESD

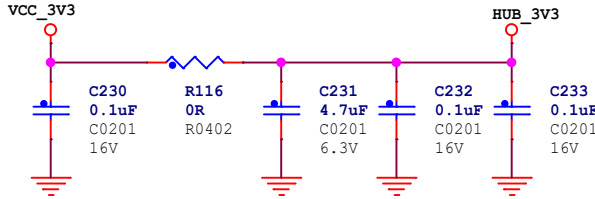


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Title 野火_RK3566 LUBANCAT_1 原理图		
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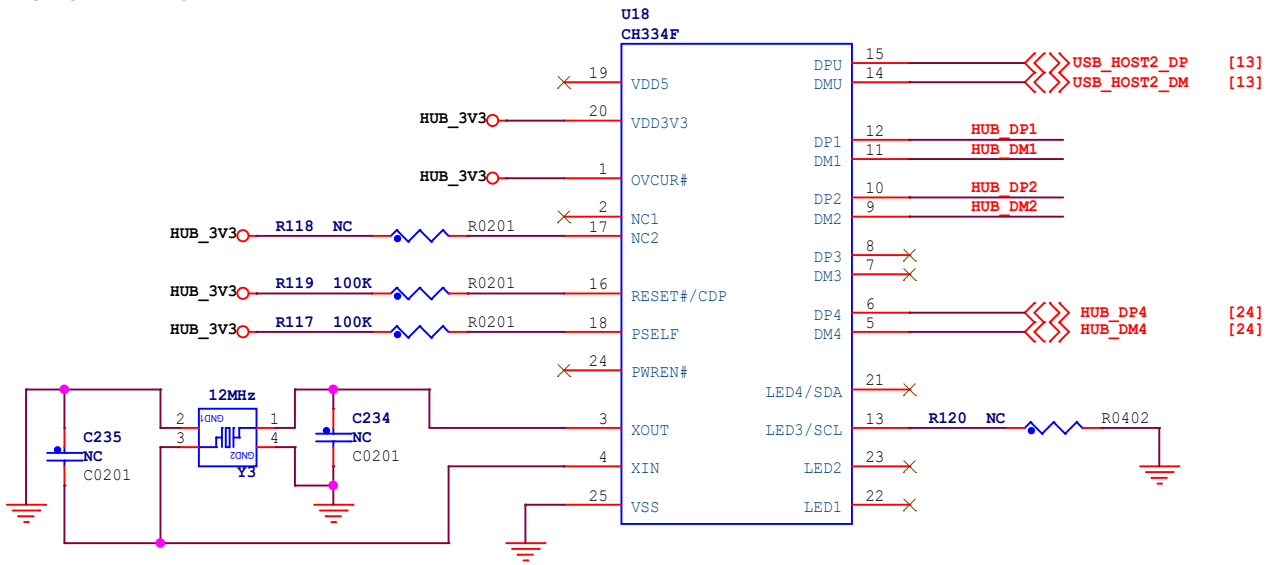
USB 2.0 HOST x2



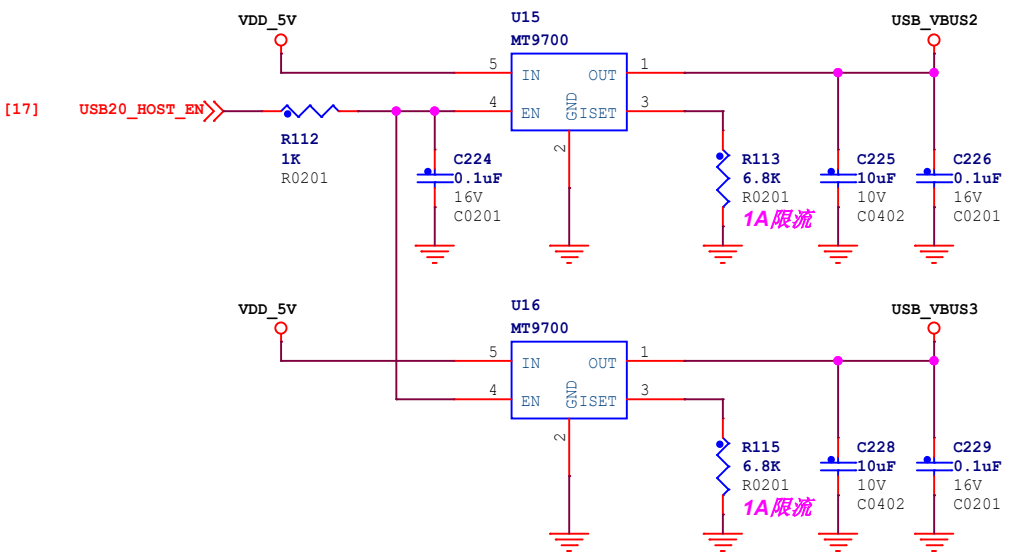
Filter capacitor



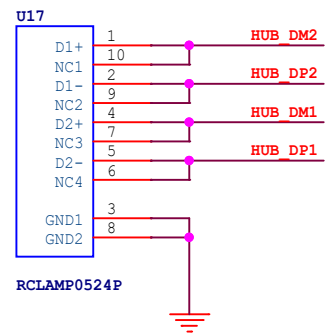
USB 2.0 HUB PHY



USB POWER

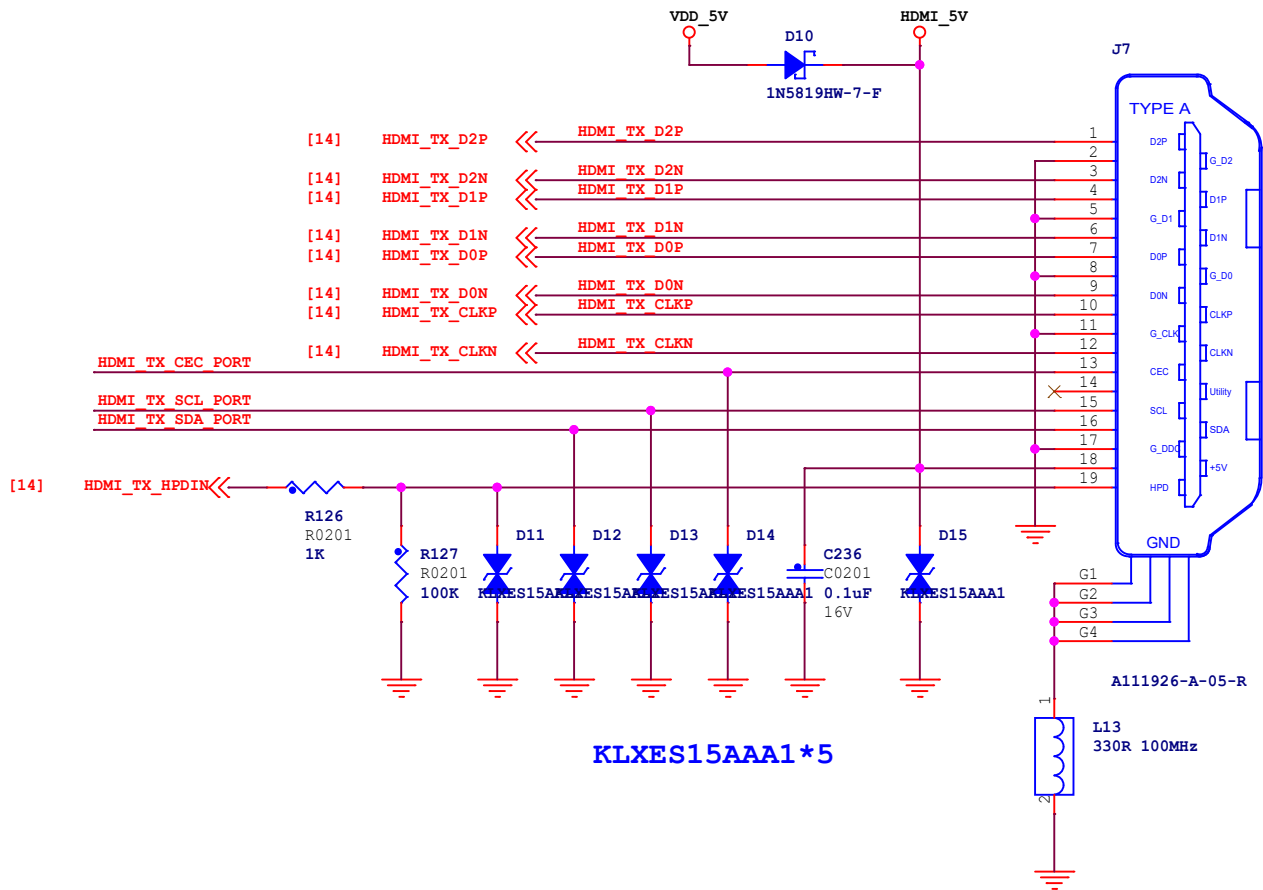
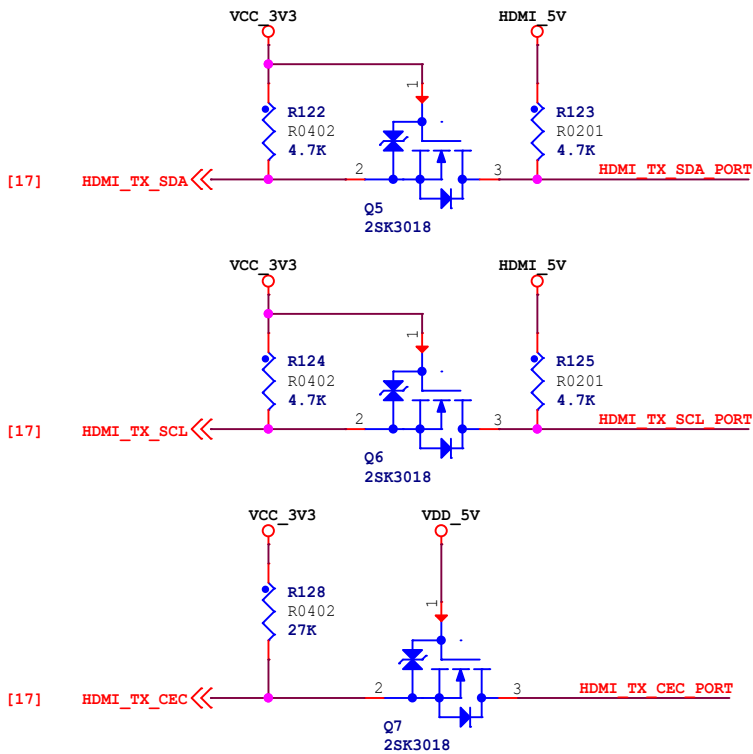


ESD

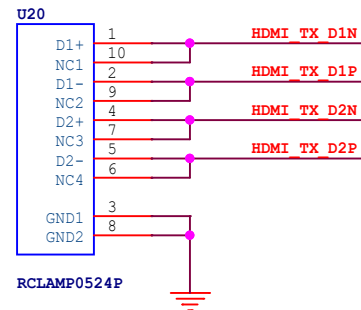
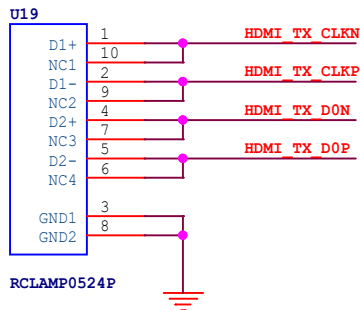


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HDMI_PORT



ESD

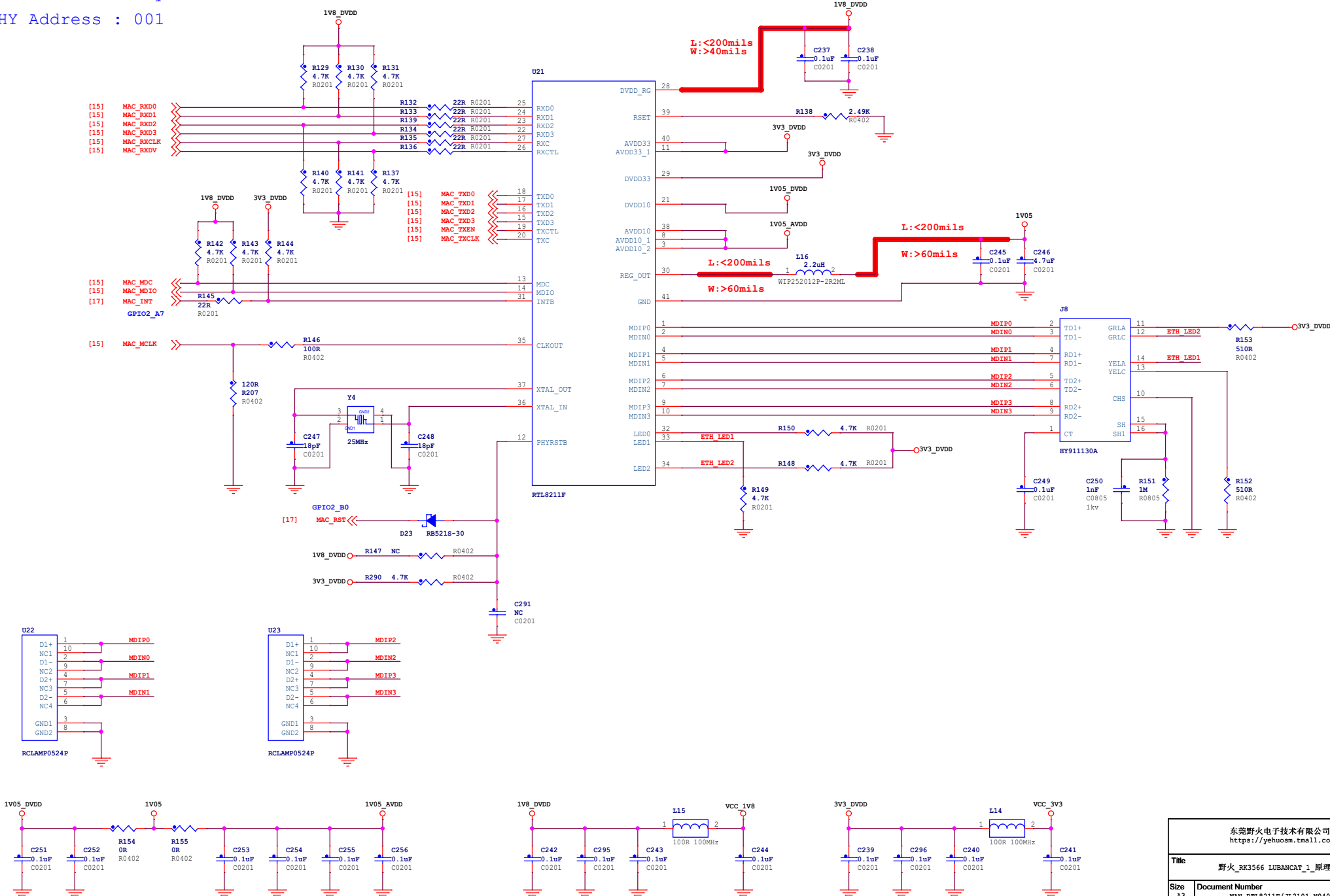


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Title 野火_RK3566 LUBANCAT_1_原理图		
Size A4	Document Number HDMI_PORT	Rev V2R3
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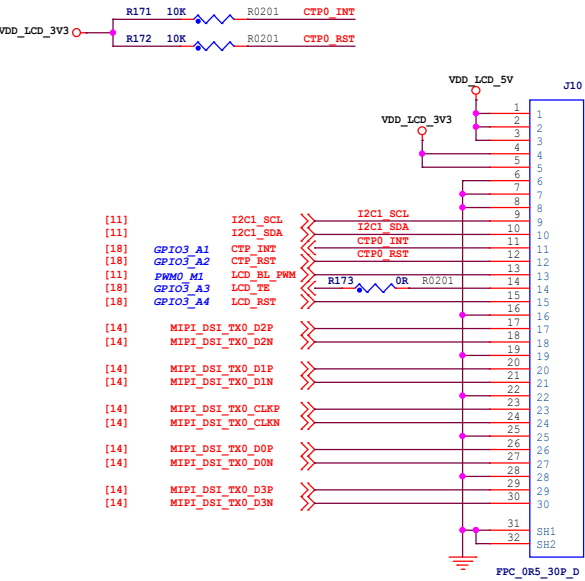
RTL8211F CG

TXC / RXC : delays 2ns

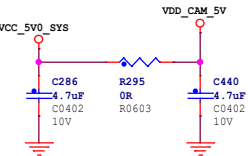
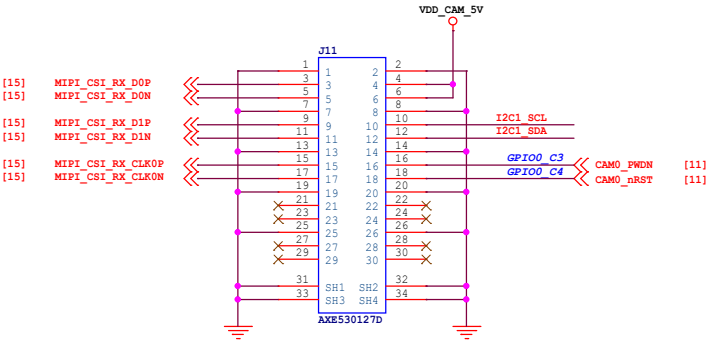
PHY Address : 001



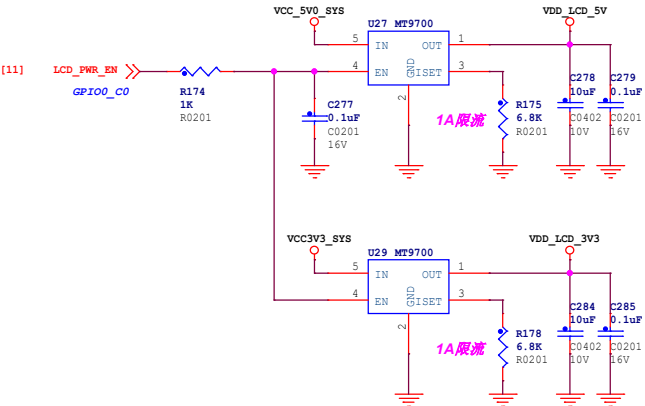
MIPI DSI LCD PORT



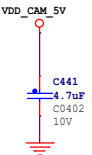
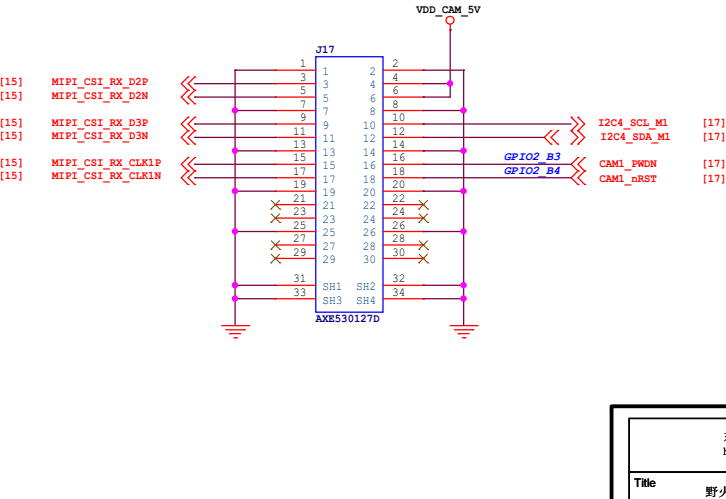
MIPI CSI0 PORT



LCD Power

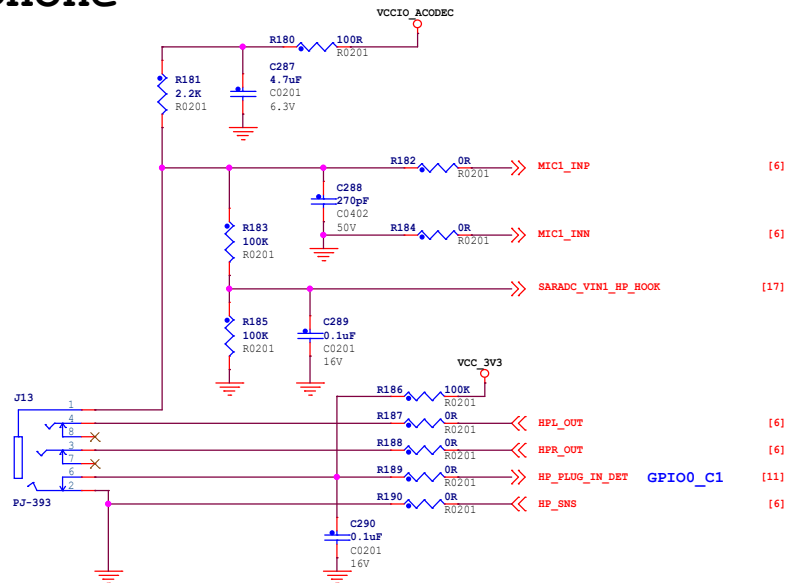


MIPI CSI1 PORT

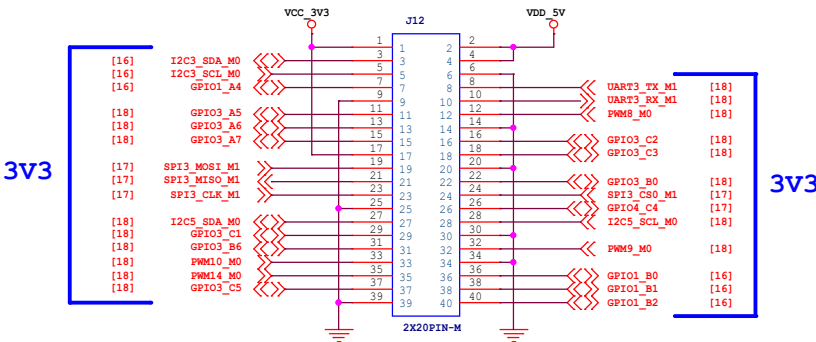


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Title 野火_RK3566_LUBANCAT_1_原理图		
Size A3	Document Number MIPI DSI/MIPI CSI_PORT	Rev V2R3
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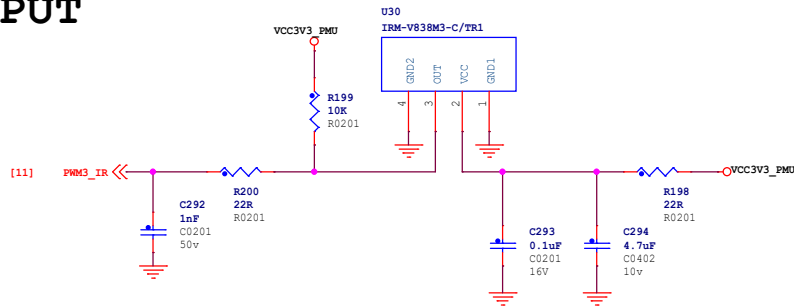
Earphone



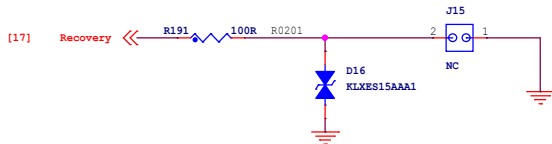
Pin Out



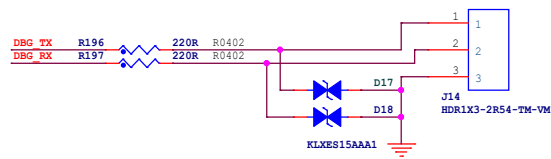
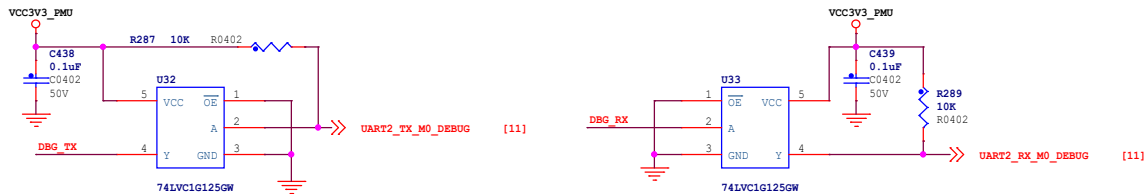
IR_INPUT



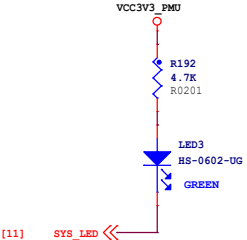
REC KEY



Debug UART2



SYS_LED



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Title 野火_RK3566_LUBANCAT_1_原理图		
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