

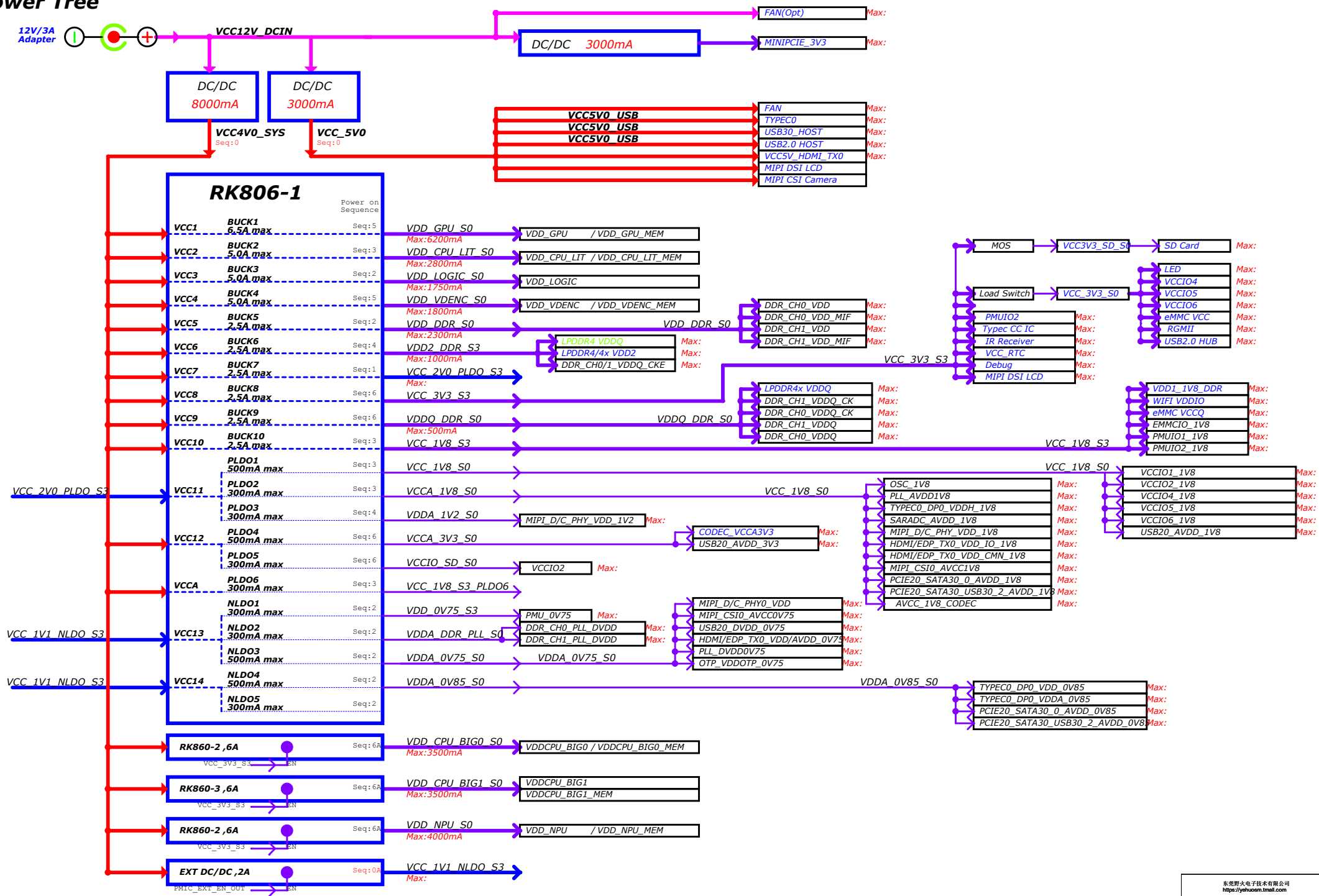
野火鲁班猫5.BTB核心板 (RK3588)

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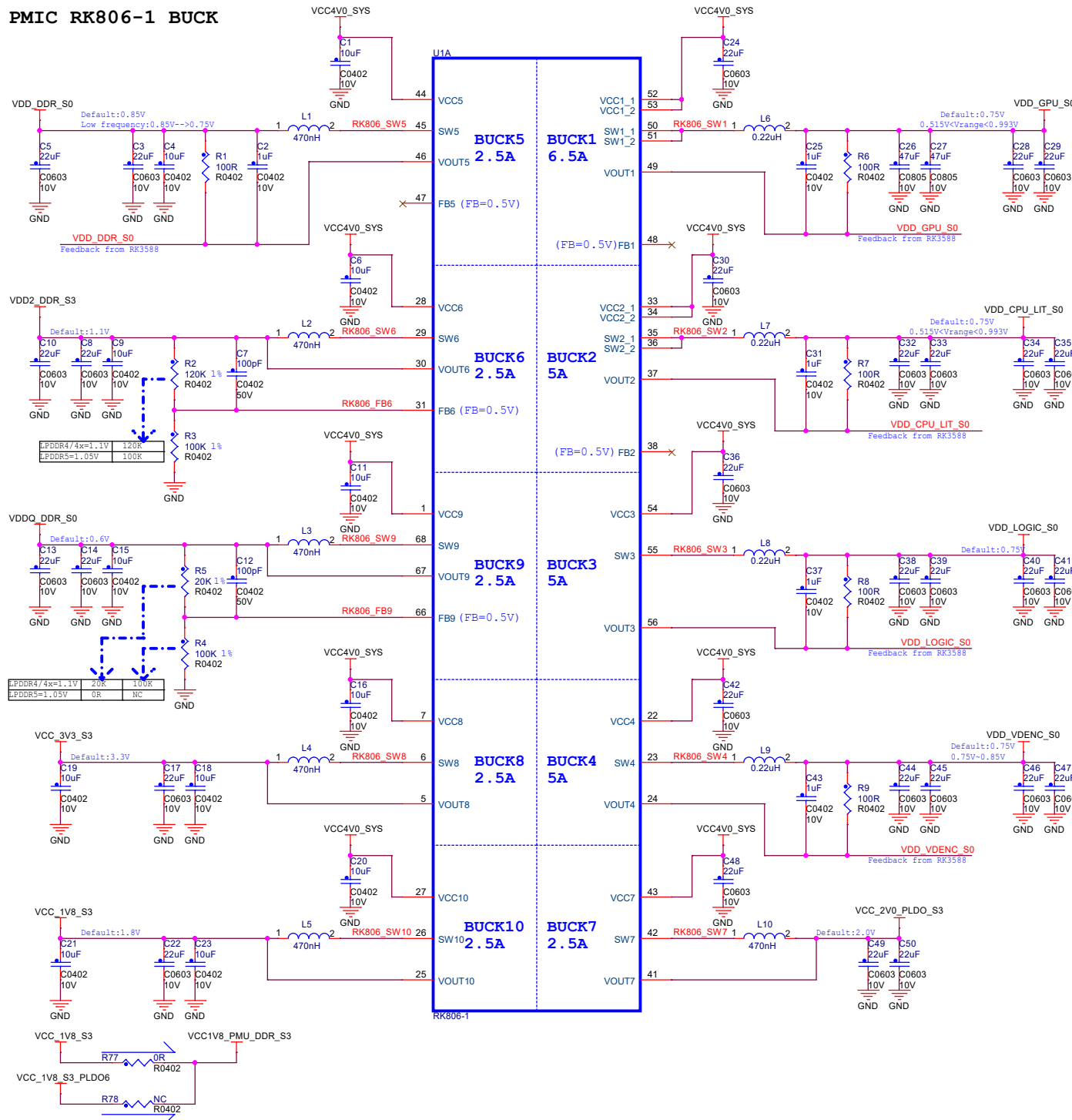
历史版本

版本号	日期	设计	描述
V0.0	2023-07-13	llm	初始版本
V0.1	2024-01-30	llm	1.修正D1二极管正负反了的问题 2.修正SARADC输入滤波电容，修正为1nF
V0.2	2024-05-24	llm	1.BTB座子更换为广濂0.4mm 100PIN的 2.添加SPI Flash 3.根据RK最新参考图，修正部分SOC电源 4.把上电自动开机引脚引出到BTB，供用户自行选择

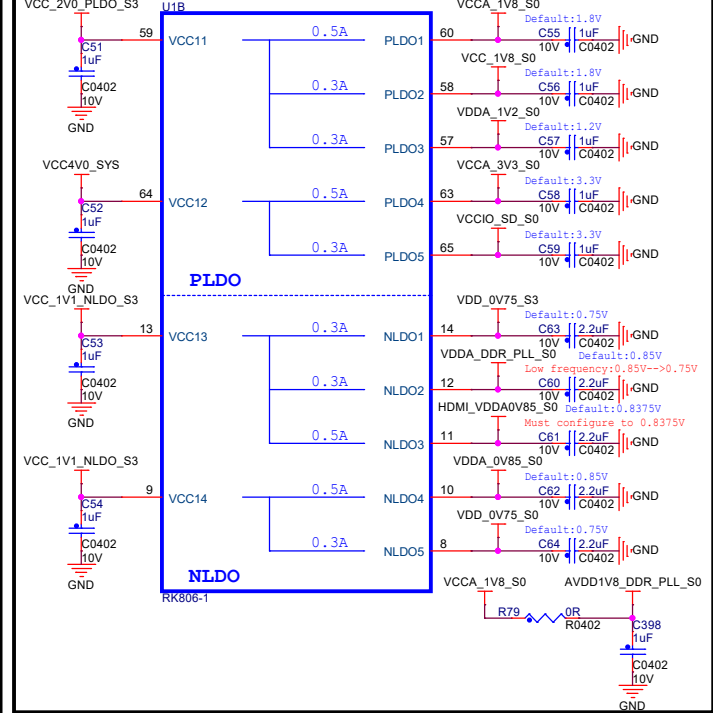
Power Tree



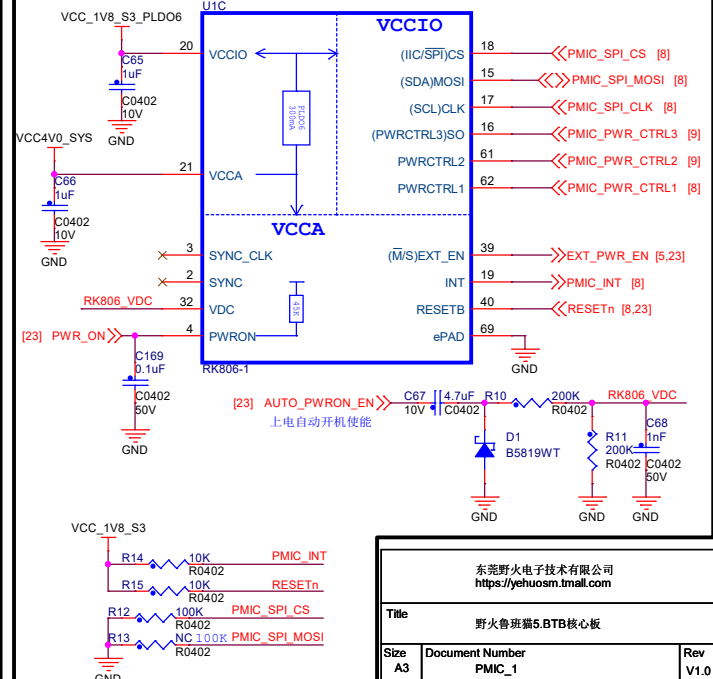
PMIC RK806-1 BUCK



PMIC RK806-1 LDO

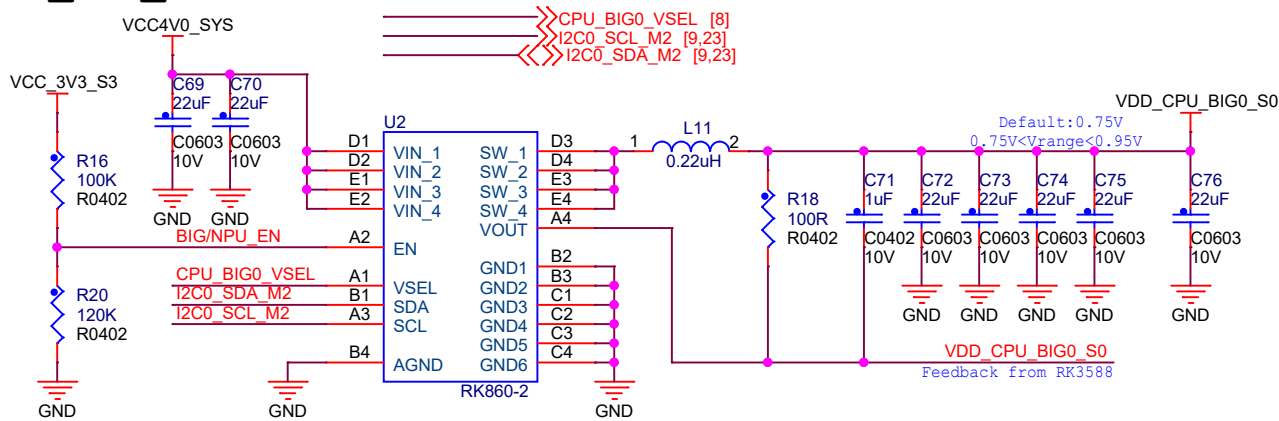


PMIC RK806-1 LDO

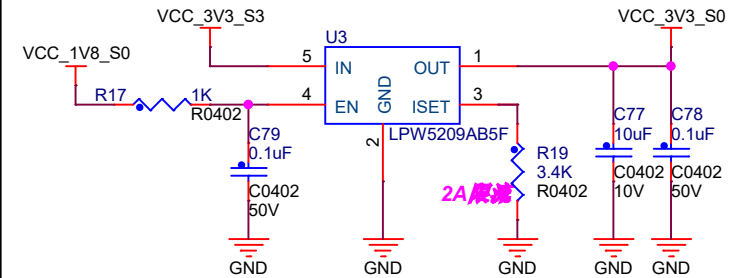


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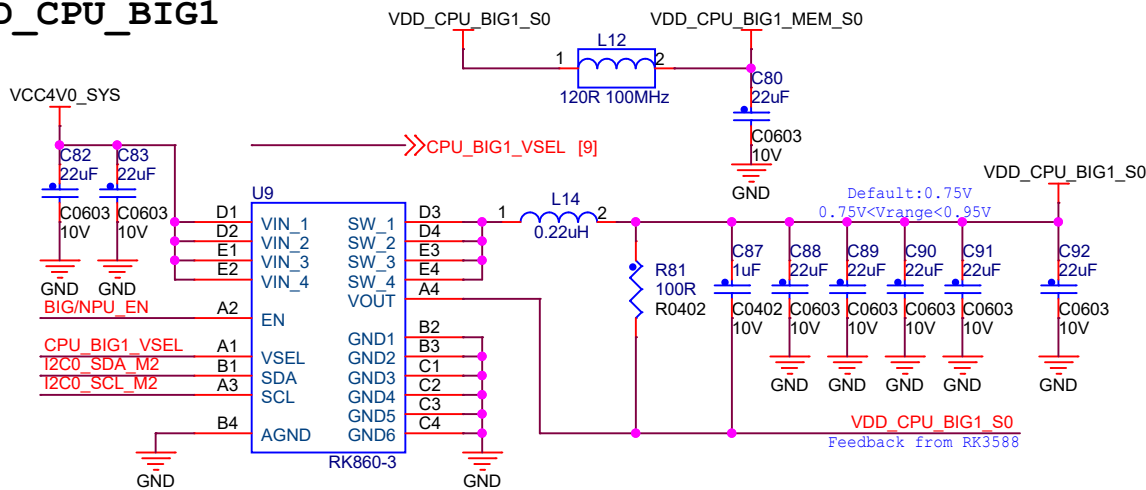
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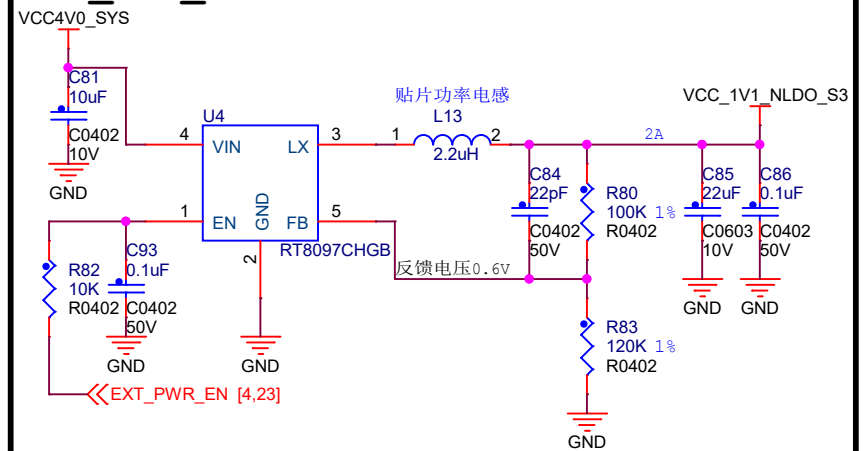
VCC_3V3_S0



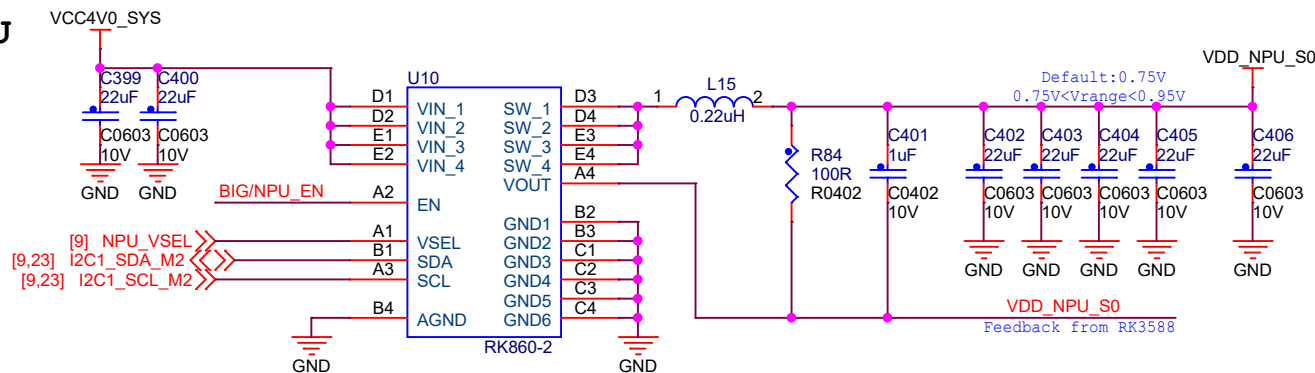
VDD_CPU_BIG1



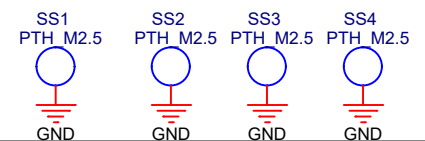
VCC_1V1_NLDO



VDD_NPU



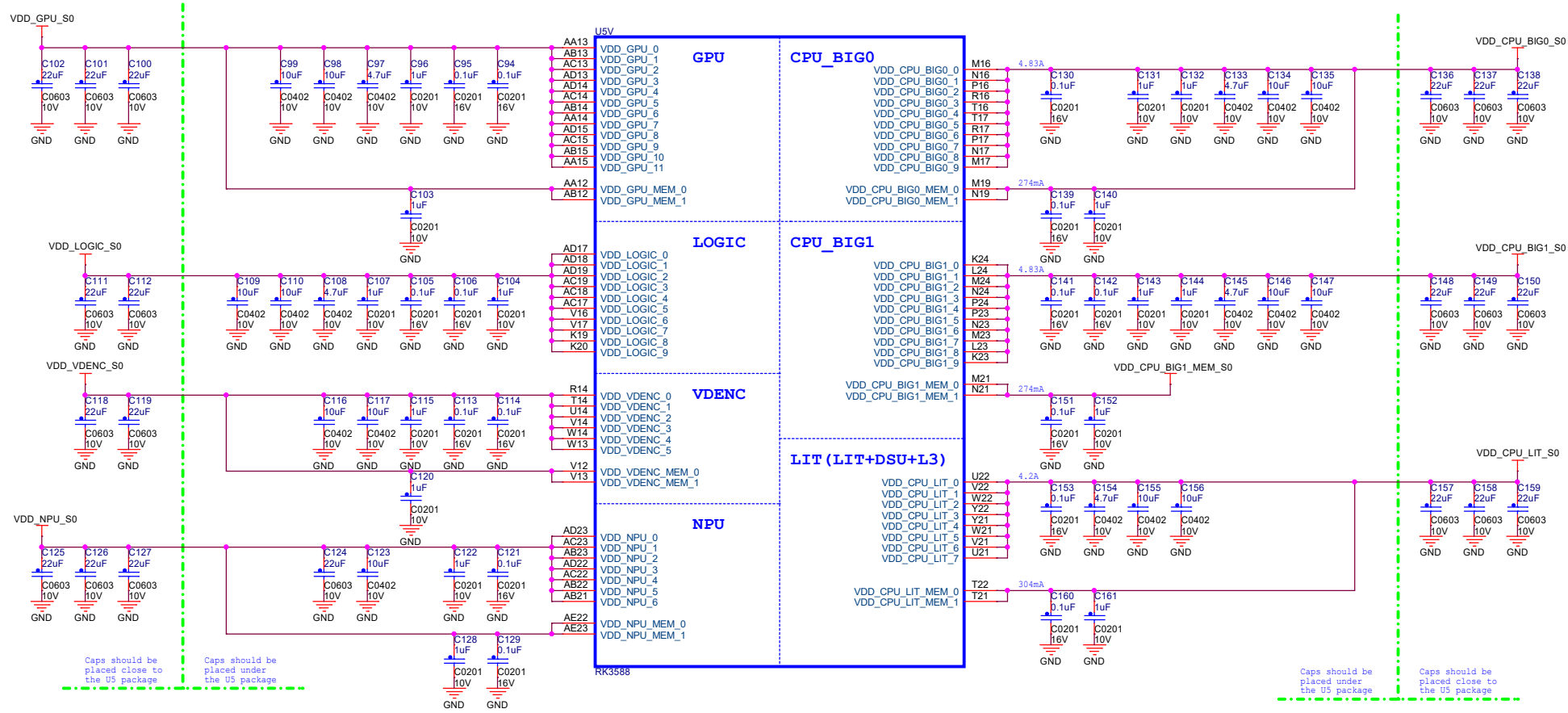
定位孔



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RK3588 POWER



Note:
Caps of between dashed green lines and U5 should be placed close to the U5 package.
Other caps should be placed close to the U5 package

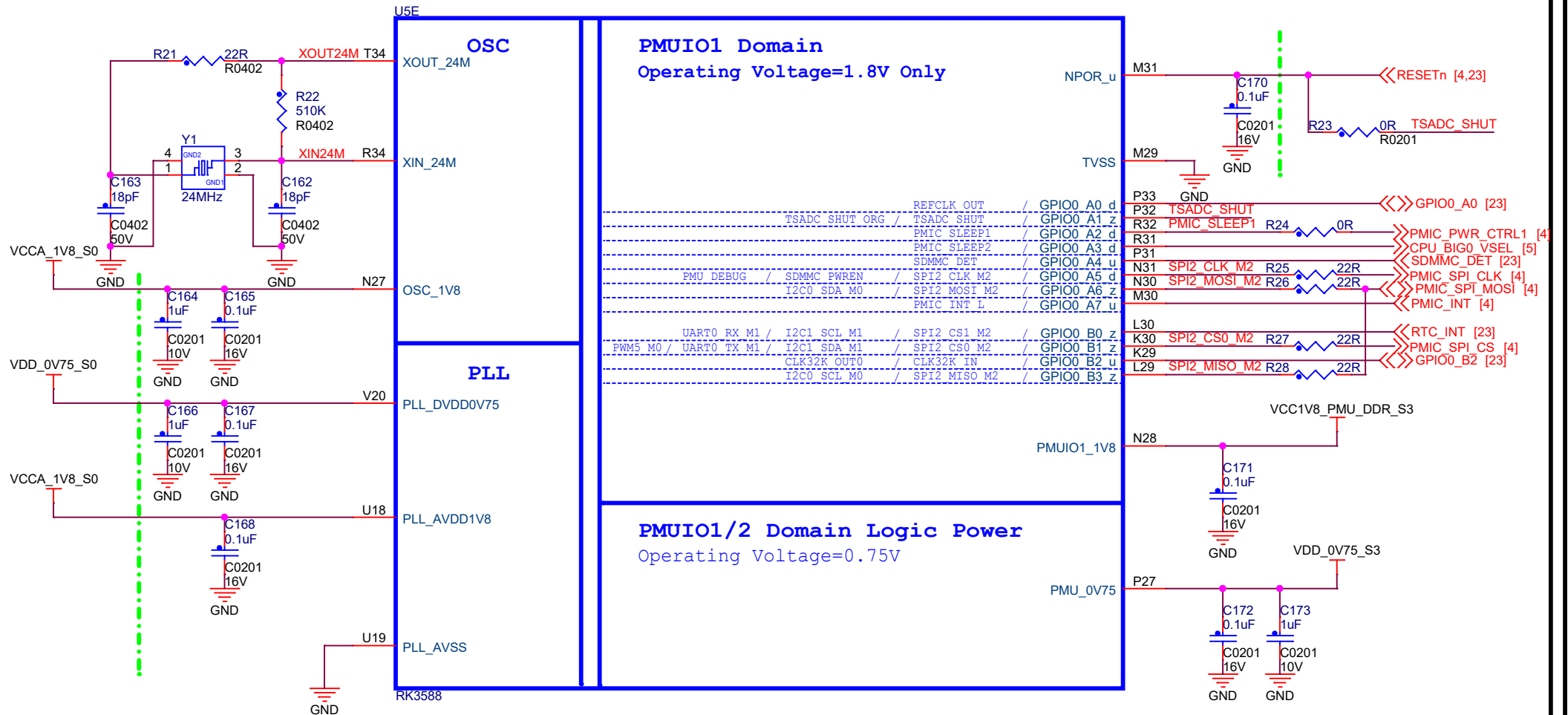
RK3588 GND



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RK3588 OSC/PLL/PMUIO1



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RK3588 PMUIO2

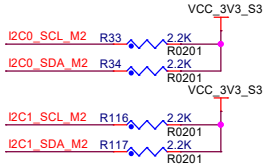
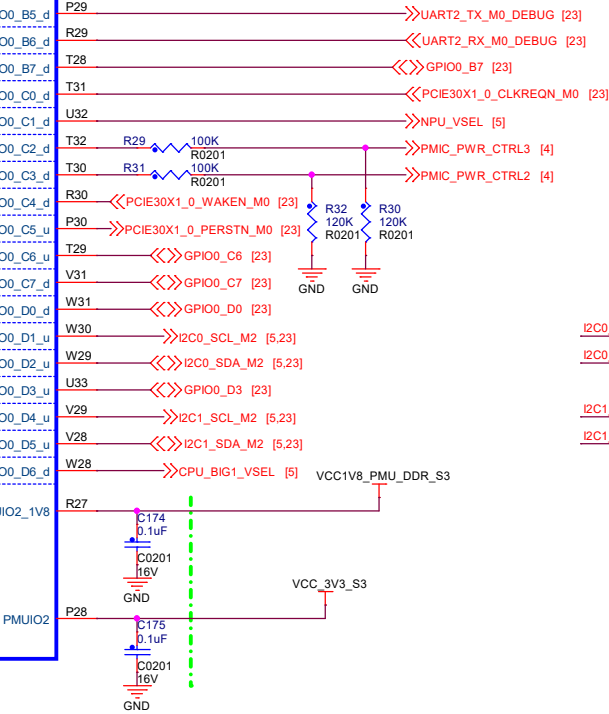
U5F

PMUIO2 Domain

Operating Voltage=1.8V/3.3V

/ UART2_TX_M0	/	/	/ I2S1_MCLK_M1	/ PCIE30X1_1_CLKREQN_M0	/	/ I2C1_SCL_M0	/ JTAG_TCK_M2	/GPIO0_B5_d
/ UART2_RX_M0	/	/	/ I2S1_SCLK_M1	/ PCIE30X1_1_WAKEN_M0	/	/ I2C1_SDA_M0	/ JTAG_TMS_M2	/GPIO0_B6_d
/	/ CAN0_TX_M0	/	/ I2S1_LRCK_M1	/ PCIE30X1_1_PERSTN_M0	/ SPI0_CS1_M0	/ I2C2_SCL_M0	/ PWM0_M0	/GPIO0_B7_d
/	/ CAN0_RX_M0	/ PDM0_CLK0_M1	/	/ PCIE30X1_0_CLKREQN_M0	/ SPI0_MOSI_M0	/ I2C2_SDA_M0	/ PWM1_M0	/GPIO0_C0_d
			/	/	/	/	/ PMIC_SLEEP3	/GPIO0_C1_d
			/	/	/	/	/ PMIC_SLEEP4	/GPIO0_C2_d
			/	/	/	/	/ PMIC_SLEEP5	/GPIO0_C3_d
/ UART0_RX_M0	/ DP0_HPDIN_M1	/ PDM0_CLK1_M1	/	/ PCIE30X1_0_WAKEN_M0	/	/ I2C4_SDA_M2	/ PWM2_M0	/GPIO0_C4_d
PWM4_M0	/ UART0_TX_M0	/ DP1_HPDIN_M1	/	/ I2S1_SDI0_M1	/ PCIE30X1_0_PERSTN_M0	/	/ I2C4_SCL_M2	/ GPU_AVS
PWM5_M1	/ UART0_RTSN	/ SATA_CP_P0D	/	/ I2S1_SDI1_M1	/ PCIE30X4_CLKREQN_M0	/ SPI0_CLK_M0	/	/ NPU_AVS
/	/ UART0_RTSN_M2	/	/ PDM0_SDI0_M1	/ I2S1_SDI2_M1	/ PCIE30X4_WAKEN_M0	/ SPI0_MISO_M0	/ I2C6_SDA_M0	/ PWM6_M0
/	/ UART1_CTSN_M2	/	/ PDM0_SDI1_M1	/ I2S1_SDI3_M1	/ PCIE30X4_PERSTN_M0	/ SPI3_MISO_M2	/ I2C6_SCL_M0	/ PWM7_IR_M0
HDMI_TX0_CEC_M1	/ UART1_TX_M2	/ UART0_CTSN	/ HDMI_RX_SDA_M0	/ I2S1_SDO0_M1	/ PCIE30X2_CLKREQN_M0	/ SPI0_CS0_M0	/ I2C0_SCL_M2	/ CPU_BIG0_AVS
HDMI_TX1_CEC_M1	/ UART1_RX_M2	/	/ HDMI_RX_SCL_M0	/ I2S1_SDO1_M1	/ PCIE30X2_WAKEN_M0	/ SPI3_MOSI_M2	/ I2C0_SDA_M2	/
/	/	/	/	/	/	/ SPI3_CLK_M2	/	/ LITCPU_AVS
HDMI_TX0_SDA_M1	/ SATA_CPDDET	/ CAN2_RX_M1	/ PDM0_SDI2_M1	/ I2S1_SDO2_M1	/ PCIE30X2_PERSTN_M0	/ SPI3_CS0_M2	/ I2C1_SCL_M2	/ PWM3_IR_M0
HDMI_TX0_SCL_M1	/ SATA_MP_SWITCH	/ CAN2_TX_M1	/	/ I2S1_SDO3_M1	/	/ SPI3_CS1_M2	/ I2C1_SDA_M2	/ CPU_BIG1_AVS
			/ PDM0_SDI3_M1	/	/	/	/	/ PMIC_SLEEP6

RK3588



Note:

Caps of between dashed green lines and U5 should be placed under the U5 package.
Other caps should be placed close to the U5 package

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The diagram illustrates the pin connections for the RK3588 SoC, organized into a grid. The left side lists signals and their pin numbers, while the right side lists signals and their pin numbers. The center shows the SoC pins and their connections to the external signals.

DDR Connections:

- DDR_CH0_DQ0_A, DDR_CH0_DQ1_A, DDR_CH0_DQ2_A, DDR_CH0_DQ3_A, DDR_CH0_DQ4_A, DDR_CH0_DQ5_A, DDR_CH0_DQ6_A, DDR_CH0_DQ7_A, DDR_CH0_DQ8_A, DDR_CH0_DQ9_A, DDR_CH0_DQ10_A, DDR_CH0_DQ11_A, DDR_CH0_DQ12_A, DDR_CH0_DQ13_A, DDR_CH0_DQ14_A, DDR_CH0_DQ15_A
- DDR_CH0_DQ0_B, DDR_CH0_DQ1_B, DDR_CH0_DQ2_B, DDR_CH0_DQ3_B, DDR_CH0_DQ4_B, DDR_CH0_DQ5_B, DDR_CH0_DQ6_B, DDR_CH0_DQ7_B, DDR_CH0_DQ8_B, DDR_CH0_DQ9_B, DDR_CH0_DQ10_B, DDR_CH0_DQ11_B, DDR_CH0_DQ12_B, DDR_CH0_DQ13_B, DDR_CH0_DQ14_B, DDR_CH0_DQ15_B

DM0 Connections:

- DDR_CH0_DM0_A, DDR_CH0_DM1_A
- DDR_CH0_DM0_B, DDR_CH0_DM1_B

DQSOP Connections:

- DDR_CH0_DQSOP_A, DDR_CH0_DQSOP_B

WCKOP Connections:

- DDR_CH0_WCKOP_A, DDR_CH0_WCKOP_B

A0-A6 Connections:

- DDR_CH0_A0_A, DDR_CH0_A0_B, DDR_CH0_A1_A, DDR_CH0_A1_B, DDR_CH0_A2_A, DDR_CH0_A2_B, DDR_CH0_A3_A, DDR_CH0_A3_B, DDR_CH0_A4_A, DDR_CH0_A4_B, DDR_CH0_A5_A, DDR_CH0_A5_B, DDR_CH0_A6_A

CLKP and CLKN Connections:

- DDR_CH0_CLKP_A, DDR_CH0_CLKP_B
- DDR_CH0_CLKN_A, DDR_CH0_CLKN_B

LP4/4X Connections:

- DDR_CH0_LP4/4X_CKE0_A, DDR_CH0_LP4/4X_CKE1_A, DDR_CH0_LP4/4X_CKE0_B, DDR_CH0_LP4/4X_CKE1_B

VDDQ Connections:

- VDDQ_DDR_S0, VDDQ_DDR_S1

Power and Ground Connections:

- AVDD1V8, VDD_PLL_S0, VDDA_DDR_PLL_S0, VDDA_DDR_PLL_S1, VDDA_DDR_PLL_S2, VDDA_DDR_PLL_S3, VDDA_DDR_PLL_S4, VDDA_DDR_PLL_S5, VDDA_DDR_PLL_S6, VDDA_DDR_PLL_S7, VDDA_DDR_PLL_S8, VDDA_DDR_PLL_S9, VDDA_DDR_PLL_S10, VDDA_DDR_PLL_S11, VDDA_DDR_PLL_S12, VDDA_DDR_PLL_S13, VDDA_DDR_PLL_S14, VDDA_DDR_PLL_S15, VDDA_DDR_PLL_S16, VDDA_DDR_PLL_S17, VDDA_DDR_PLL_S18, VDDA_DDR_PLL_S19, VDDA_DDR_PLL_S20, VDDA_DDR_PLL_S21, VDDA_DDR_PLL_S22, VDDA_DDR_PLL_S23, VDDA_DDR_PLL_S24, VDDA_DDR_PLL_S25, VDDA_DDR_PLL_S26, VDDA_DDR_PLL_S27, VDDA_DDR_PLL_S28, VDDA_DDR_PLL_S29, VDDA_DDR_PLL_S30, VDDA_DDR_PLL_S31, VDDA_DDR_PLL_S32, VDDA_DDR_PLL_S33, VDDA_DDR_PLL_S34, VDDA_DDR_PLL_S35, VDDA_DDR_PLL_S36, VDDA_DDR_PLL_S37, VDDA_DDR_PLL_S38, VDDA_DDR_PLL_S39, VDDA_DDR_PLL_S40, VDDA_DDR_PLL_S41, VDDA_DDR_PLL_S42, VDDA_DDR_PLL_S43, VDDA_DDR_PLL_S44, VDDA_DDR_PLL_S45, VDDA_DDR_PLL_S46, VDDA_DDR_PLL_S47, VDDA_DDR_PLL_S48, VDDA_DDR_PLL_S49, VDDA_DDR_PLL_S50, VDDA_DDR_PLL_S51, VDDA_DDR_PLL_S52, VDDA_DDR_PLL_S53, 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Pin-to-pin mapping diagram for RK3588 showing connections between the processor pins and the DDR4 memory module pins. The diagram is divided into several sections: DDR CH1 signals (Data, Command, Address, Strobe, Sense Amplifier, and Clock), VDDQ and VDD signals, and power planes (PLL, Memory Interface, Digital Core, and I/O).

DDR CH1 Signals:

- DDR_CH1_DQ0_C:** A8, B9, A9, B10, A6, B7, A7, B8, A3, B3, A2, B2, A5, B5, A4, B4, A6, B6, A7, B7, A8, B8, A9, B9, A10, B10, A11, B11, A12, B12, A13, B13, A14, B14, A15, B15, A16, B16, A17, B17, A18, B18, A19, B19, A20, B20, A21, B21, A22, B22, A23, B23, A24, B24, A25, B25, A26, B26, A27, B27, A28, B28, A29, B29, A30, B30, A31, B31, A32, B32, A33, B33, A34, B34, A35, B35, A36, B36, A37, B37, A38, B38, A39, B39, A40, B40, A41, B41, A42, B42, A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50, A51, B51, A52, B52, A53, B53, A54, B54, A55, B55, A56, B56, A57, B57, A58, B58, A59, B59, A60, B60, A61, B61, A62, B62, A63, B63, A64, B64, A65, B65, A66, B66, A67, B67, A68, B68, A69, B69, A70, B70, A71, B71, A72, B72, A73, B73, A74, B74, A75, B75, A76, B76, A77, B77, A78, B78, A79, B79, A80, B80, A81, B81, A82, B82, A83, B83, A84, B84, A85, B85, A86, B86, A87, B87, A88, B88, A89, B89, A90, B90, A91, B91, A92, B92, A93, B93, A94, B94, A95, B95, A96, B96, A97, B97, A98, B98, A99, B99, A100, B100, A101, B101, A102, B102, A103, B103, A104, B104, A105, B105, A106, B106, A107, B107, A108, B108, A109, B109, A110, B110, A111, B111, A112, B112, A113, B113, A114, B114, A115, B115, A116, B116, A117, B117, A118, B118, A119, B119, A120, B120, A121, B121, A122, B122, A123, B123, A124, B124, A125, B125, A126, B126, A127, B127, A128, B128, A129, B129, A130, B130, A131, B131, A132, B132, A133, B133, A134, B134, A135, B135, A136, B136, A137, B137, A138, B138, A139, B139, A140, B140, A141, B141, A142, B142, A143, B143, A144, B144, A145, B145, A146, B146, A147, B147, A148, B148, A149, B149, A150, B150, A151, B151, A152, B152, A153, B153, A154, B154, A155, B155, A156, B156, A157, B157, A158, B158, A159, B159, A160, B160, A161, B161, A162, B162, A163, B163, A164, B164, A165, B165, A166, B166, A167, B167, A168, B168, A169, B169, A170, B170, A171, B171, A172, B172, A173, B173, A174, B174, A175, B175, A176, B176, A177, B177, A178, B178, A179, B179, A180, B180, A181, B181, A182, B182, A183, B183, A184, B184, A185, B185, A186, B186, A187, B187, A188, B188, A189, B189, A190, B190, A191, B191, A192, B192, A193, B193, A194, B194, A195, B195, A196, B196, A197, B197, A198, B198, A199, B199, A200, B200, A201, B201, A202, B202, A203, B203, A204, B204, A205, B205, A206, B206, A207, B207, A208, B208, A209, B209, A210, B210, A211, B211, A212, B212, A213, B213, A214, B214, A215, B215, A216, B216, A217, B217, A218, B218, A219, B219, A220, B220, A221, B221, A222, B222, A223, B223, A224, B224, A225, B225, A226, B226, A227, B227, A228, B228, A229, B229, A230, B230, A231, B231, A232, B232, A233, B233, A234, B234, A235, B235, A236, B236, A237, B237, A238, B238, A239, B239, A240, B240, A241, B241, A242, B242, A243, B243, A244, B244, A245, B245, A246, B246, A247, B247, A248, B248, A249, B249, A250, B250, A251, B251, A252, B252, A253, B253, A254, B254, A255, B255, A256, B256, A257, B257, A258, B258, A259, B259, A260, B260, A261, B261, A262, B262, A263, B263, A264, B264, A265, B265, A266, B266, A267, B267, A268, B268, A269, B269, A270, B270, A271, B271, A272, B272, A273, B273, A274, B274, A275, B275, A276, B276, A277, B277, A278, B278, A279, B279, A280, B280, A281, B281, A282, B282, A283, B283, A284, B284, A285, B285, A286, B286, A287, B287, A288, B288, A289, B289, A290, B290, A291, B291, A292, B292, A293, B293, A294, B294, A295, B295, A296, B296, A297, B297, A298, B298, A299, B299, A300, B300, A301, B301, A302, B302, A303, B303, A304, B304, A305, B305, A306, B306, A307, B307, A308, B308, A309, B309, A310, B310, A311, B311, A312, B312, A313, B313, A314, B314, A315, B315, A316, B316, A317, B317, A318, B318, A319, B319, A320, B320, A321, B321, A322, B322, A323, B323, A324, B324, A325, B325, A326, B326, A327, B327, A328, B328, A329, B329, A330, B330, A331, B331, A332, B332, A333, B333, A334, B334, A335, B335, A336, B336, A337, B337, A338, B338, A339, B339, A340, B340, A341, B341, A342, B342, A343, B343, A344, B344, A345, B345, A346, B346, A347, B347, A348, B348, A349, B349, A350, B350, A351, B351, A352, B352, A353, B353, A354, B354, A355, B355, A356, B356, A357, B357, A358, B358, A359, B359, A360, B360, A361, B361, A362, B362, A363, B363, A364, B364, A365, B365, A366, B366, A367, B367, A368, B368, A369, B369, A370, B370, A371, B371, A372, B372, A373, B373, A374, B374, A375, B375, A376, B376, A377, B377, A378, B378, A379, B379, A380, B380, A381, B381, A382, B382, A383, B383, A384, B384, A385, B385, A386, B386, A387, B387, A388, B388, A389, B389, A390, B390, A391, B391, A392, B392, A393, B393, A394, B394, A395, B395, A396, B396, A397, B397, A398, B398, A399, B399, A400, B400, A401, B401, A402, B402, A403, B403, A404, B404, A405, B405, A406, B406, A407, B407, A

VDDQ_DDR_S0

VDDQ_DDR_CK_S0 VDDQ_DDR_CKE_S3

Hold power of CLK during retention times.

Sequence:
VDD-VDDQ_CKE-VDDQ

VDDQ_LP4/4X_CKE/LP5 CS:
power for LP4_CKE/LP5 CS and RESET,
lpddr4x=1.1V/lpddr5=1.05V

VDDQ_CK:power for CK,
LPDDR4/4X=0.6V/LPDDR5=0.5V

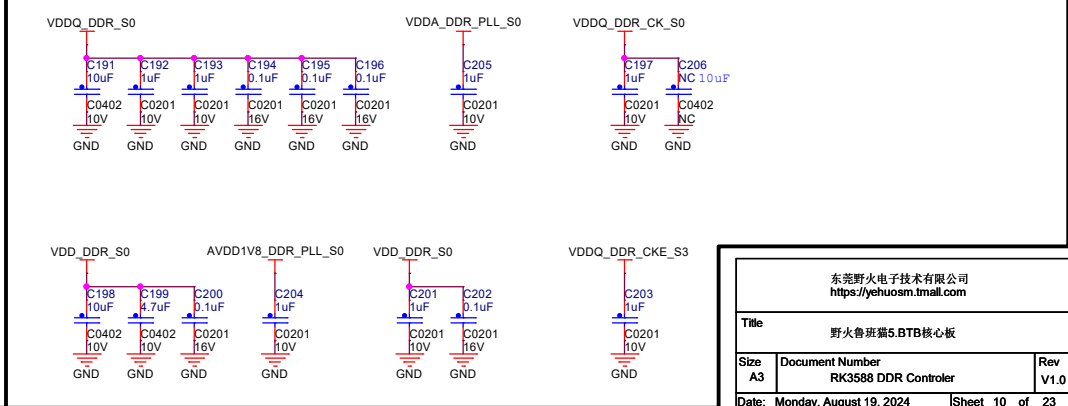
VDDQ:Power for DDR IO(except for ck,
cke and reset);
LPDDR4/4X=0.6V/LPDDR5=0.5V

VDD_DDR_S0

AVDDI1V8_DDR_PLL_S0

VDDA_DDR_PLL_S0

VDDQ_DDR_S0



RK3588 EMMCIO Domain

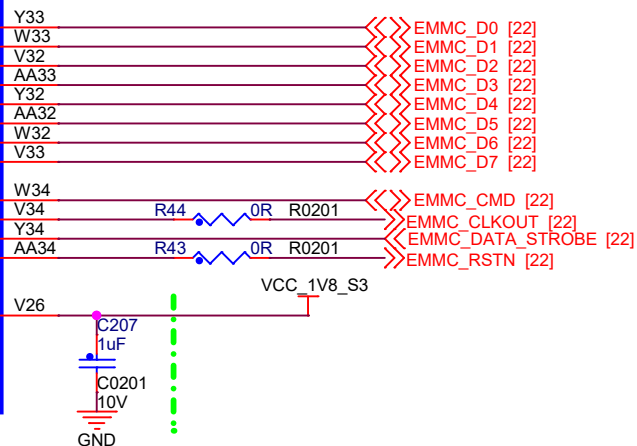
U5C

EMMCIO Domain

Operating Voltage=1.8V

FSPI D0 M0	/ EMMC D0	/ GPIO2 D0 u
FSPI D1 M0	/ EMMC D1	/ GPIO2 D1 u
FSPI D2 M0	/ EMMC D2	/ GPIO2 D2 u
FSPI D3 M0	/ EMMC D3	/ GPIO2 D3 u
UART5 RX M2	/ I2C1 SCL M3	/ EMMC D4
UART5 TX M2	/ I2C1 SDA M3	/ EMMC D5
FSPI CS0N M0	/ EMMC D6	/ GPIO2 D6 u
FSPI CS1N M0	/ EMMC D7	/ GPIO2 D7 u
FSPI CLK M0	/ EMMC CMD	/ GPIO2 A0 u
	/ EMMC CLKOUT	/ GPIO2 A1 d
UART5 CTSN M1	/ I2C2 SDA M2	/ EMMC DATA STROBE
UART5 RTSN M1	/ I2C2 SCL M2	/ EMMC RSTN

EMMCIO_1V8



RK3588 VCCIO2 Domain

U5D

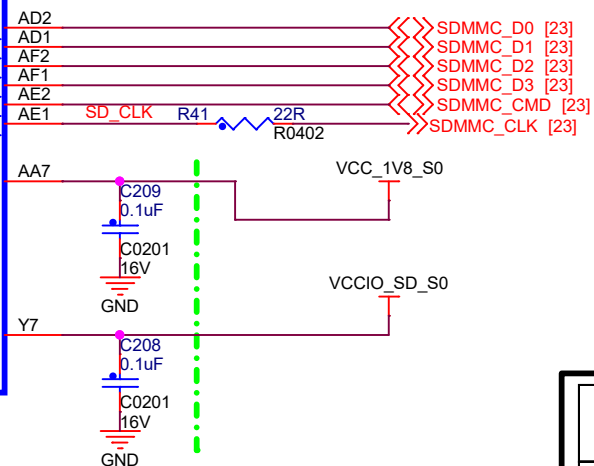
VCCIO2 Domain

Operating Voltage=1.8V/3.3V

PWM8 M1	/ I2C3 SCL M4	/ PDM1 SDI3 M0	/ JTAG TCK M1	/ UART2 TX M1	/ SDMMC D0	/ GPIO4 D0 u
PWM9 M1	/ I2C3 SDA M4	/ PDM1 SDI2 M0	/ JTAG TMS M1	/ UART2 RX M1	/ SDMMC D1	/ GPIO4 D1 u
	/ I2C8 SCL M0	/ PDM1 SDI1 M0	/ JTAG TCK M0	/ UART5 CTSN M0	/ SDMMC D2	/ GPIO4 D2 u
PWM10 M1	/ I2C8 SDA M0	/ PDM1 SDI0 M0	/ JTAG TMS M0	/ UART5 RTSN M0	/ SDMMC D3	/ GPIO4 D3 u
PWM7 IR M1	/ CAN0 TX M1	/ PDM1 CLK1 M0	/ MCU JTAG TCK M0	/ UART5 RX M0	/ SDMMC CMD	/ GPIO4 D4 u
TEST CLKOUT M0	/ CAN0 RX M1	/ PDM1 CLK0 M0	/ MCU JTAG TMS M0	/ UART5 TX M0	/ SDMMC CLK	/ GPIO4 D5 d

VCCIO2_1V8

VCCIO2



Note:

Caps of between dashed green lines and U5 should be placed under the U5 package.
Other caps should be placed close to the U5 package

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Title

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Size
A4

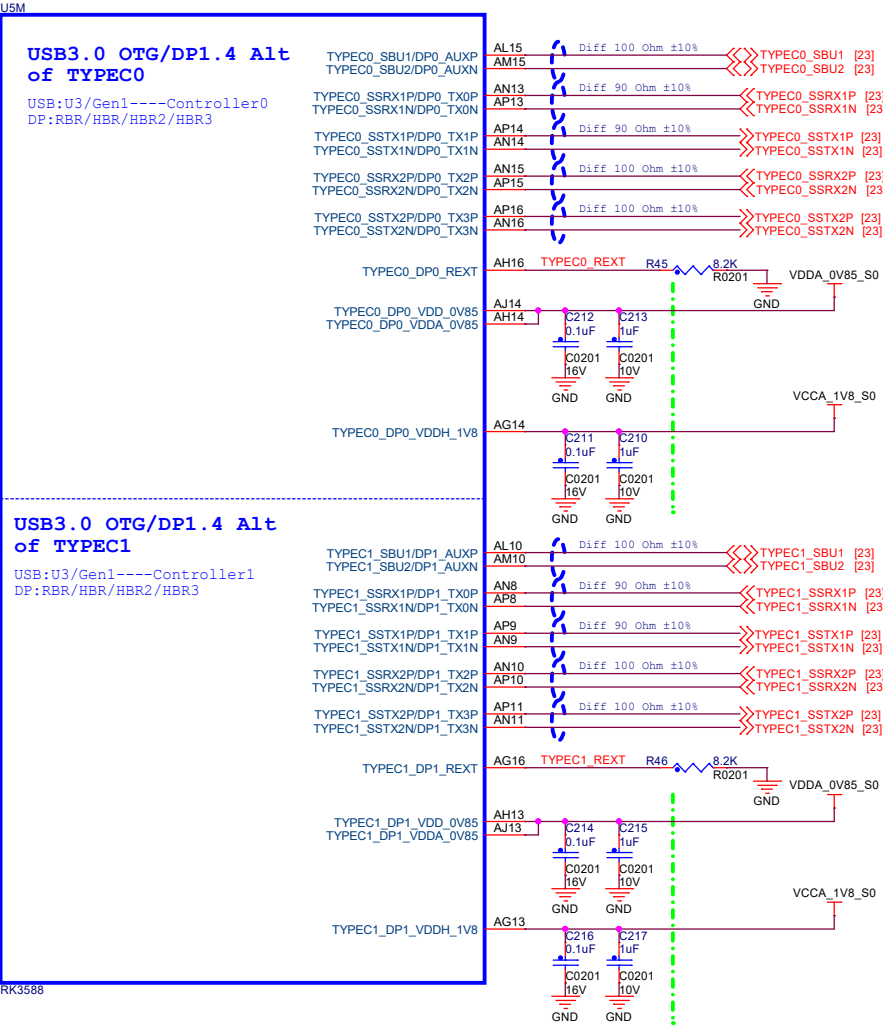
Document Number
RK3588 EMMCIO/VCCIO2

Rev
V1.0

Date: Monday, August 19, 2024

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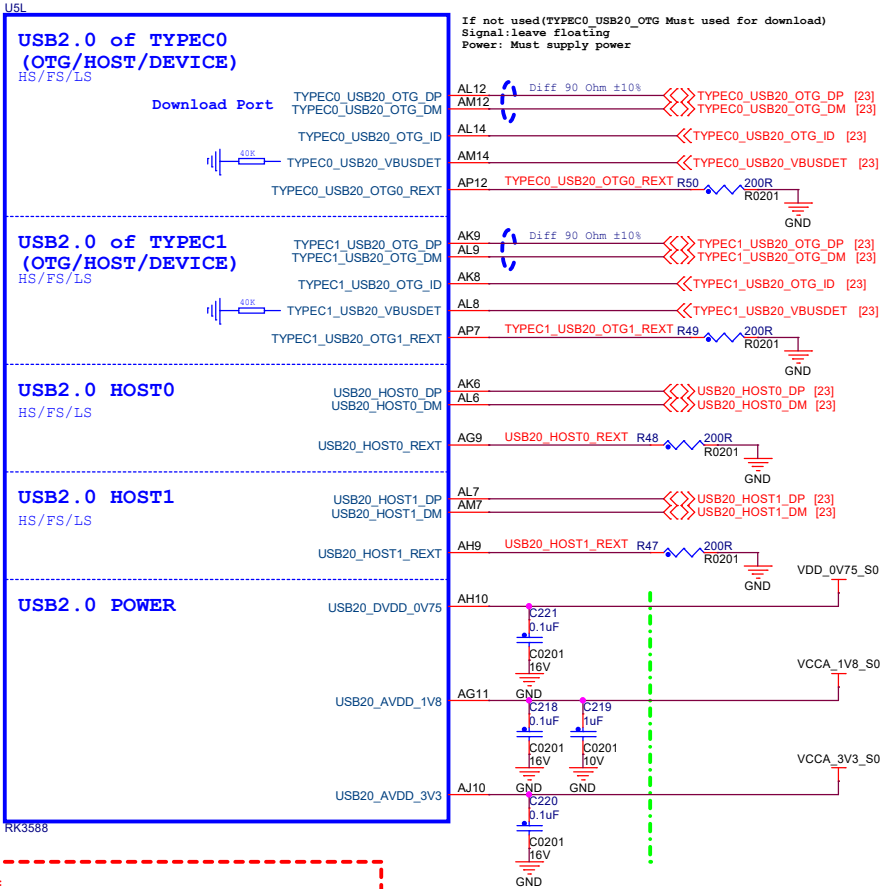
RK3588 TYPEC/DP



USB30/DP1.4 Alt Mode Configuration

Option1	DP x4Lane	DP_TX_Lane0-3
Option2	USB30 x4Lane	DP_TX_Lane0-3
Option3	USB30X2Lane+DPX2Lane	USB30: Lane0 Lane1 DP: Lane2 Lane3
Option4	USB30X2Lane+DPX2Lane	USB30: Lane2 Lane3 DP: Lane0 Lane1

RK3588 USB2.0 HOST/OTG



Note:

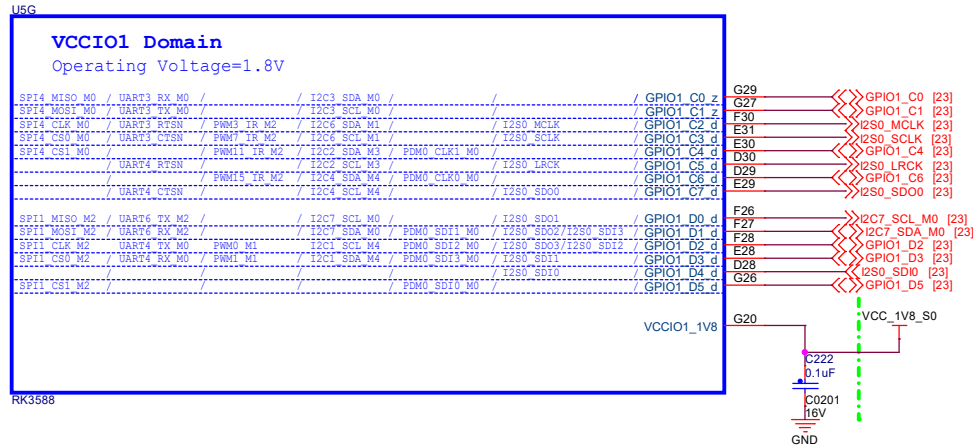
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground.The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:

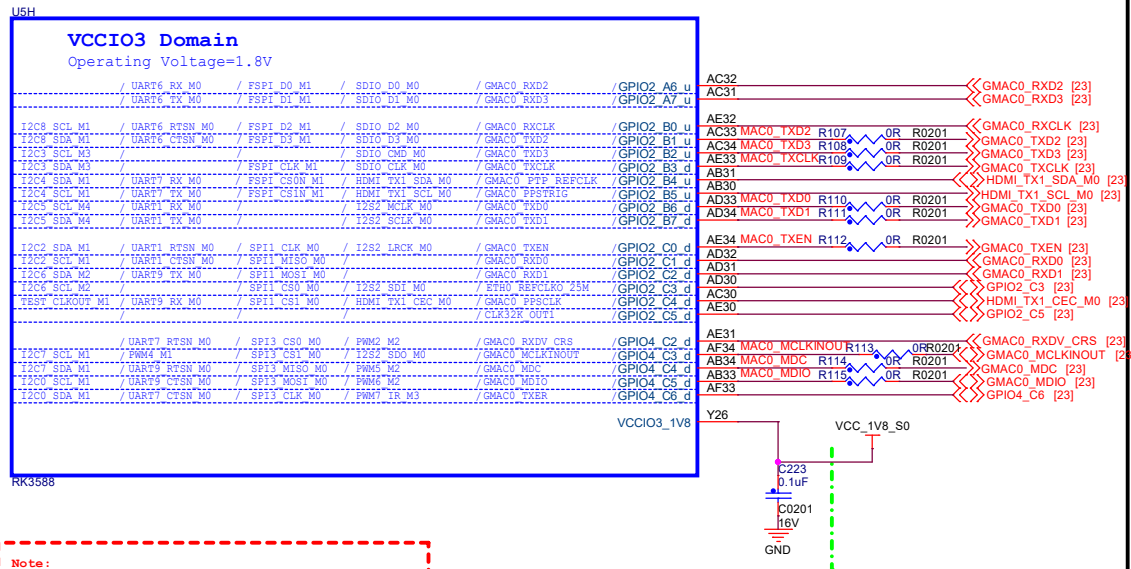
Caps of between dashed green lines and U5 should be placed under the U5 package.
Other caps should be placed close to the U5 package

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Size A3	Document Number RK3588 DDR Controller	Rev V1.0
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RK3588 VCCIO1



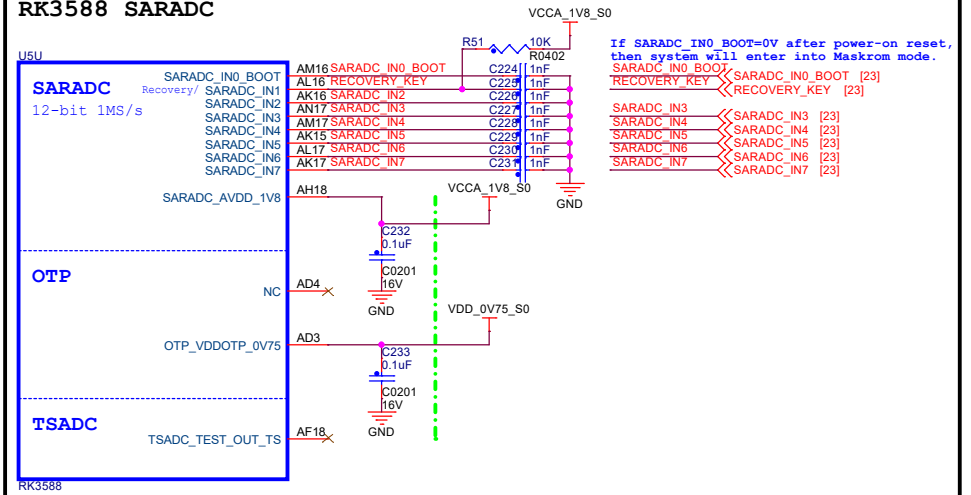
RK3588 VCCIO3



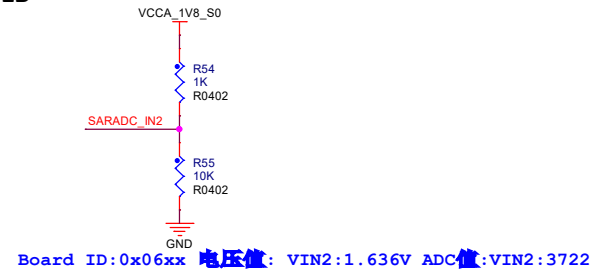
Note:

Caps of between dashed green lines and U5 should be placed under the U5 package.
Other caps should be placed close to the U5 package

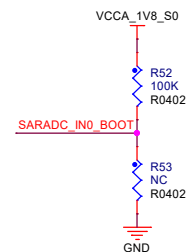
RK3588 SARADC



BOARD ID



BOOT MODE CONFIG

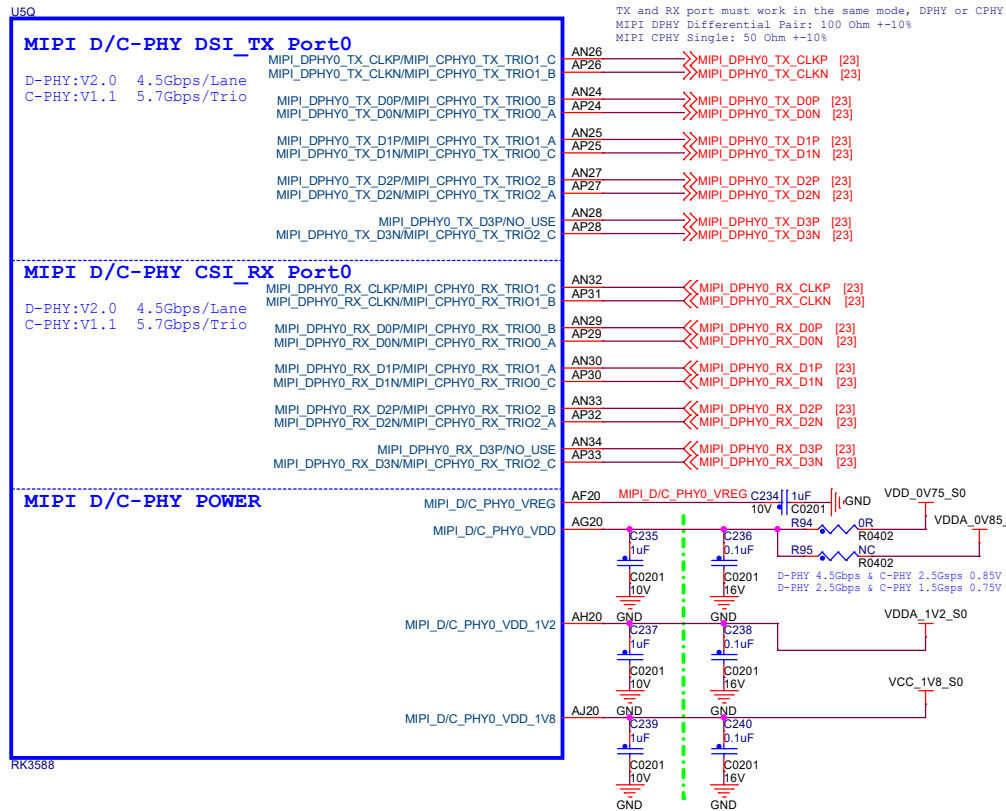


Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0-EMMC-SD Card-USB

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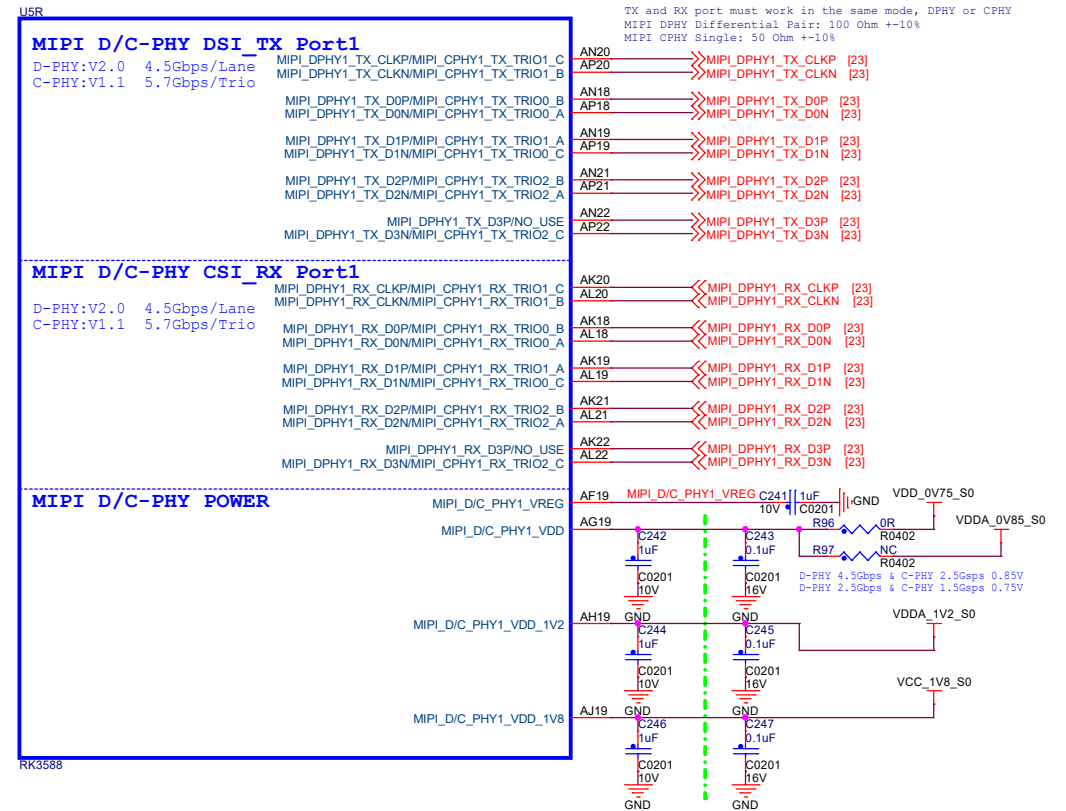
Title 野火鲁班猫5.BTB核心板		
Size A3	Document Number RK3588 VCCIO1/VCCIO3/SARADC	Rev V1.0
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RK3588 MIPI_D/C_PHY0



RK3588

RK3588 MIPI_D/C_PHY1



RK3588

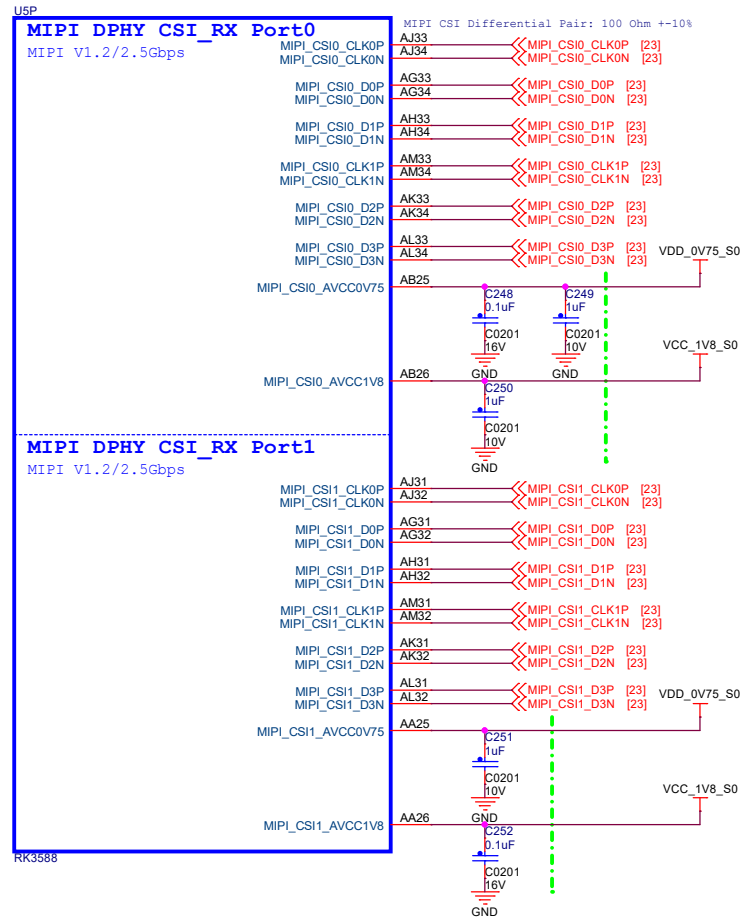
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Size A3	Document Number RK3588 MIPI_D/C_PHY0/1	Rev V1.0
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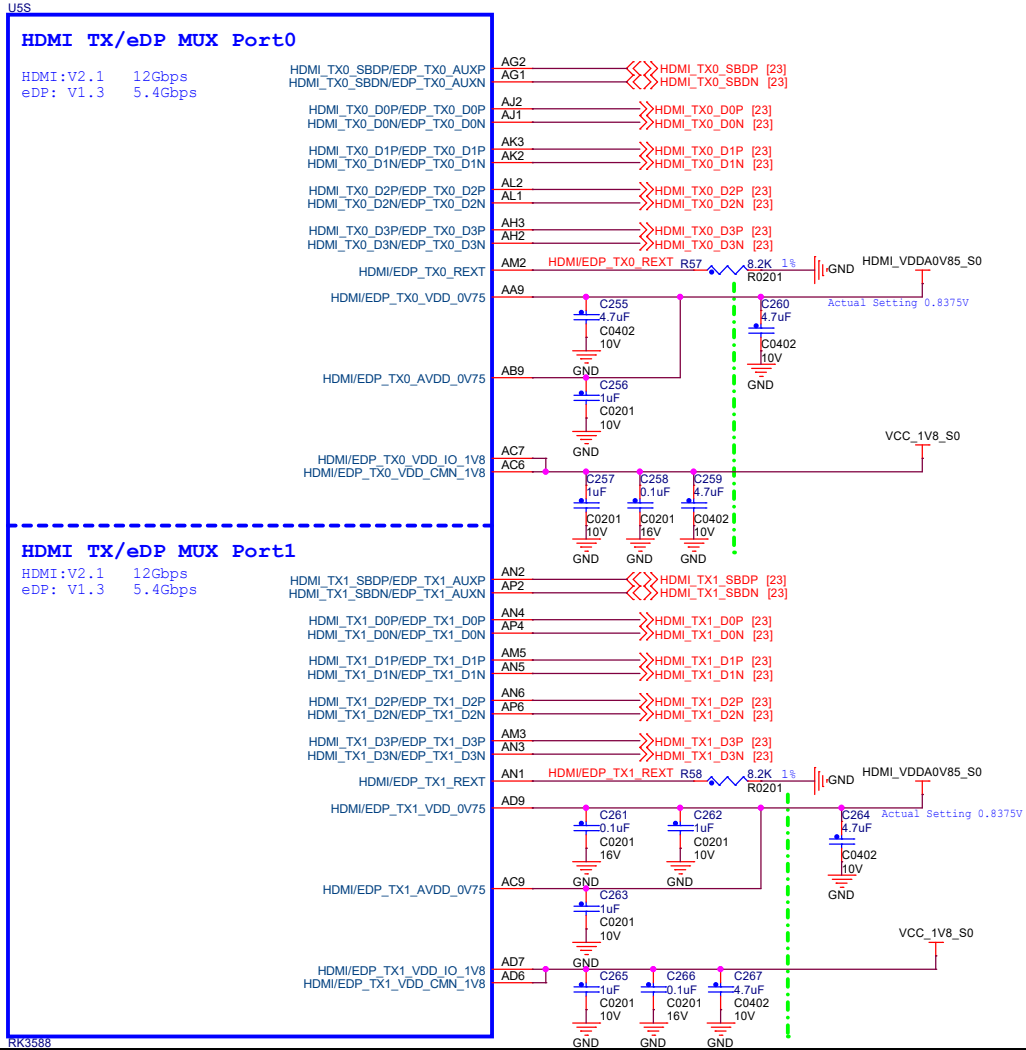
RK3588 MIPI_CSI_RX_PHY

MIPI_CSI_RX Configuration

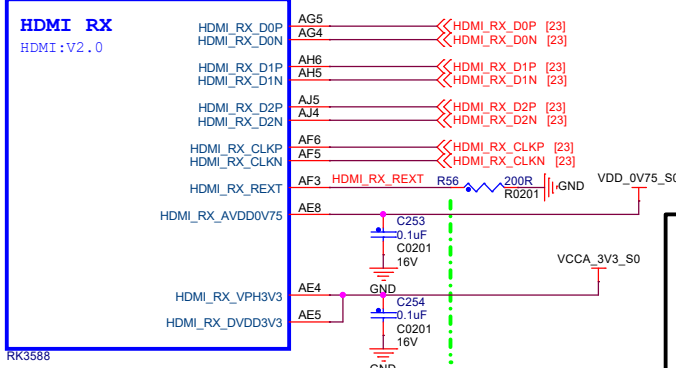
Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1



RK3588 HDMI2.1 TX

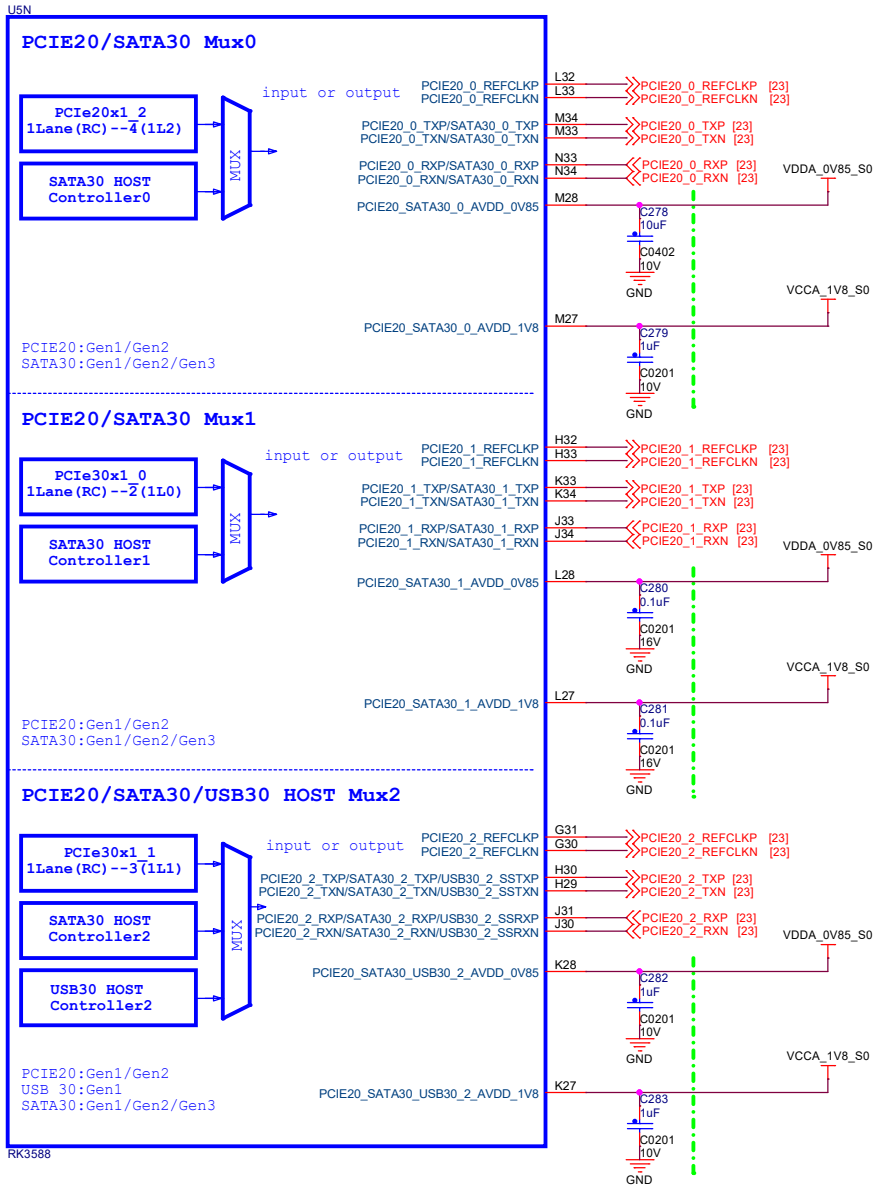


RK3588 HDMI2.0 RX

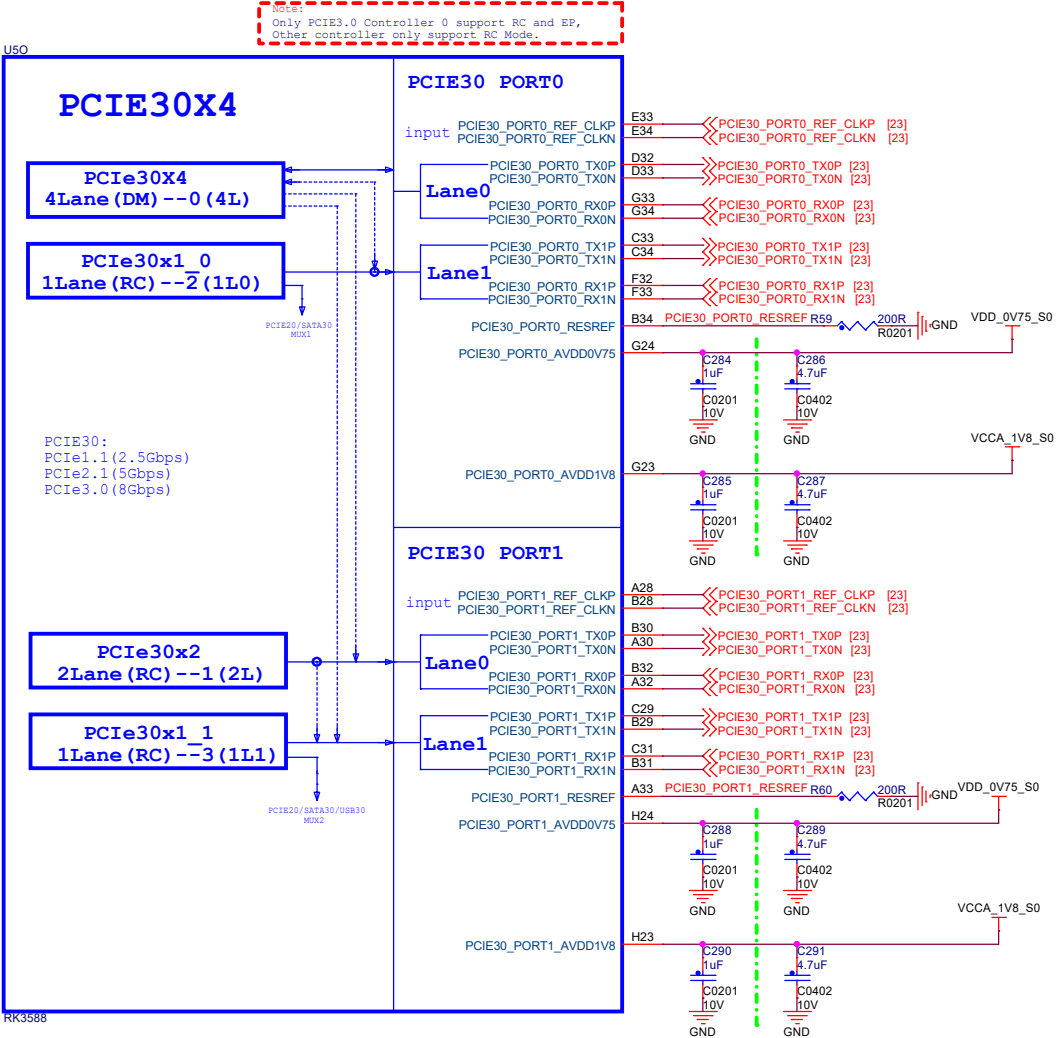


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RK3588 PCIe2.0



RK3588 PCIe3.0



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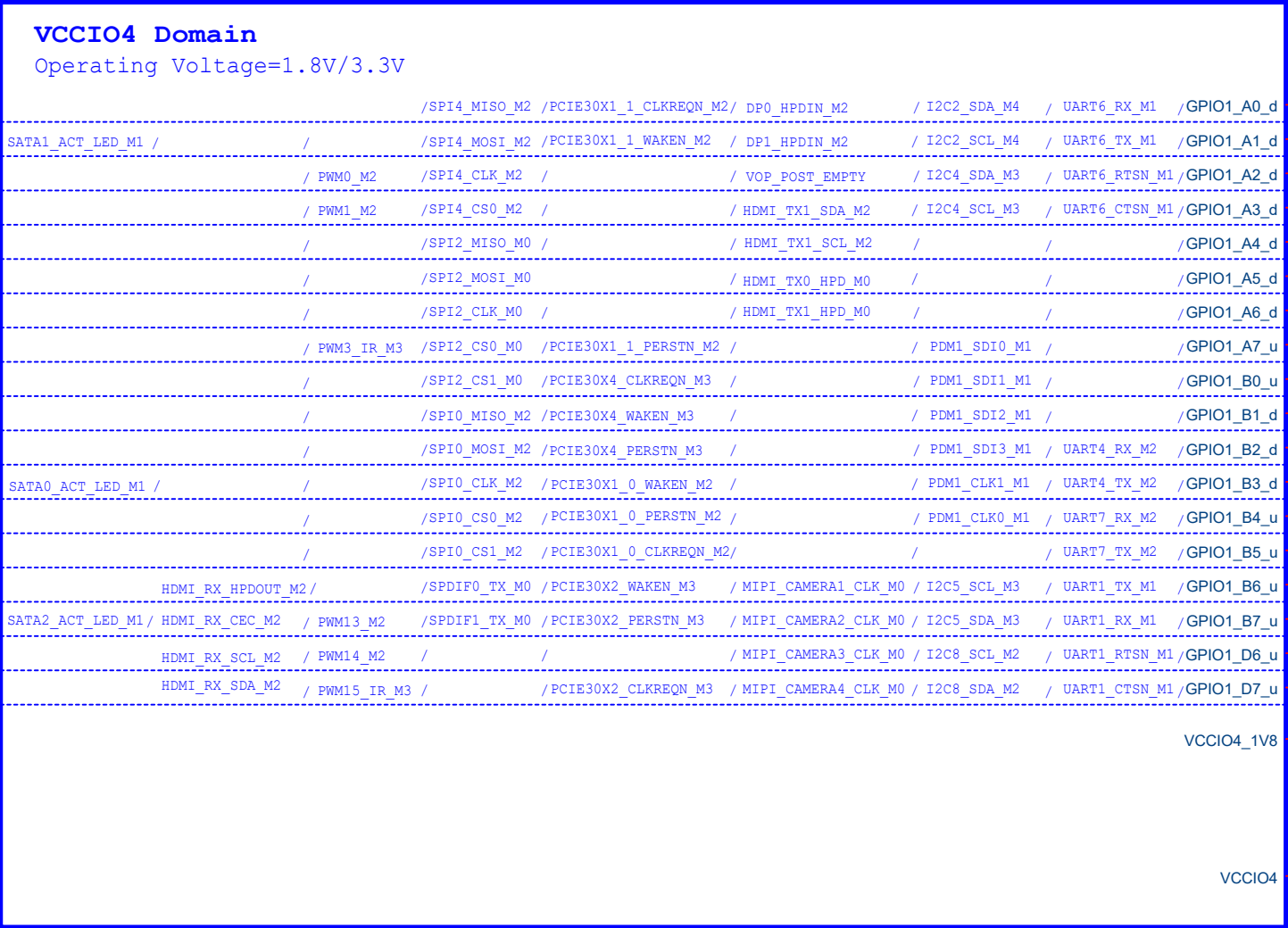
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野火鲁班猫5.BTB核心板

Size A3	Document Number RK3588 PCIe2.0/PCIe3.0	Rev V1.0
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RK3588 VCCIO4

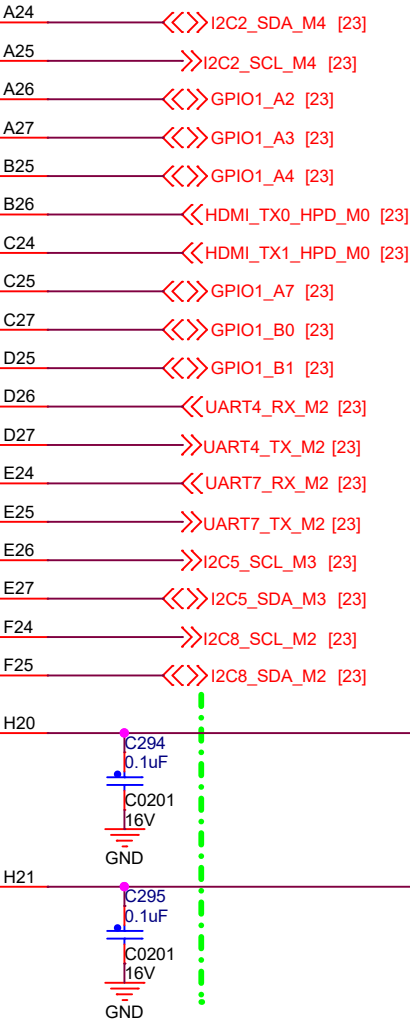
U5I



RK3588

VCCIO4_1V8

VCCIO4



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RK3588 VCCIO5

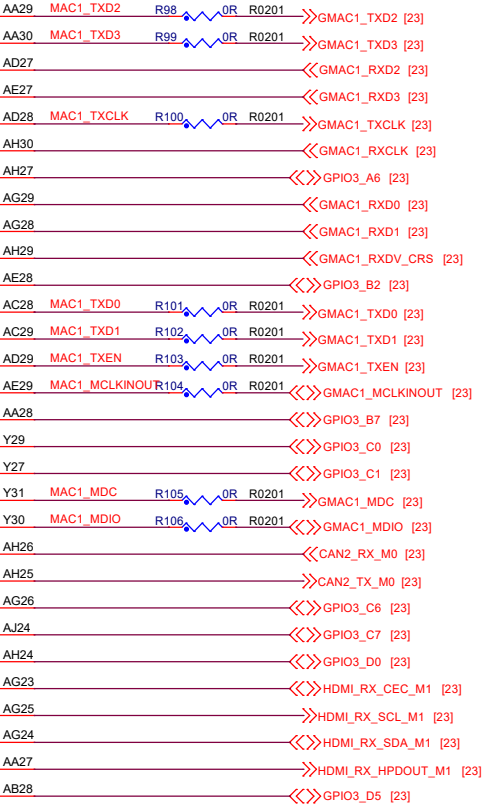
U5J

VCCIO5 Domain
Operating Voltage=1.8V/3.3V

PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/ FSPI_D0_M2	/ I2S3_MCLK	/ SDIO_D0_M1	/ GMAC1_TXD2	/ GPIO3_A0_u
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_D1_M2	/ I2S3_SCLK	/ SDIO_D1_M1	/ GMAC1_TXD3	/ GPIO3_A1_u
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_TX_M1	/	/ FSPI_D2_M2	/ I2S3_LRCK	/ SDIO_D2_M1	/ GMAC1_RXD2	/ GPIO3_A2_u
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S3_SDO	/ SDIO_D3_M1	/ GMAC1_RXD3	/ GPIO3_A3_u
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/ I2S3_SDI	/ SDIO_CMD_M1	/ GMAC1_TXCLK	/ GPIO3_A4_d
	/ MIPI_CAMERA0_CLK_M1	/ UART9_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d
	/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/ ETH1_REFCLK0_25M	/	/ GPIO3_A6_d
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXD0	/ GPIO3_A7_u
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/	/	/ GMAC1_RXD1	/ GPIO3_B0_u
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_TX_M2	/	/	/	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/ I2S2_SDI_M1	/	/ GMAC1_TXER	/ GPIO3_B2_d
	/	/ UART2_RTSN	/	/	/ I2S2_SDO_M1	/	/ GMAC1_TXD0	/ GPIO3_B3_u
	/	/ UART2_CTSN	/	/	/ I2S2_MCLK_M1	/	/ GMAC1_TXD1	/ GPIO3_B4_u
PWM12_M0	/ CAN1_RX_M0	/ UART3_TX_M1	/	/	/ I2S2_SCLK_M1	/	/ GMAC1_TXEN	/ GPIO3_B5_u
PWM13_M0	/ CAN1_TX_M0	/ UART3_RX_M1	/	/	/ I2S2_LRCK_M1	/	/ GMAC1_MCLKINOUT	/ GPIO3_B6_d
	/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_TX1_HPD_M1	/	/ GMAC1_PTP_REF_CLK	/ GPIO3_B7_d
	/	/ UART7_TX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/ GMAC1_PPSTRIG	/ GPIO3_C0_d
	/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPSCCLK	/ GPIO3_C1_d
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_TX_M1	/ FSPI_CS0N_M2	/ SPI3_CS0_M3	/ HDMI_TX1_CEC_M2	/	/ CIF_D8	/ GPIO3_C4_u
CAN2_TX_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1N_M2	/ SPI3_CS1_M3	/ HDMI_TX1_SDA_M1	/	/ CIF_D9	/ GPIO3_C5_u
	/ PCIE30X4_PERSTN_M2	/	/	/ SPI3_MISO_M3	/ HDMI_TX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u
	/ PCIE20X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_TX0_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u
PWM8_M2	/ PCIE20X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/ HDMI_TX0_SDA_M2	/	/ CIF_D12	/ GPIO3_D0_u
PWM9_M2	/ PCIE20X1_2_PERSTN_M0	/ UART4_TX_M1	/	/ SPI0_MISO_M3	/ HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d
	/ PCIE30X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SCL_M2	/ SPI0_MOSI_M3	/ HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M3	/ HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_d
	/ PCIE30X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI0_CS0_M3	/ HDMI_RX_HPDOUT_M1	/ MCU_UTAG_TCK_M1	/	/ GPIO3_D4_d
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART9_TX_M2	/	/ SPI0_CS1_M3	/ DPI_HPDIN_M0	/ MCU_UTAG_TMS_M1	/	/ GPIO3_D5_d

VCCIO5_1V8

VCCIO5

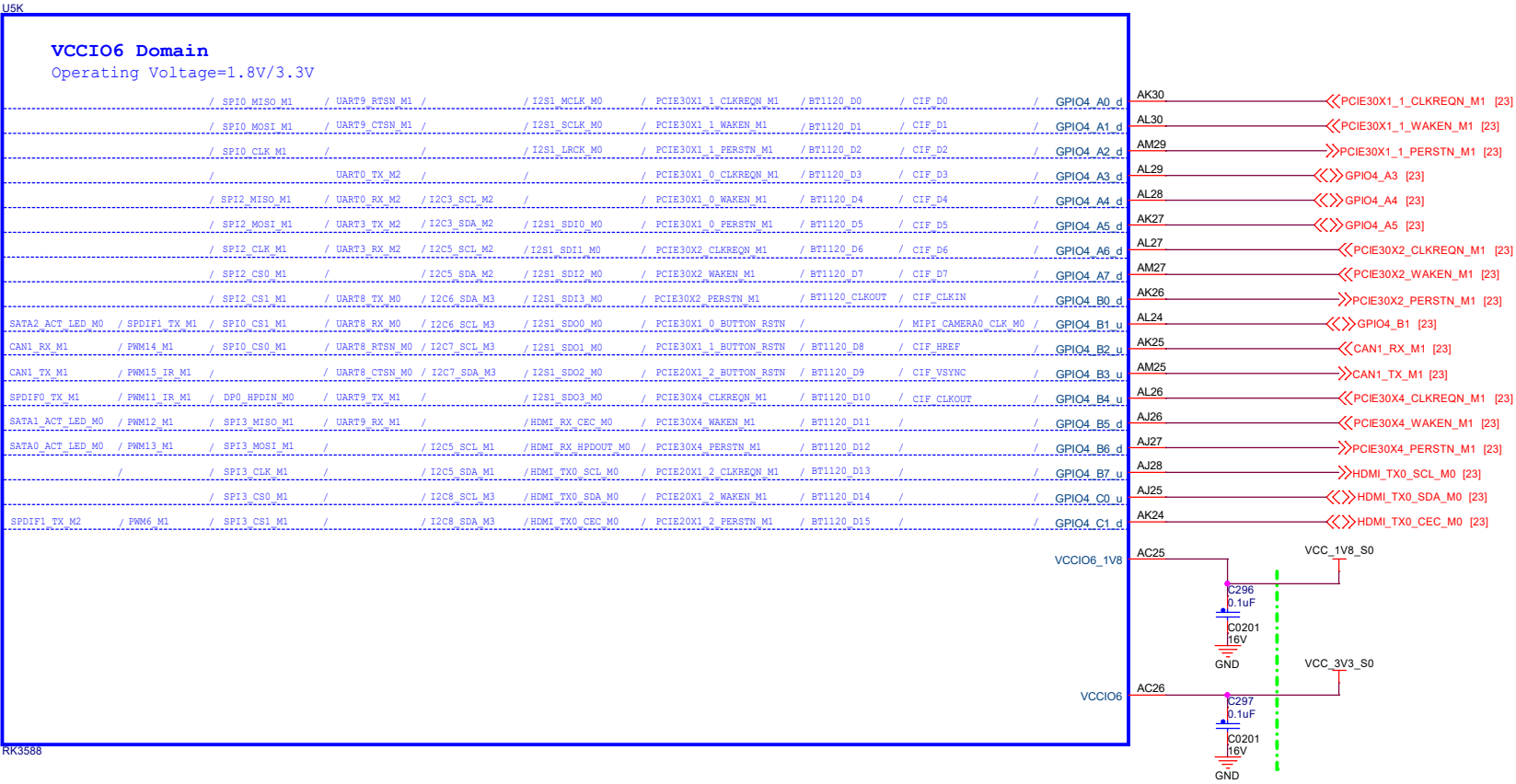


RK3588

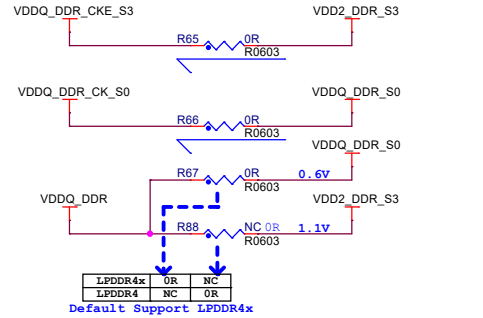
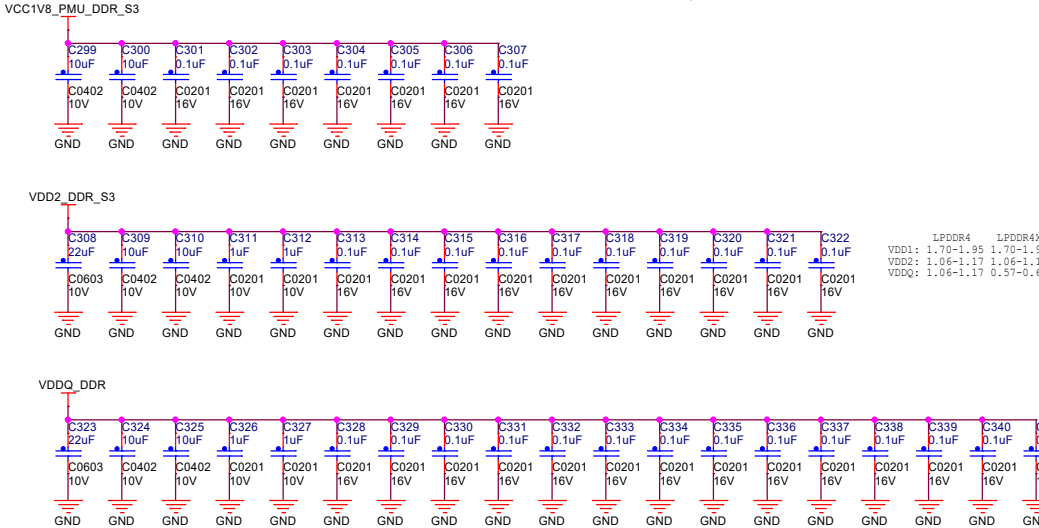
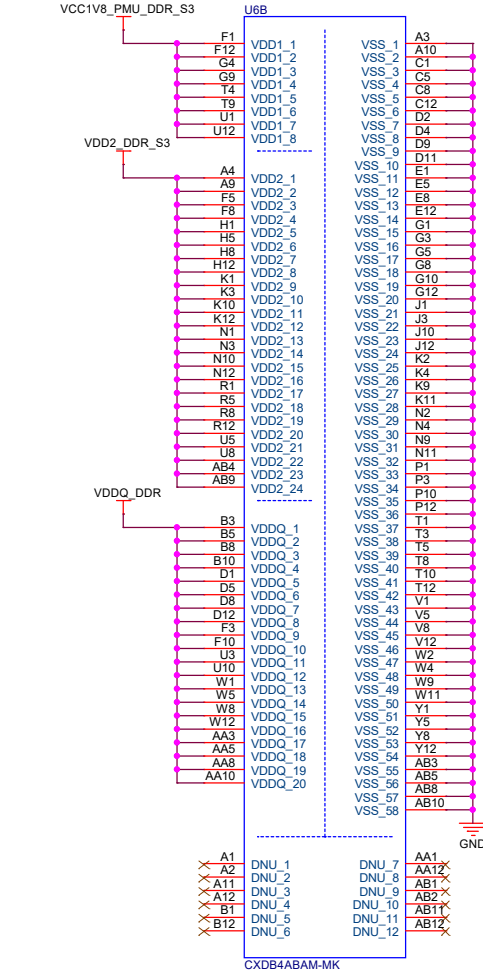
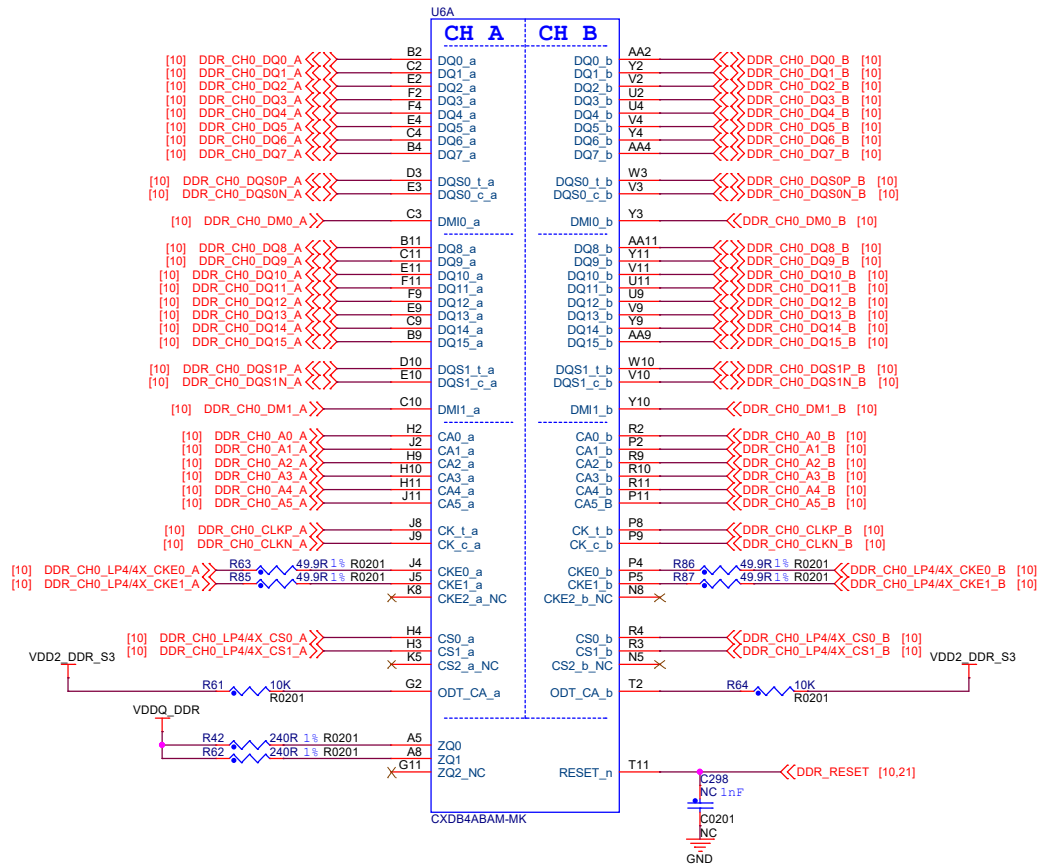
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Size A3	Document Number RK3588 VCCIO5	Rev V1.0
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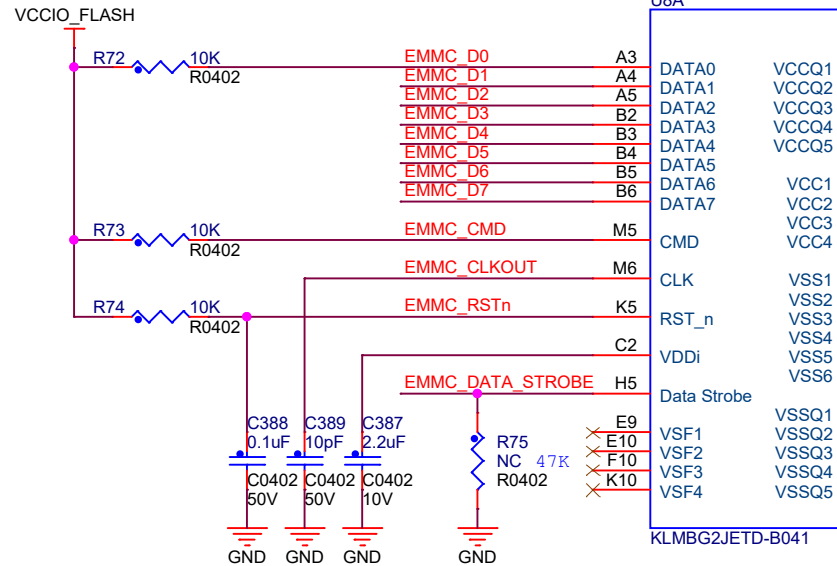
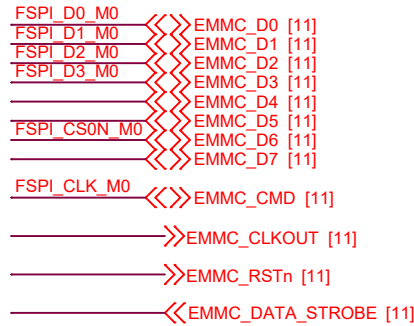
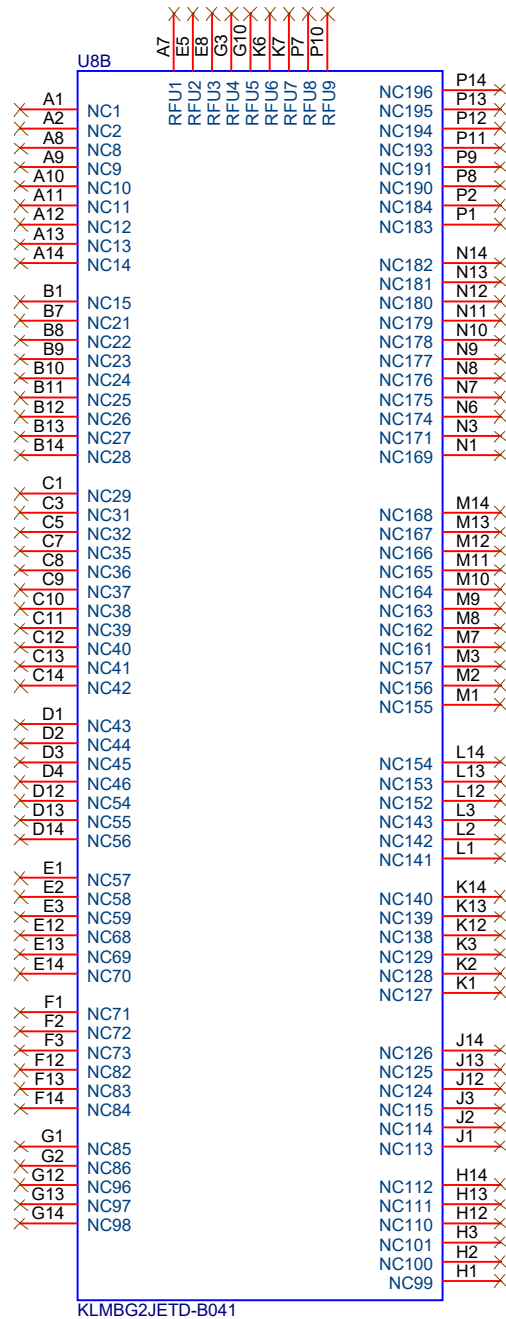
RK3588 VCCIO6



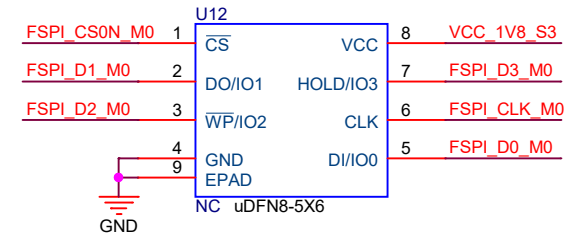
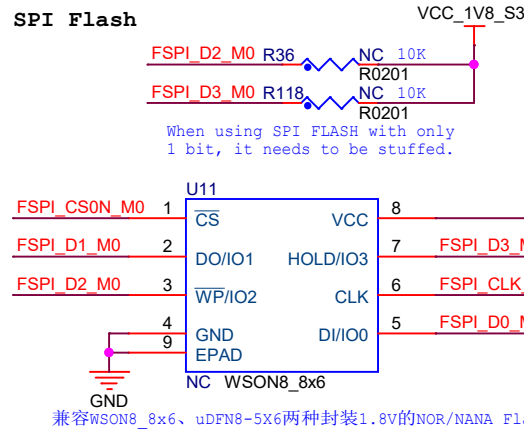
LPDDR4/LPDDR4x_1



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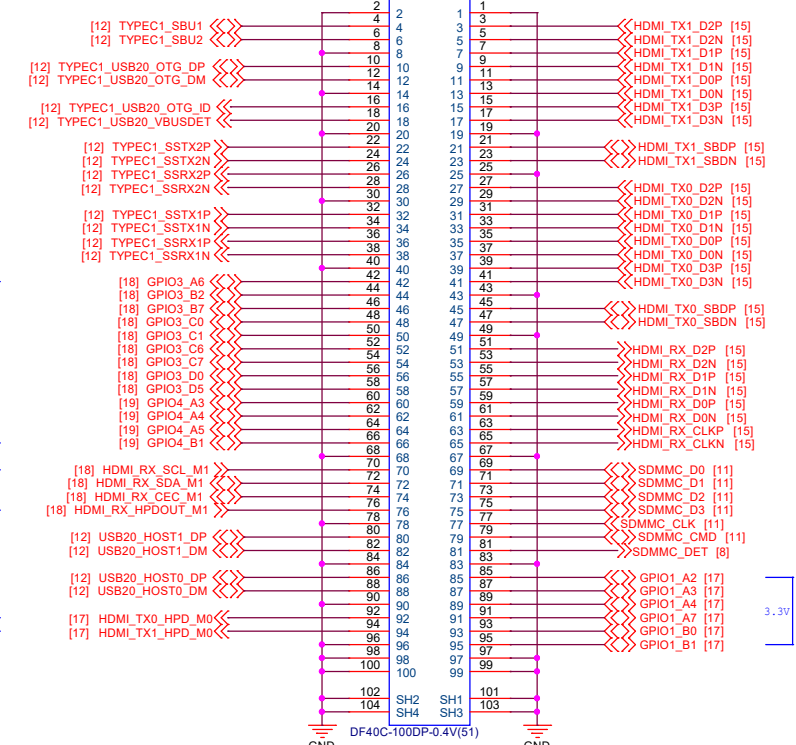
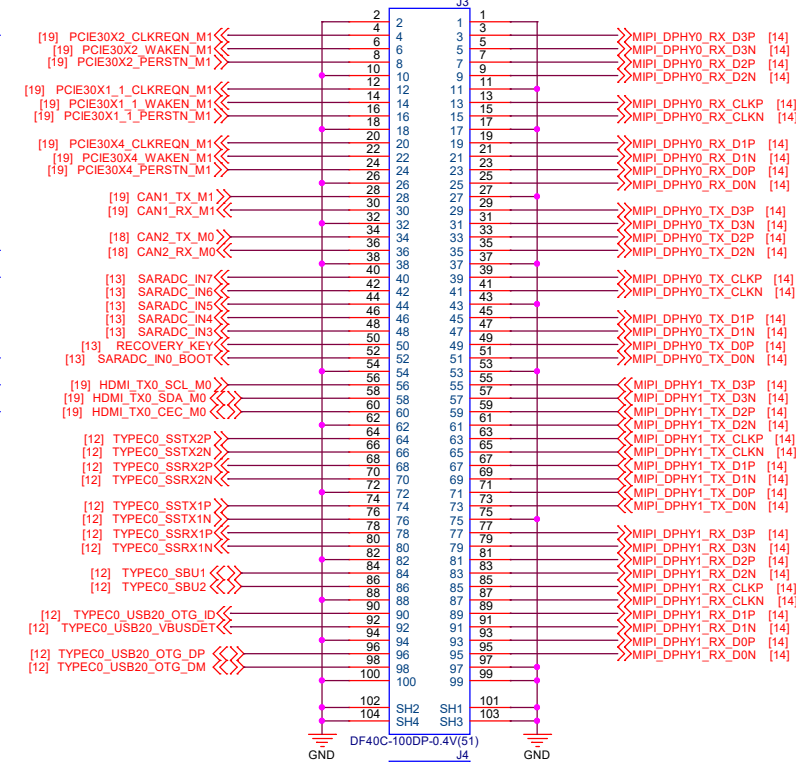
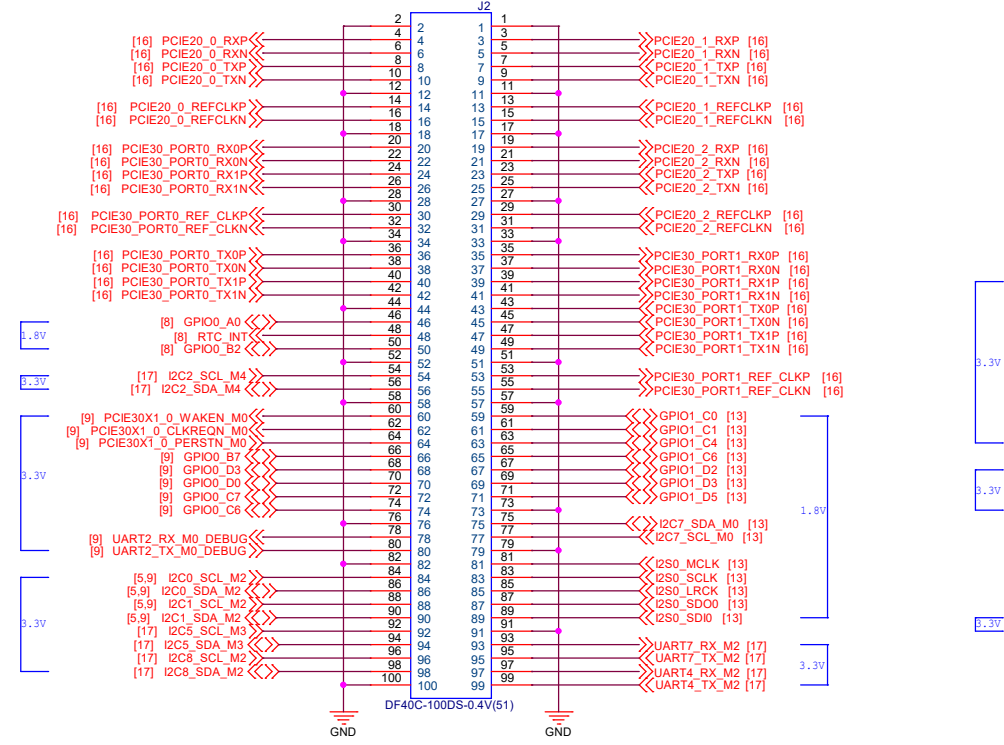
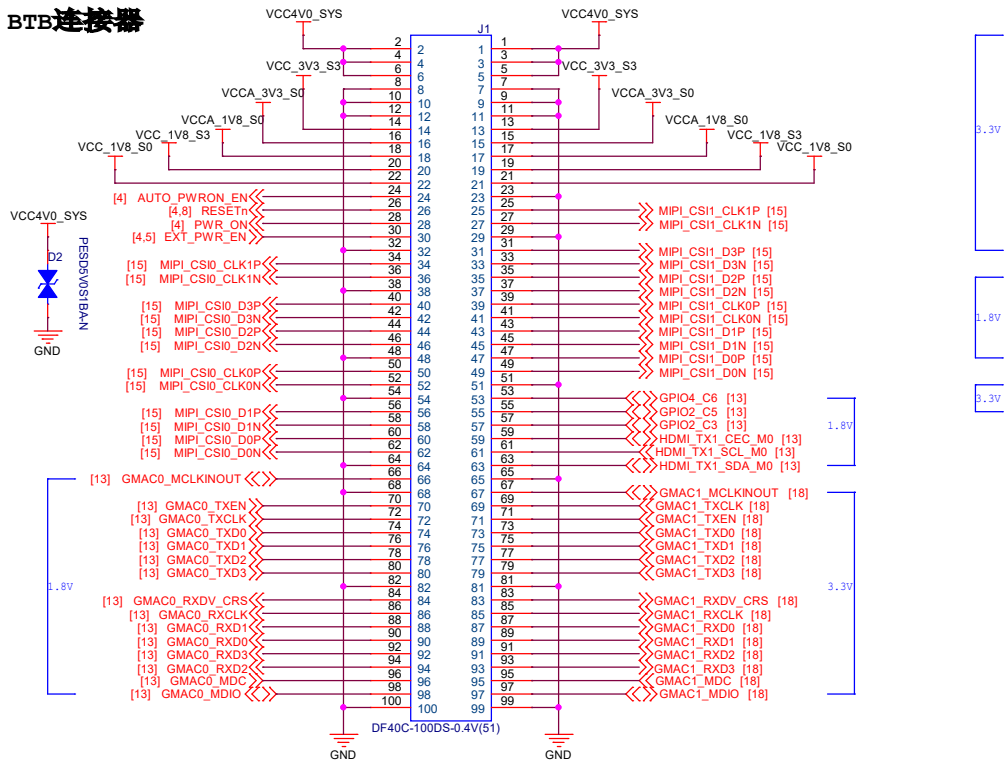


SPI Flash



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BTB连接器



屏蔽夹

Diagram showing the use of shielding clips (屏蔽夹) to connect the BTB connector pins to the PCB pads. The clips are labeled J5, J6, J7, J8, and J9. Each clip is shown with its pin numbers and the corresponding PCB pad connections.

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