

野火_RK3568 LubanCat 2 N_原理图_V1.3

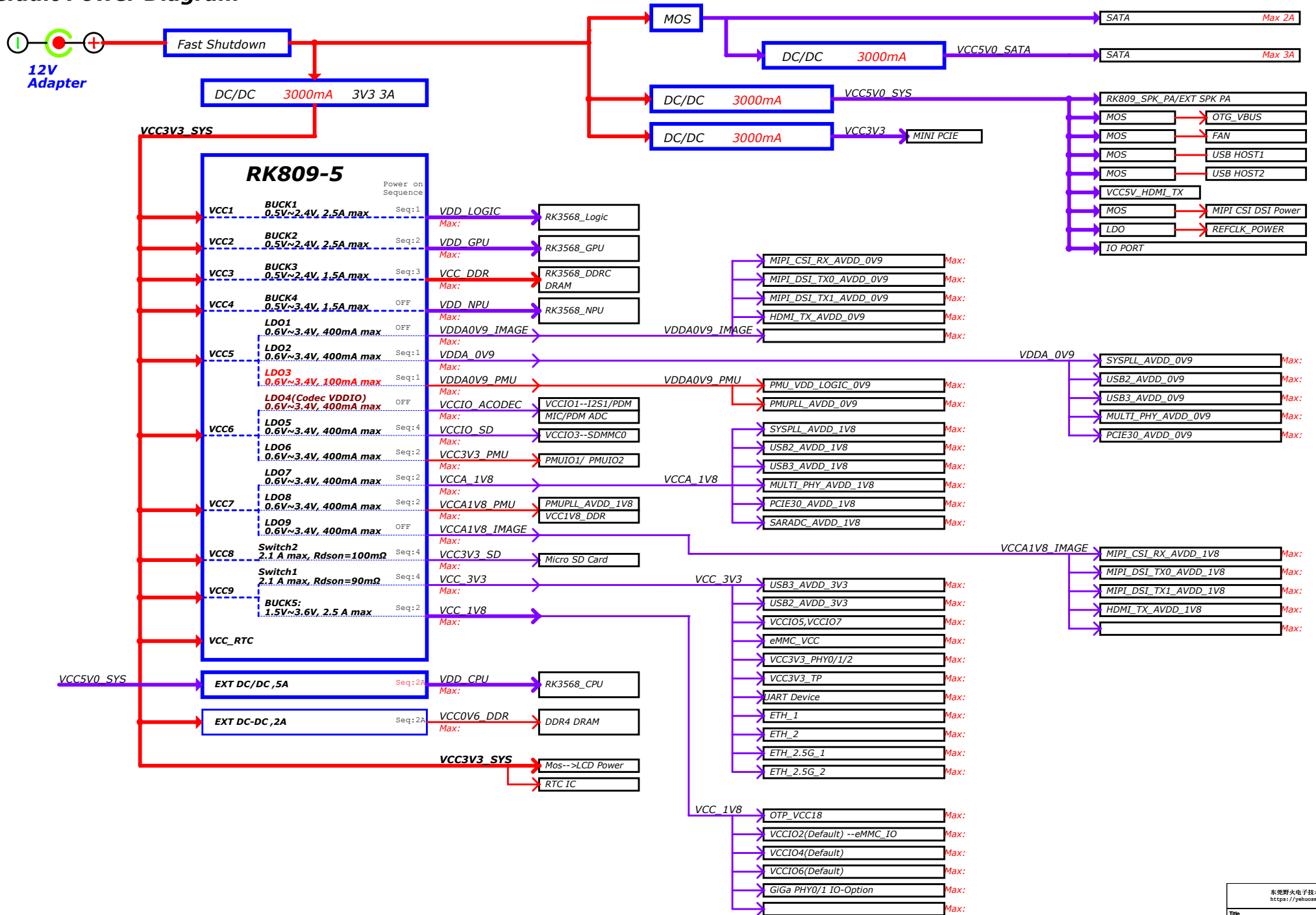
目录

Page 1	Content	Page 27	ETH_2.5G_1
Page 2	Historic Version	Page 28	ETH_2.5G_2
Page 3	POWER DIAGRAM	Page 29	MINI_PCIE_PORT
Page 4	DC_IN/OTG_Download	Page 30	Earphone/DEBUG/IO_PORT/LED
Page 5	PMIC_DCDC/LDO	Page 31	
Page 6	PMIC_Managerment/CODE		
Page 7	Power_other		
Page 8	RK3568_Power/GND		
Page 9	DDR_PHY		
Page 10	LPDDR4/4x		
Page 11	RK3566_OSC/PLL/PMUIO		
Page 12	EMMC/SD Controller		
Page 13	USB/PCIE/SATA_PHY		
Page 14	SARADC/GPIO		
Page 15	VI Interface		
Page 16	VO Interface_1		
Page 17	VO Interface_2		
Page 18	Audio Interface		
Page 19	EMMC_FLASH		
Page 20	ETH_1		
Page 21	ETH_2		
Page 22	USB_PORT		
Page 23	HDMI_PORT/SATA_PORT		
Page 24	MIPI_DSI/MIPI_CSI_PORT 1		
Page 25	MIPI_DSI/MIPI_CSI_PORT 2		
Page 26	PCIE3.0_REFCLK		

历史版本

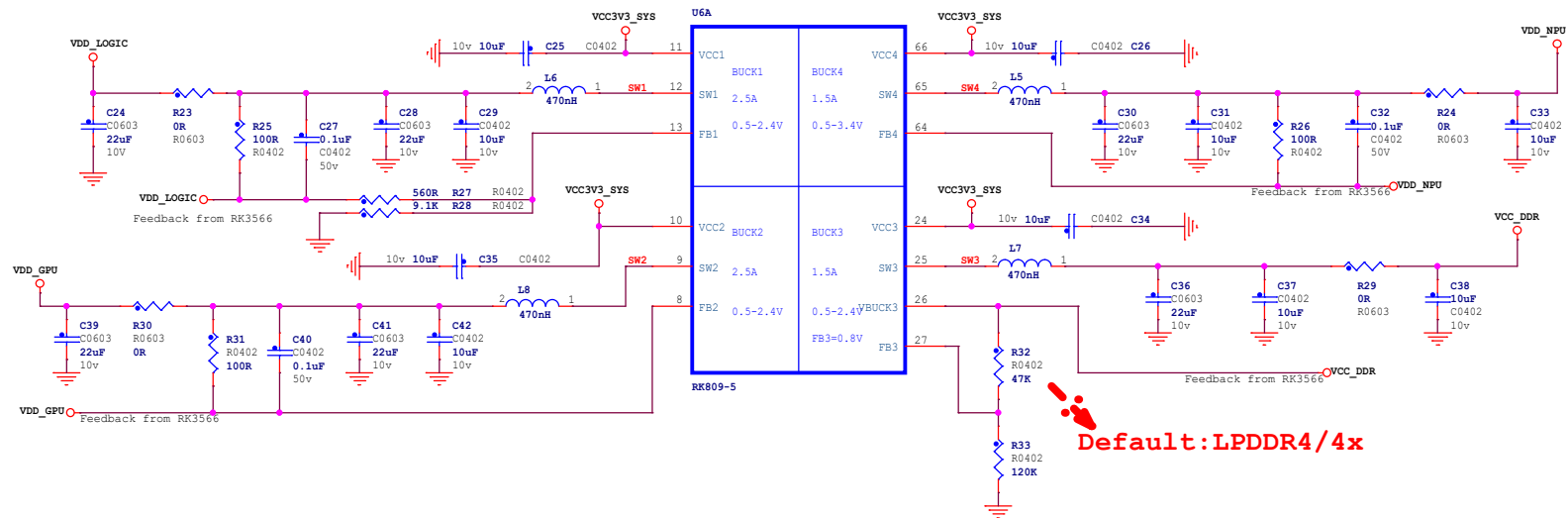
版本号	日期	设计	描述
V0.1	2022-05-05	ghs	初始版本
V1.0	2022-09-09	ghs	修正U27开启信号接反的问题，解决调试接口漏电的问题
V1.1	2022-09-09	ghs	修正BOARD ID的ID识别电阻的电源域，修正PHY芯片的复位引脚电压不匹配问题
V1.2	2022-12-13	ghs	增加网卡上拉电阻，更新mini pcie的固定螺丝柱
V1.3	2023-07-13	ghs	新增一个MIPI CSI，一个MIPI DSI

Default Power Diagram



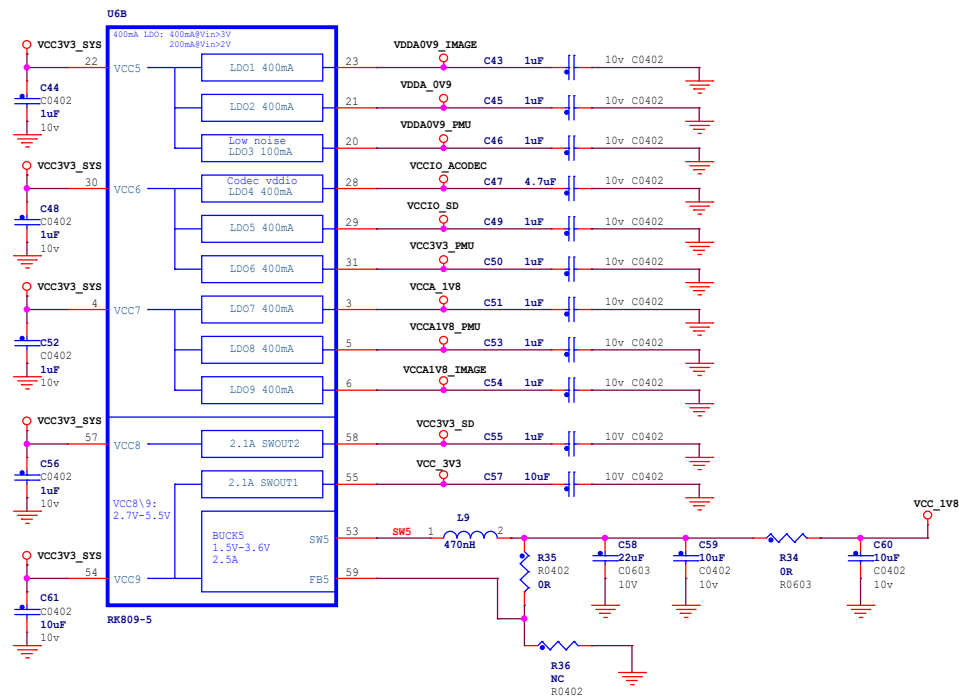
Date: Wednesday, August 23, 2023 Sheet 4 of 29

PMIC RK809 DCDC



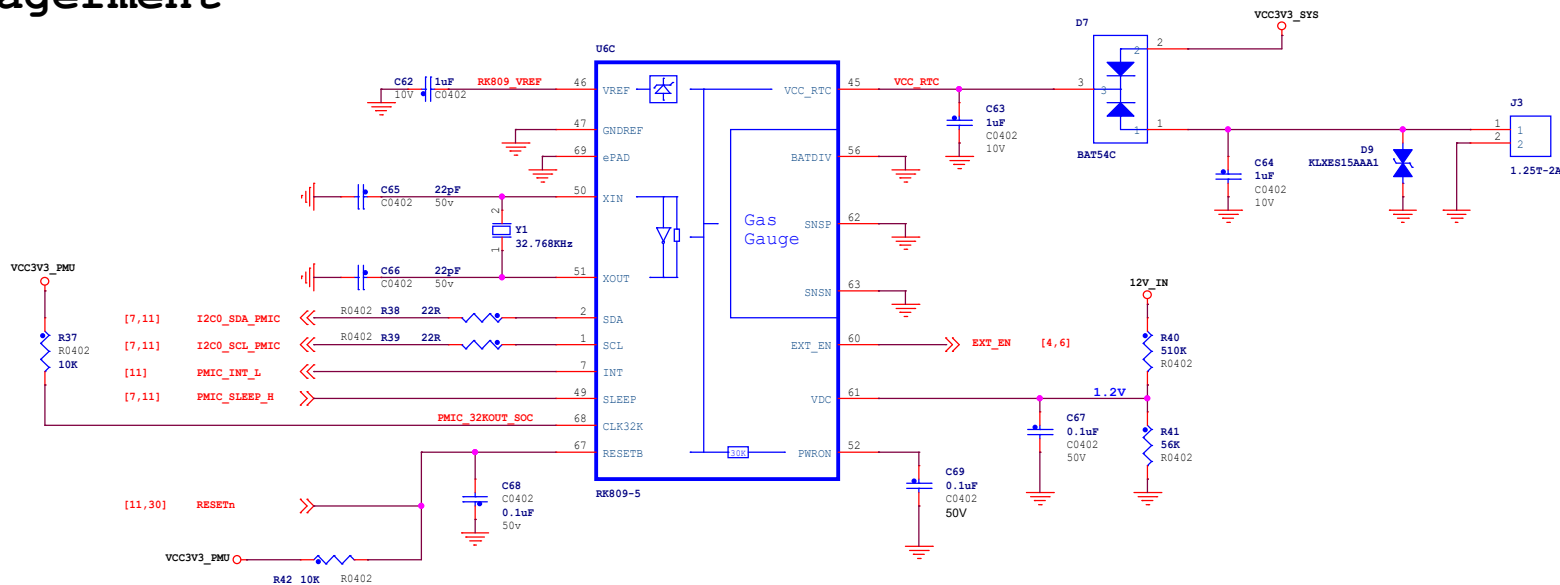
RK3566 BUCK FB

PMIC RK809 LDO

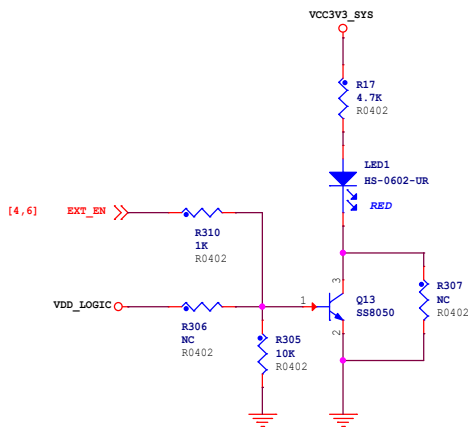


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Title	野火_RK3568 LubanCat 2 H_原理图_V1.3	
Size	Document Number	Rev
A3	PMIC_DCDC/LDO	V1.3
Date: Wednesday, August 23, 2023	Sheet 5	of 29

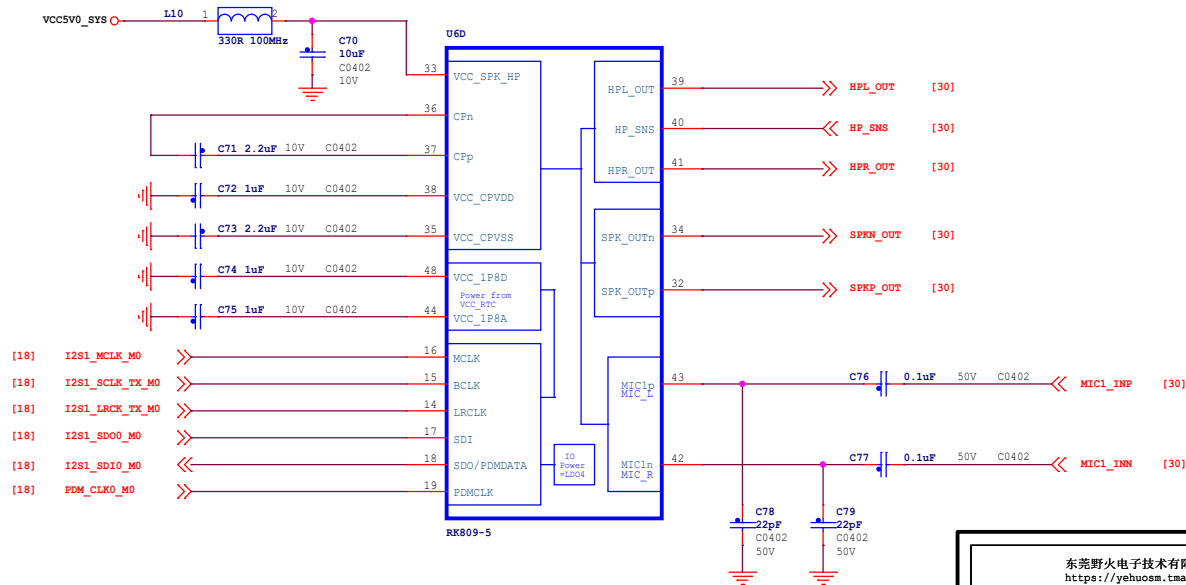
PMIC RK809 Managerment



PWR_LED



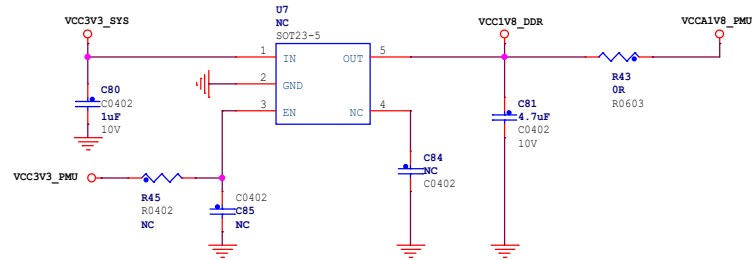
PMIC RK809 CODEC



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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A3	Document Number PMIC_Management/CODE	Rev V1.3
Date: Wednesday, August 23, 2023 Sheet 6 of 29		

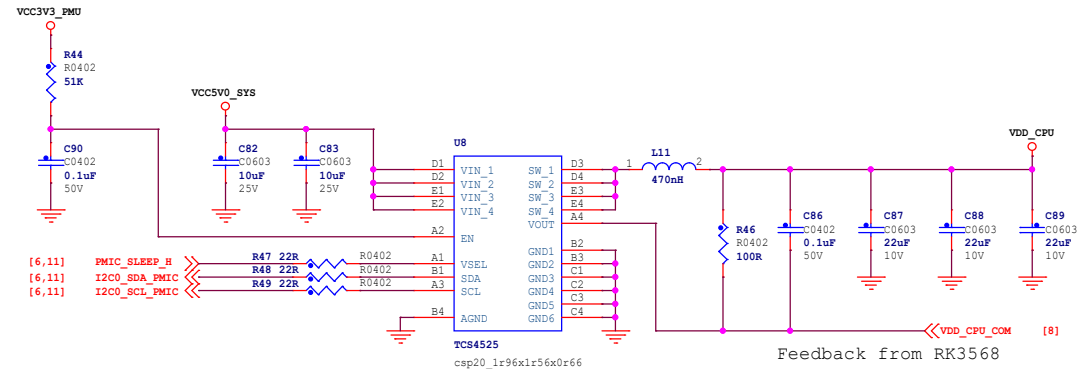
Auxiliary power supply

LPDDR4_VCC1V8_DDR



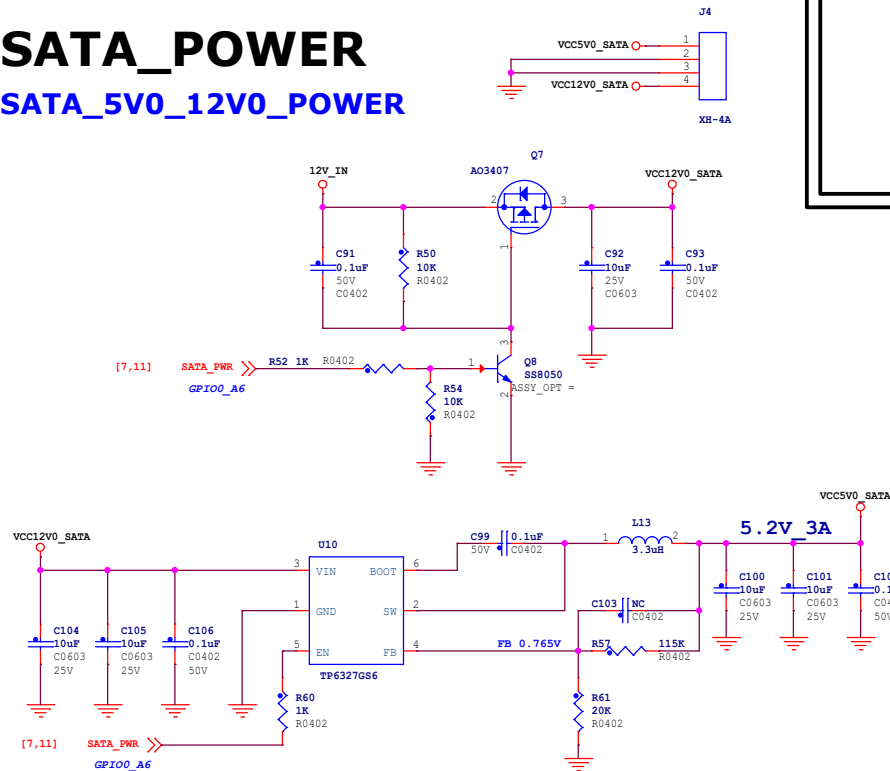
RK3568 CPU Power

VDD_CPU_EXT



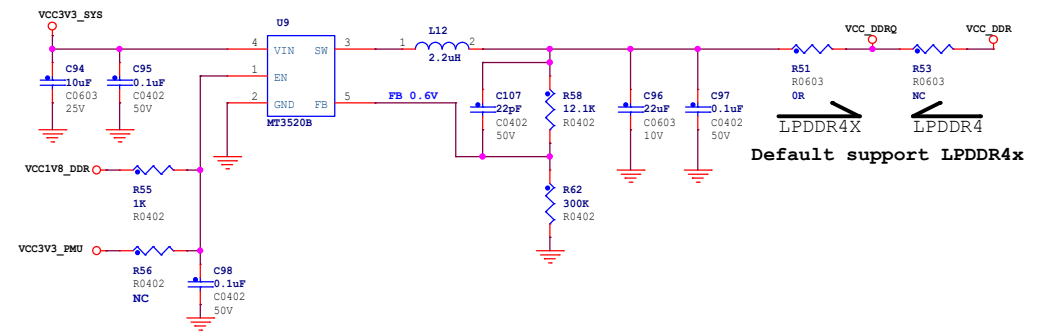
SATA_POWER

SATA_5V0_12V0_POWER



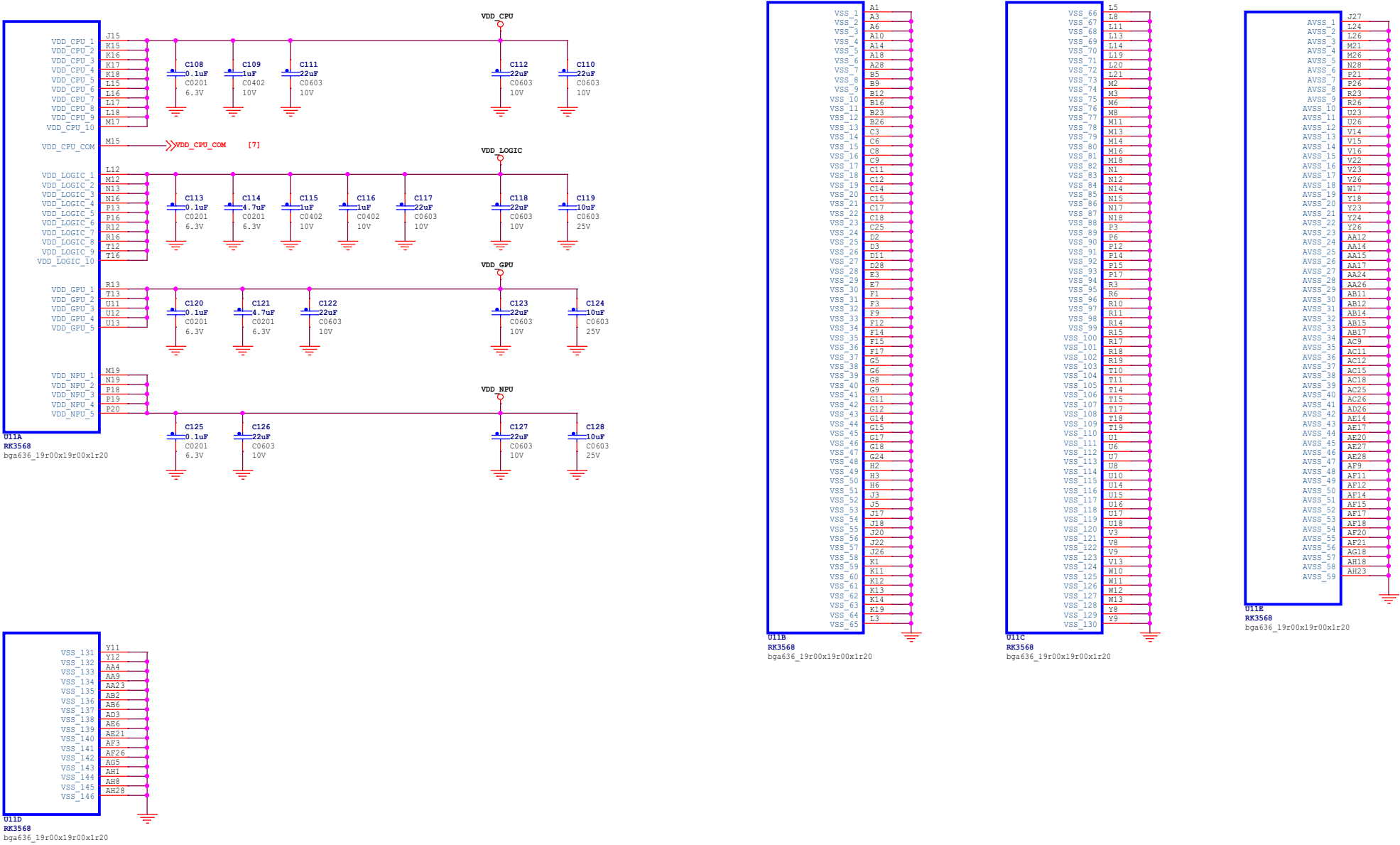
LPDDR4x Power

output: 0.6V

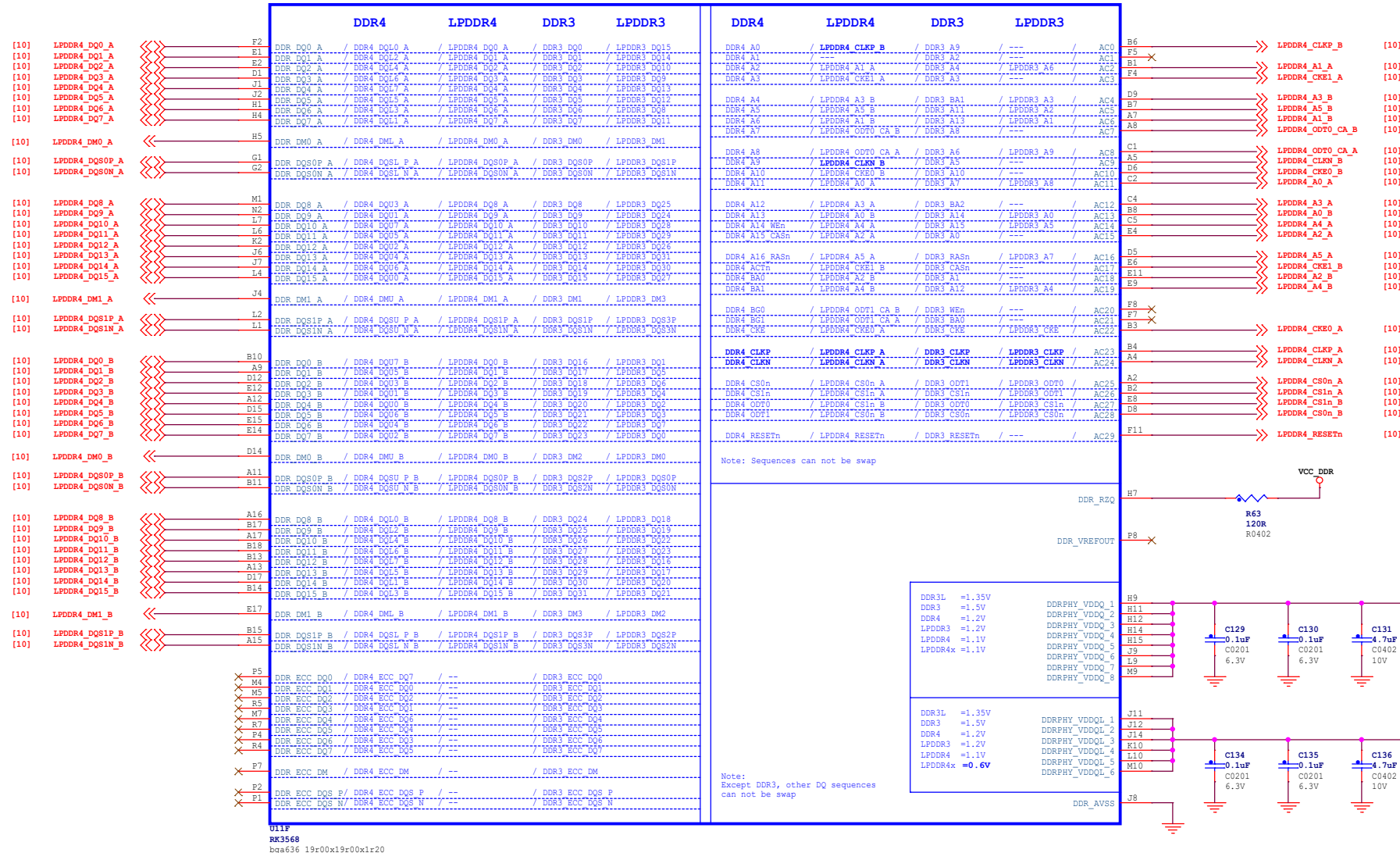


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A3	Power_other	V1.3
Date:	Wednesday, August 23, 2023	Sheet 7 of 29

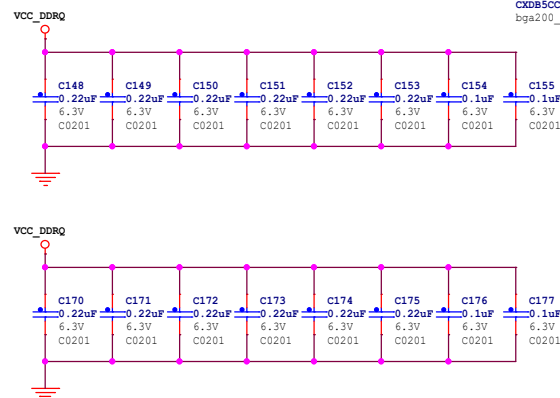
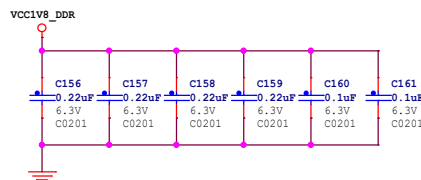
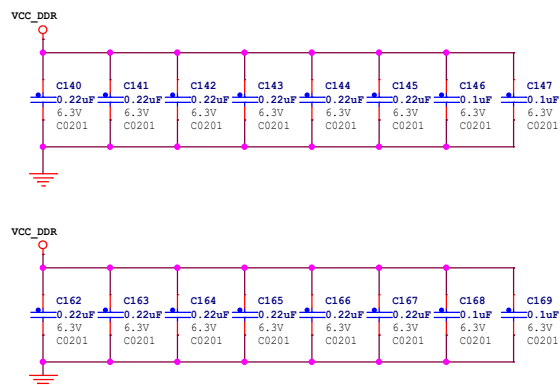
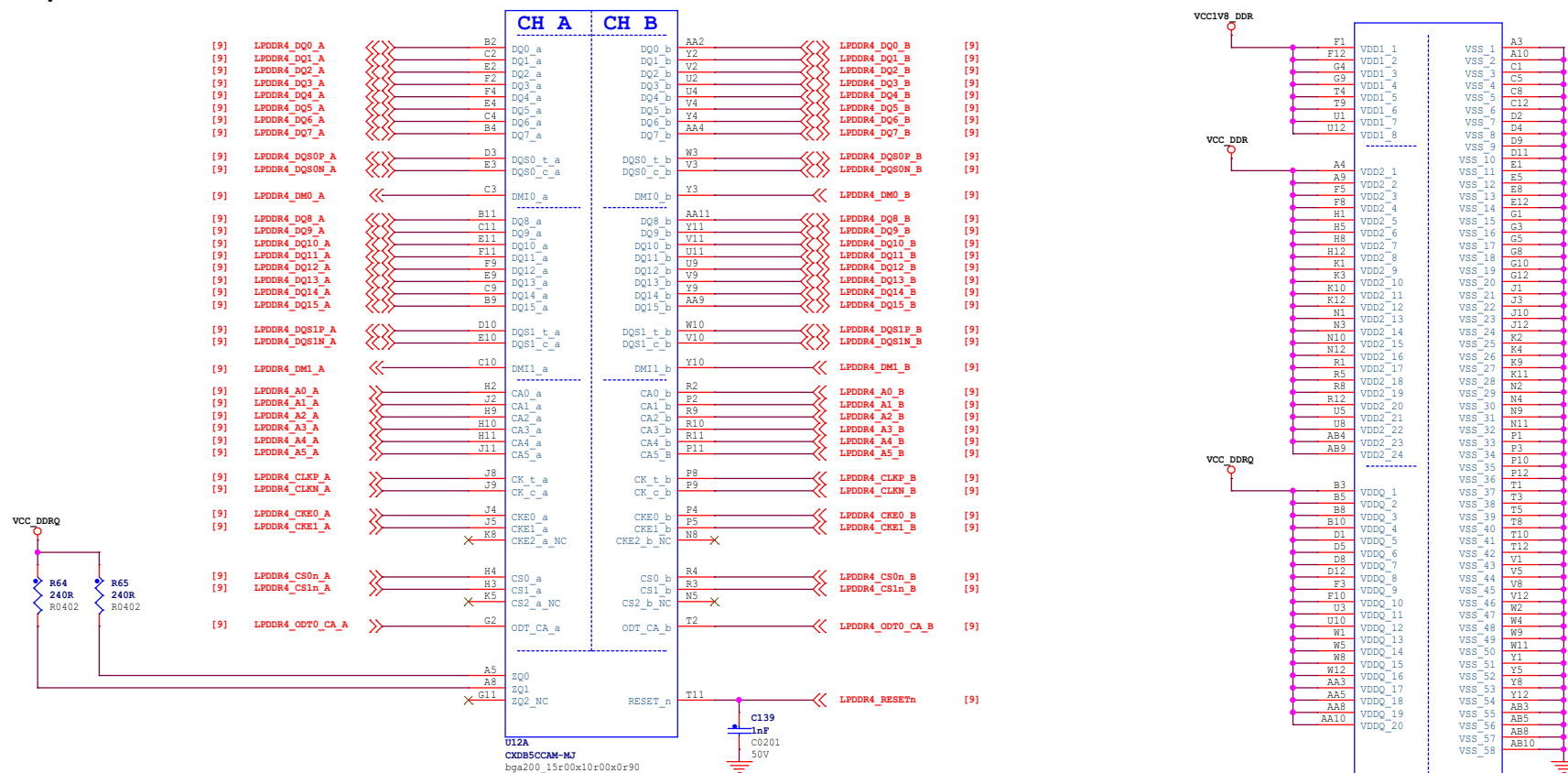
RK3568 Power/GND



RK3568 DDR PHY

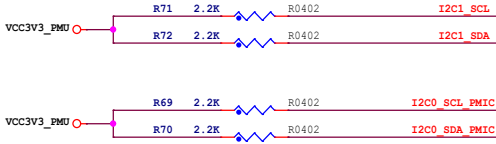
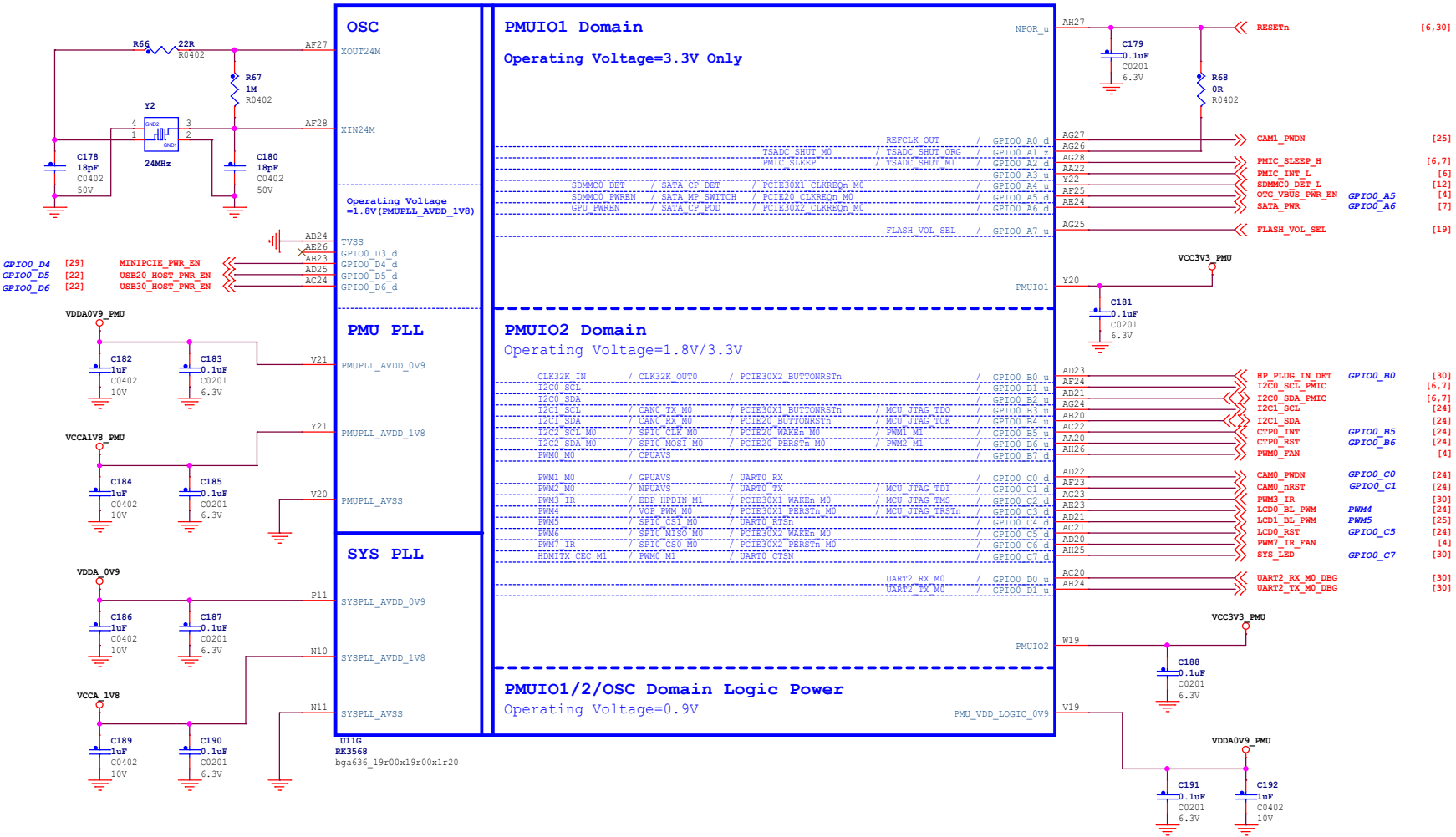


LPDDR4 / 4x



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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3			
Size A3	Document Number LPDDR4/4x		Rev V1.3
Date:	Wednesday, August 23, 2023	Sheet 10 of	29

RK3568 OSC/PLL/PMUIO



RK3568 VCCIO2 Domain

VCCIO2 Domain

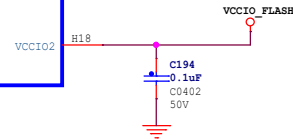
Operating Voltage=1.8V/3.3V

EMMC D0	/ FLASH D0	/ GPIO1 B4 u	A24	EMMC D0	[19]
EMMC D1	/ FLASH D1	/ GPIO1 B5 u	C21	EMMC D1	[19]
EMMC D2	/ FLASH D2	/ GPIO1 B6 u	B24	EMMC D2	[19]
EMMC D3	/ FLASH D3	/ GPIO1 B7 u	D21	EMMC D3	[19]
EMMC D4	/ FLASH D4	/ GPIO1 C0 u	A25	EMMC D4	[19]
EMMC D5	/ FLASH D5	/ GPIO1 C1 u	E21	EMMC D5	[19]
EMMC D6	/ FLASH D6	/ GPIO1 C2 u	E22	EMMC D6	[19]
EMMC D7	/ FLASH D7	/ GPIO1 C3 u	B25	EMMC D7	[19]
EMMC CMD	/ FLASH WRn	/ GPIO1 C4 u	B22	EMMC_CMD	[19]
EMMC CLKOUT	/ FLASH DQS	/ GPIO1 C5 d	A23	EMMC_CLK	[19]
EMMC DATA STROBE	/ FSPI CSIn	/ FLASH CLE	A26	EMMC_STRB	[19]
EMMC RSTn	/ FSPI D2	/ FLASH WPh	F20	EMMC_RST	[19]
FSPI CLK	/ FLASH ALE	/ GPIO1 D0 d	A22		
FSPI D0	/ FLASH RDY	/ GPIO1 D1 u	C24		
FSPI D1	/ FLASH RDn	/ GPIO1 D2 u	C23		
FSPI CSOut	/ FLASH CSOut	/ GPIO1 D3 u	A27		
FSPI D3	/ FLASH CSIn	/ GPIO1 D4 u			

Default is determined by Pin
FLASH VOL_SEL/GPIO0 A7 u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

U117
RK3568
bga636_19r00x19r00x1r20

Resistor close to SOC
terminal



RK3568 VCCIO3 Domain

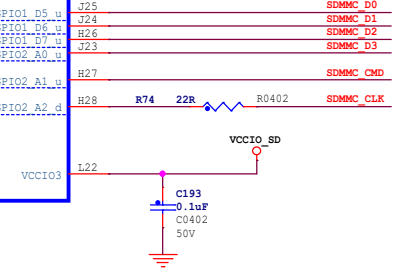
VCCIO3 Domain

Operating Voltage=1.8V/3.3V

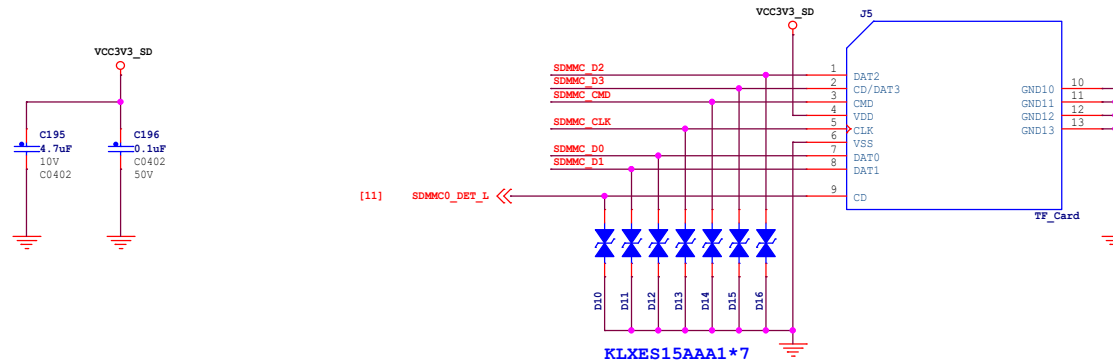
SDMMC0 D0	/ UART2 TX M1	/ UART6 TX M1	/ PWM8 M1	/ GPIO1 D5 u	J25	SDMMC D0
SDMMC0 D1	/ UART2 RX M1	/ UART6 RX M1	/ PWM8 M1	/ GPIO1 D6 u	J24	SDMMC D1
SDMMC0 D2	/ ARMUTAG TCK	/ UART5 CSB M0	/ GPIO1 D7 u	/ GPIO1 D7 u	H26	SDMMC D2
SDMMC0 D3	/ ARMUTAG TMS	/ UART5 RSTn M0	/ GPIO1 D7 u	/ GPIO1 D7 u	J23	SDMMC D3
SDMMC0 CMD	/ PWM10 M1	/ UART5 RX M0	/ CAN0 TX M1	/ GPIO2 A1 u	H27	SDMMC_CMD
SDMMC0 CLK	/ TEST CLKOUT	/ UART5 TX M0	/ CAN0 RX M1	/ GPIO2 A2 d	H28	SDMMC_CLK

U117
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bga636_19r00x19r00x1r20

Resistor close to SOC
terminal



TF_CARD

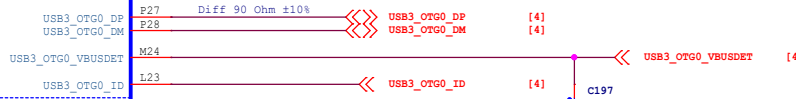


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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A3	Document Number Flash/SD Controller	Rev V1.3
Date: Wednesday, August 23, 2023 Sheet 12 of 29		

RK3568 USB3.0/SATA/QSGMII/PCIe2.0 x1

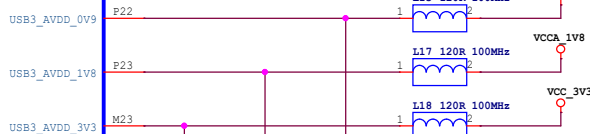
USB3.0 OTG0_HS/FS/LS (USB Download)



USB3.0 HOST1_HS/FS/LS



USB3.0 OTG0/HOST1_ HS/FS/LS Power

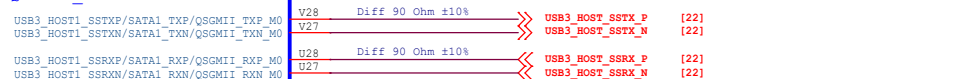


MULTI_PHY0/1/2

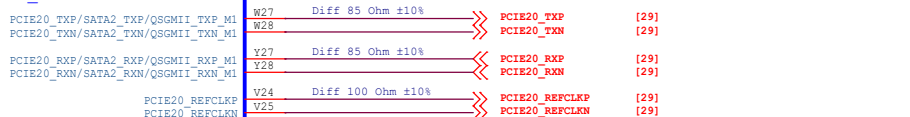
USB3.0 OTG0_SS and SATA0 Mux



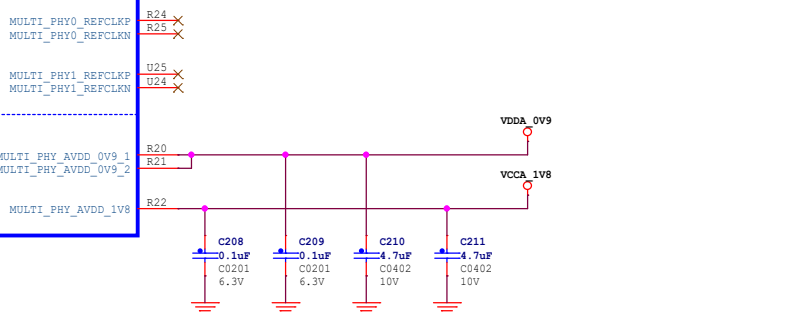
USB3.0 HOST1_SS and SATA1 and QSGMII_M0 Mux



PCIe2.0 and SATA2 and QSGMII_M1 Mux



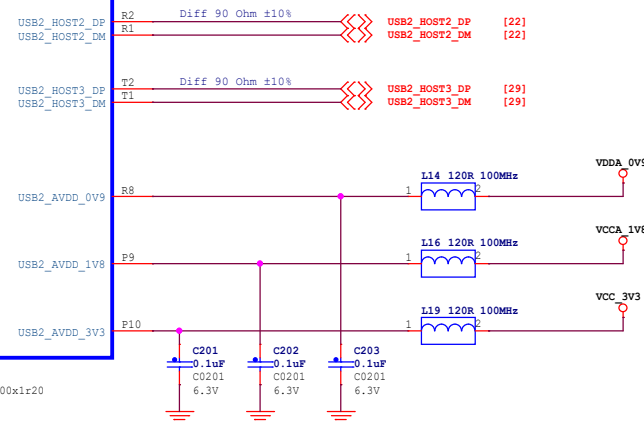
MULTI_PHY REFCLK



U110
RK3568
bga636_19r00x19r00x1r20

RK3568 USB2.0 HOST

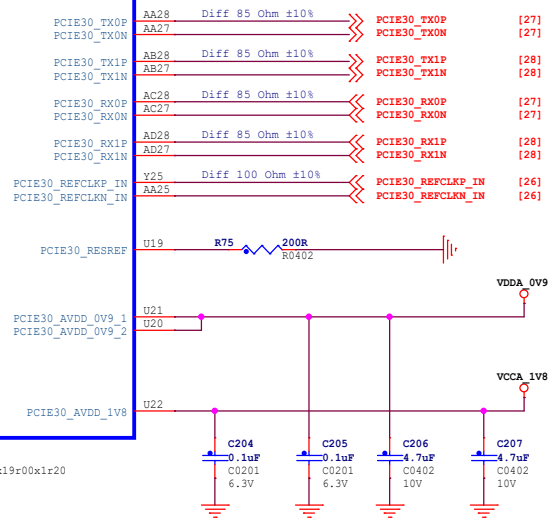
USB2.0 HOST



U11V
RK3568
bga636_19r00x19r00x1r20

RK3568 PCIe3.0 x2

PCIe3.0 x 2



U11W
RK3568
bga636_19r00x19r00x1r20

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Title
野火_RK3568 LubanCat 2 N_原理图_V1.3

Size
A3

Document Number
USB/PCIe/STAT_PHY

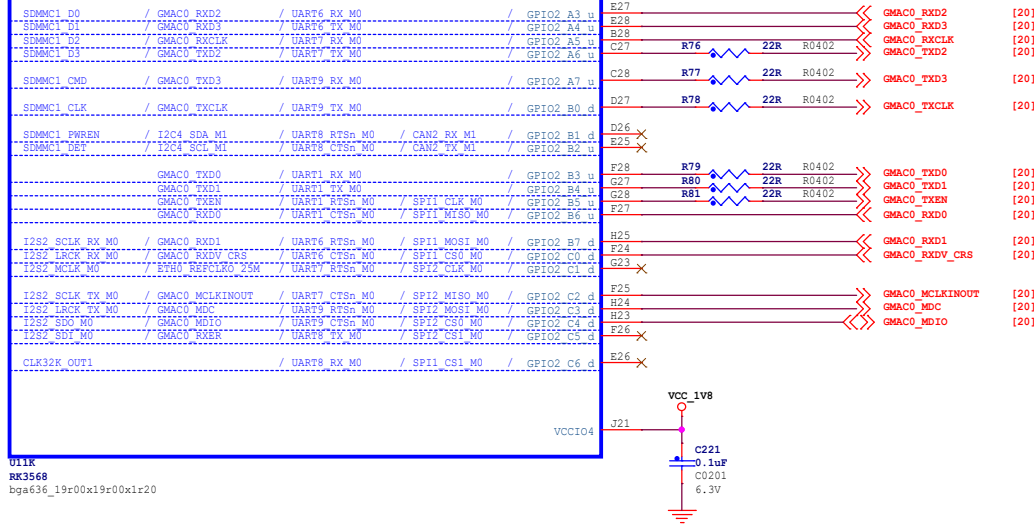
Rev
V1.3

Date: Wednesday, August 23, 2023 Sheet 13 of 29

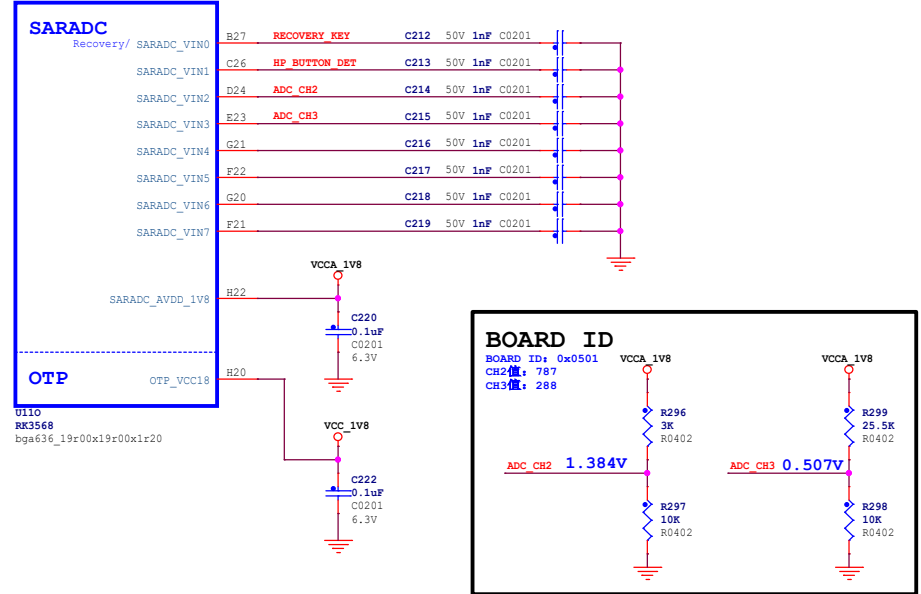
RK3568 VCCIO4 Domain

VCCIO4 Domain

Operating Voltage=1.8V/3.3V



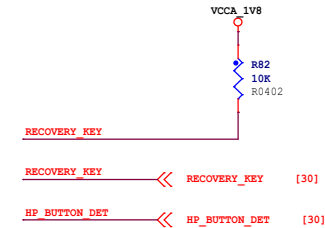
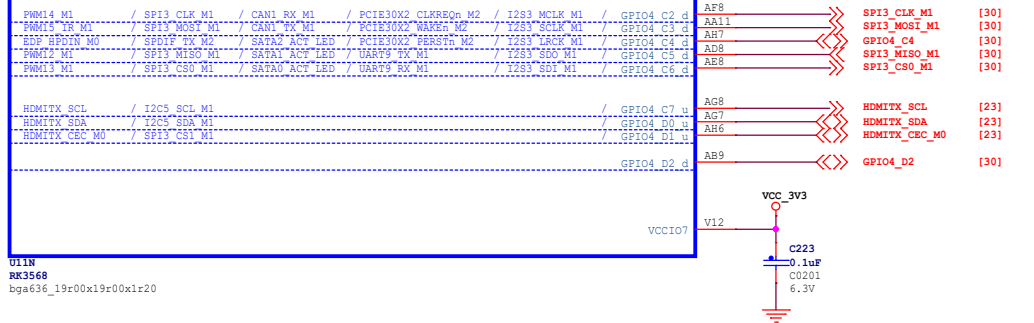
RK3568 SARADC/OTP



RK3568 VCCIO7 Domain

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

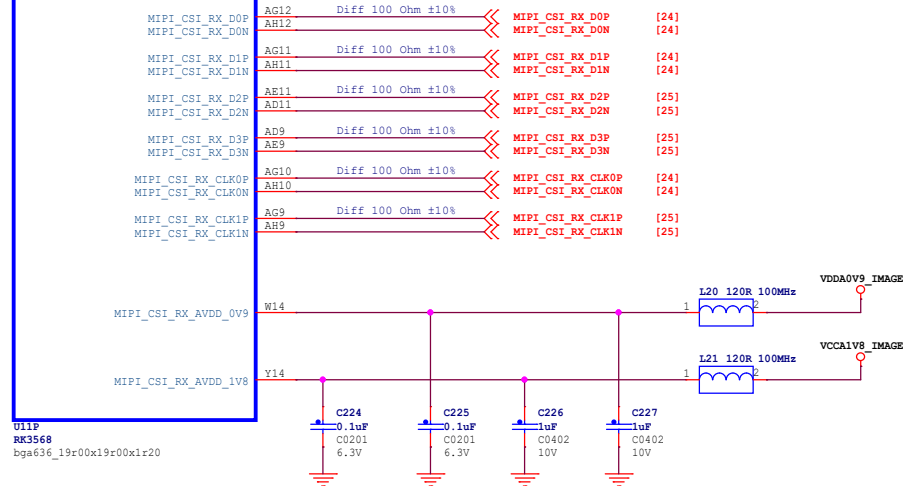


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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A3	Document Number SARADC/GPIO	Rev V1.3
Date: Wednesday, August 23, 2023 Sheet 14 of 29		

RK3568 MIPI_CSI_RX

MIPI CSI RX

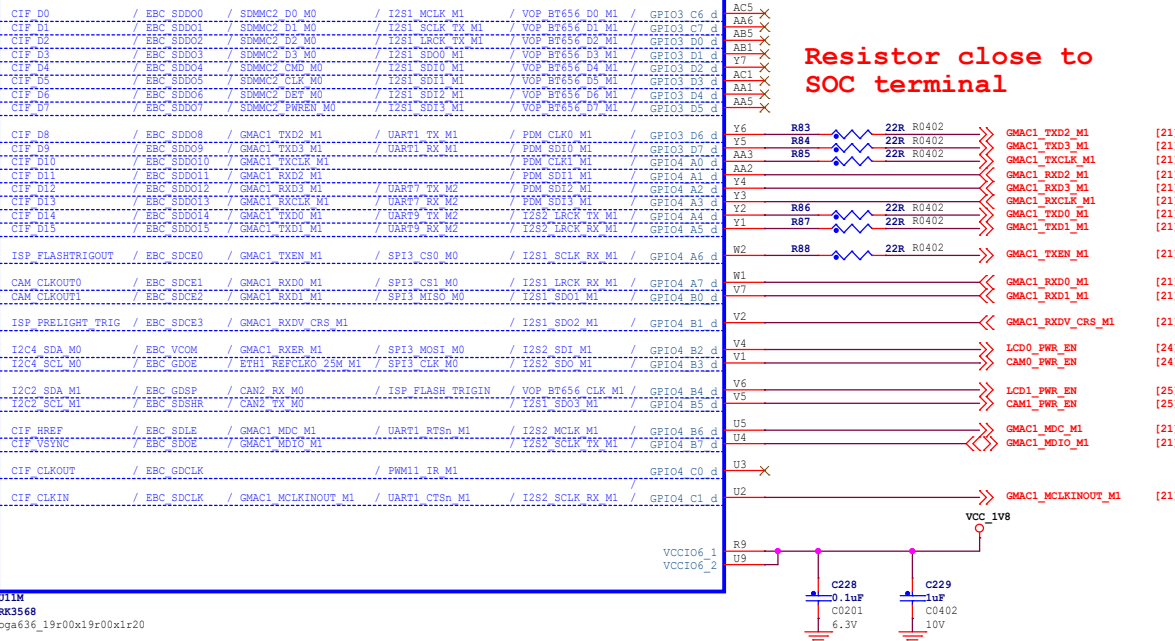


Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
	+ Sensor2 x2Lane	MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568 VCCIO6 Domain

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

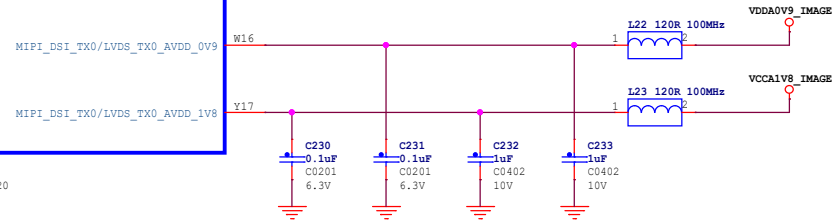


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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A3	Document Number VI Interface	Rev V1.3
Date: Wednesday, August 23, 2023 Sheet 15 of 29		

RK3568 MIPI_DSI_TX0/LVDS_TX0

MIPI DSI TX0/LVDS TX0

MIPI_DSI_TX0_D0P/LVDS_TX0_D0P AH17 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX0_D0P [24]
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N AG17 MIPI_DSI_TX0_D0N [24]
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P AH16 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX0_D1P [24]
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N AG16 MIPI_DSI_TX0_D1N [24]
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P AH14 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX0_D2P [24]
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N AG14 MIPI_DSI_TX0_D2N [24]
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P AH13 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX0_D3P [24]
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N AG13 MIPI_DSI_TX0_D3N [24]
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP AH15 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX0_CLKP [24]
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN AG15 MIPI_DSI_TX0_CLKN [24]

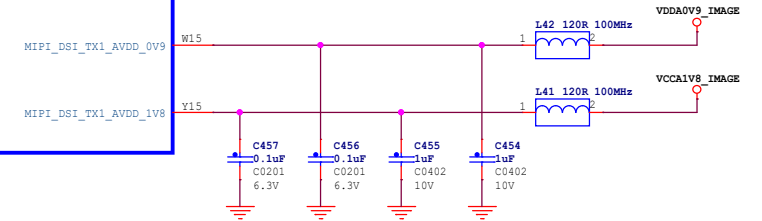


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RK3568 MIPI_DSI_TX1

MIPI DSI TX1

MIPI_DSI_TX1_D0P AH18 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX1_D0P [25]
MIPI_DSI_TX1_D0N AE18 MIPI_DSI_TX1_D0N [25]
MIPI_DSI_TX1_D1P AD17 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX1_D1P [25]
MIPI_DSI_TX1_D1N AC17 MIPI_DSI_TX1_D1N [25]
MIPI_DSI_TX1_D2P AD14 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX1_D2P [25]
MIPI_DSI_TX1_D2N AC14 MIPI_DSI_TX1_D2N [25]
MIPI_DSI_TX1_D3P AD12 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX1_D3P [25]
MIPI_DSI_TX1_D3N AE12 MIPI_DSI_TX1_D3N [25]
MIPI_DSI_TX1_CLKP AD15 Diff 100 Ohm $\pm 10\%$ MIPI_DSI_TX1_CLKP [25]
MIPI_DSI_TX1_CLKN AE15 MIPI_DSI_TX1_CLKN [25]

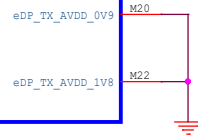


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RK3568 eDP TX

eDP_TX

eDP_TX_D0P J28
eDP_TX_D0N K27
eDP_TX_D1P K28
eDP_TX_D1N L27
eDP_TX_D2P L28
eDP_TX_D2N M27
eDP_TX_D3P M28
eDP_TX_D3N N27
eDP_TX_AUXP L25
eDP_TX_AUXN M25



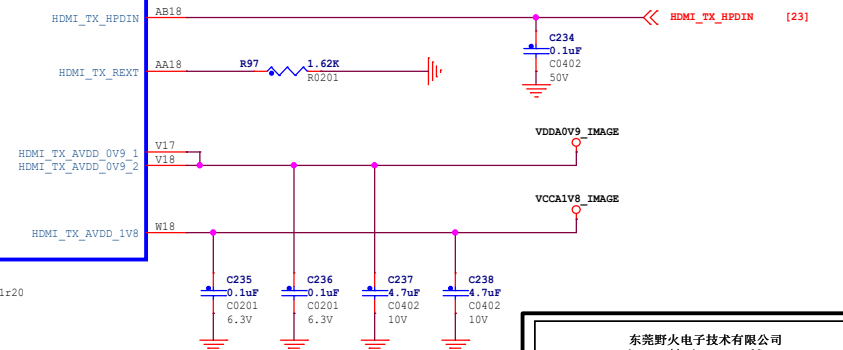
U11T
RK3568
bga636_19r00x19r00x1r20

RK3568 HDMI2.0 TX

Resistor close to SOC terminal

HDMI2.0 TX

HDMI_TX_D2P AG22 2.2R R0402 Diff 100 Ohm $\pm 10\%$ HDMI_TX_D2P [23]
HDMI_TX_D2N AH22 2.2R R0402 HDMI_TX_D2N [23]
HDMI_TX_D1P AG21 2.2R R0402 Diff 100 Ohm $\pm 10\%$ HDMI_TX_D1P [23]
HDMI_TX_D1N AH21 2.2R R0402 HDMI_TX_D1N [23]
HDMI_TX_D0P AG20 2.2R R0402 Diff 100 Ohm $\pm 10\%$ HDMI_TX_D0P [23]
HDMI_TX_D0N AH20 2.2R R0402 HDMI_TX_D0N [23]
HDMI_TX_CLKP AH19 2.2R R0402 Diff 100 Ohm $\pm 10\%$ HDMI_TX_CLKP [23]
HDMI_TX_CLKN AG19 2.2R R0402 HDMI_TX_CLKN [23]

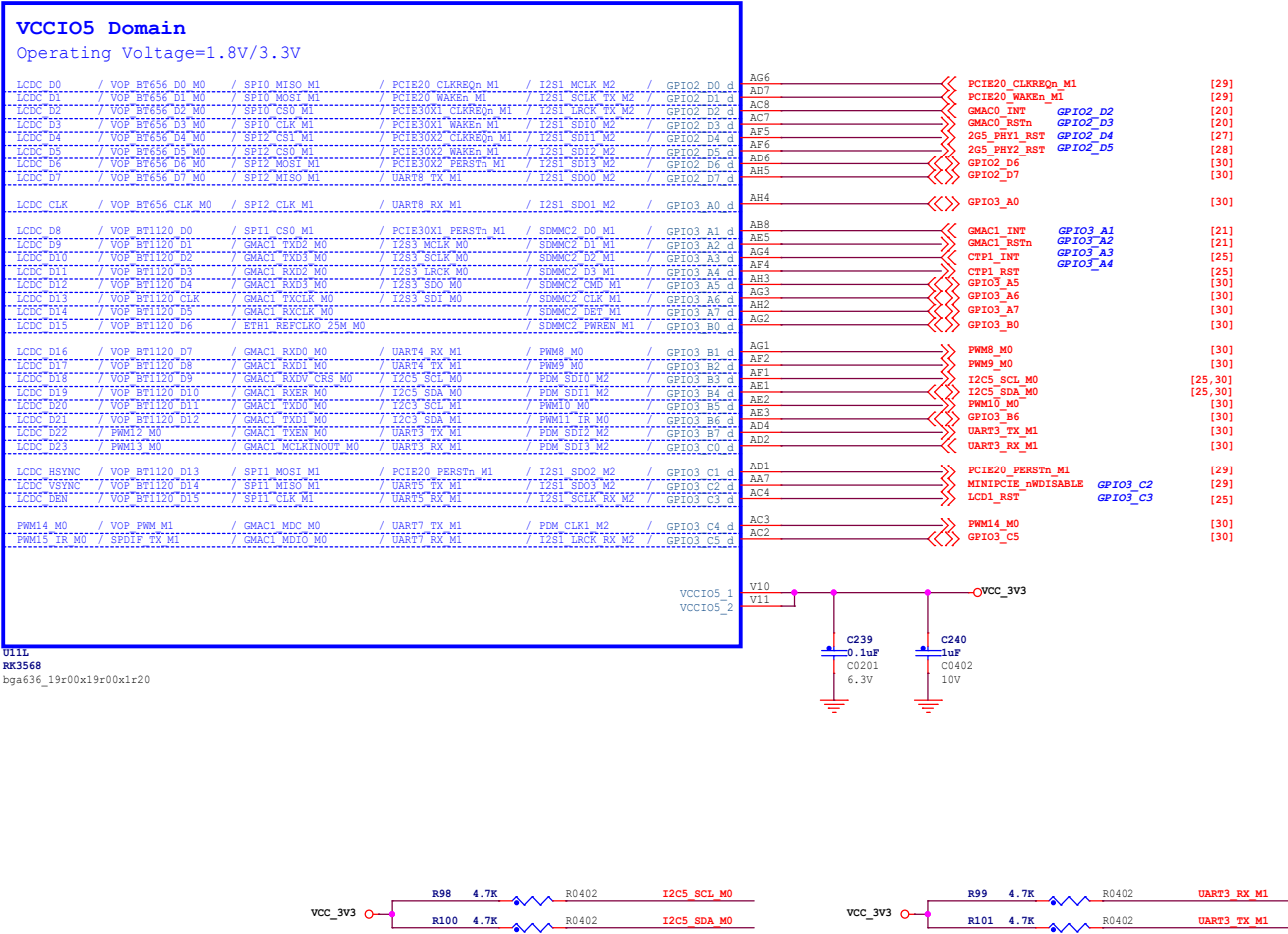


U11Q
RK3568
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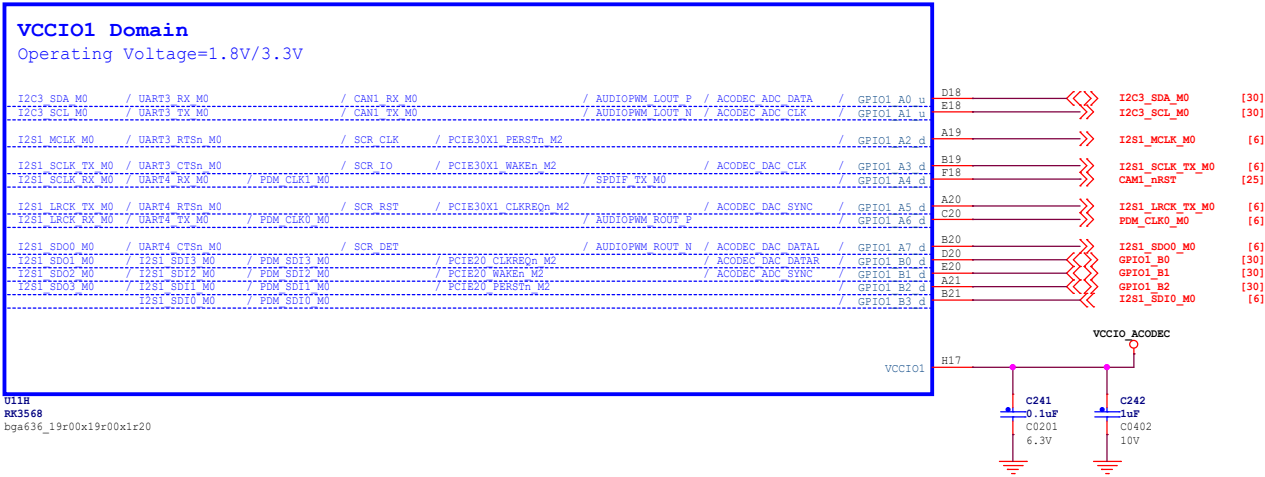
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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A3	Document Number VO Interface_1	Rev V1.3
Date: Wednesday, August 23, 2023 Sheet 16 of 29		

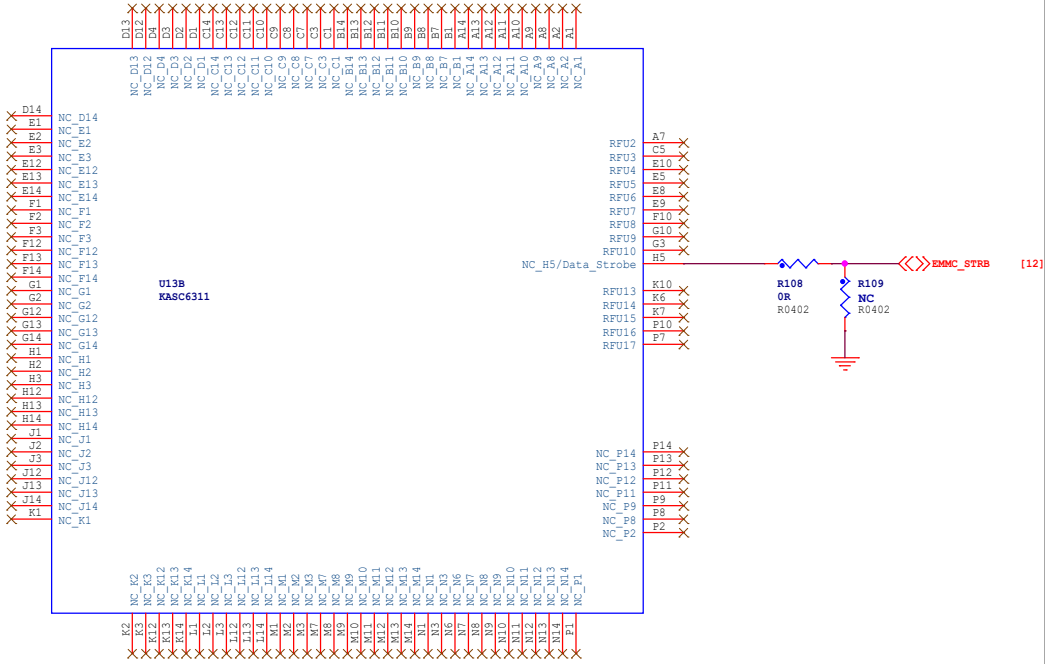
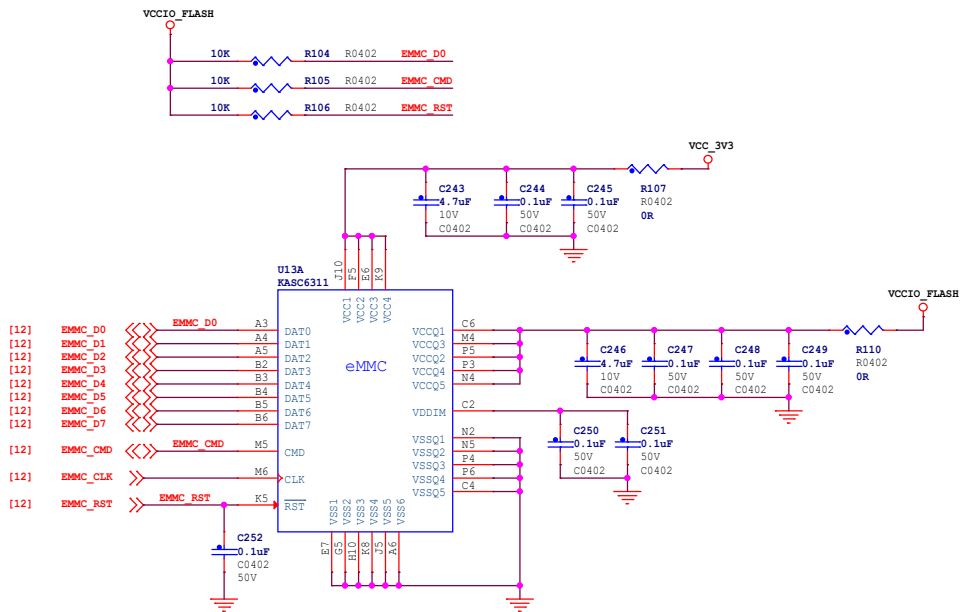
RK3568 VCCIO5 Domain



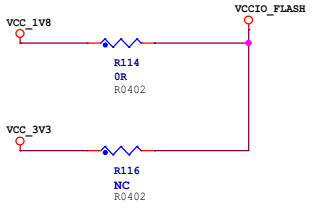
RK3568 VCCIO1 Domain



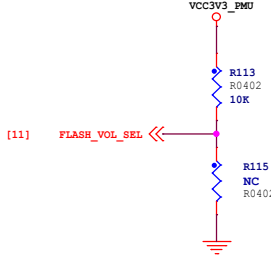
EMMC FLASH



EMMC_IO_Toggle



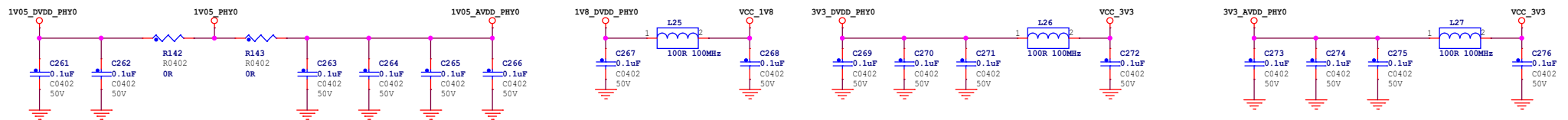
FLASH_VOL_SEL



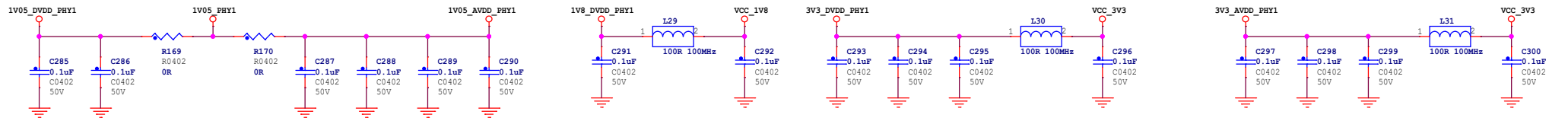
Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

野火_RK3568 Iubancat 2 N_原理图_V1.3		
Size	Document Number	Rev
A3	EMMC_FLASH	V1.3
Date:	Wednesday, August 23, 2023	Sheet 19 of 29

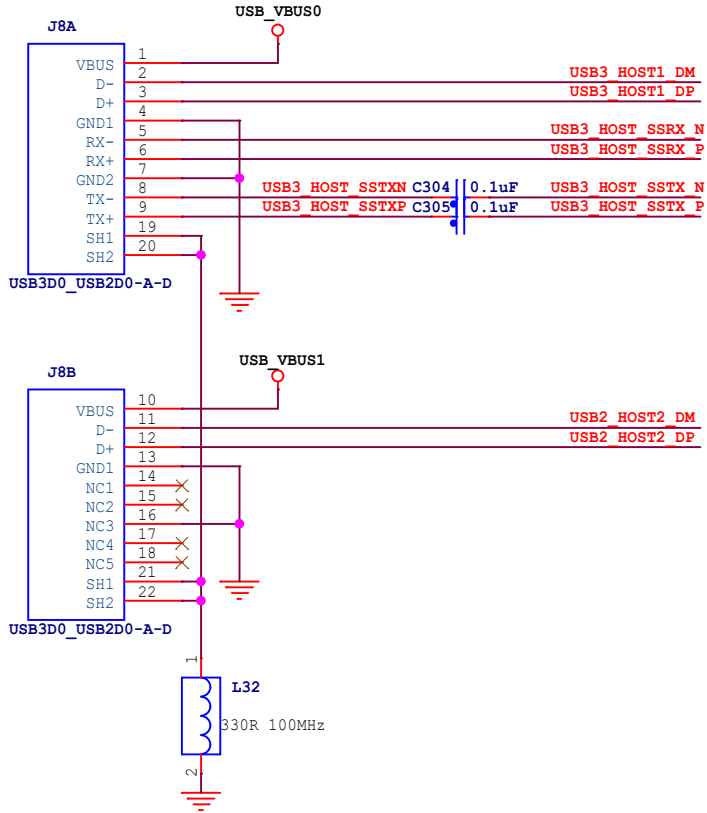
PHY Address : 001



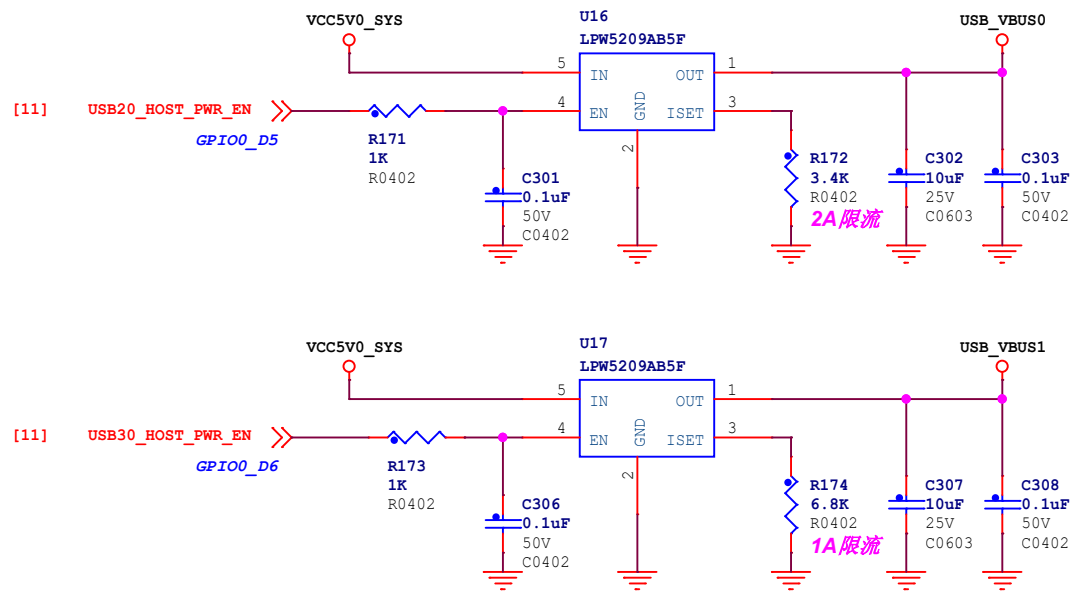
PHY Address : 010



USB 3.0 HOST x1
USB 2.0 HOST x1

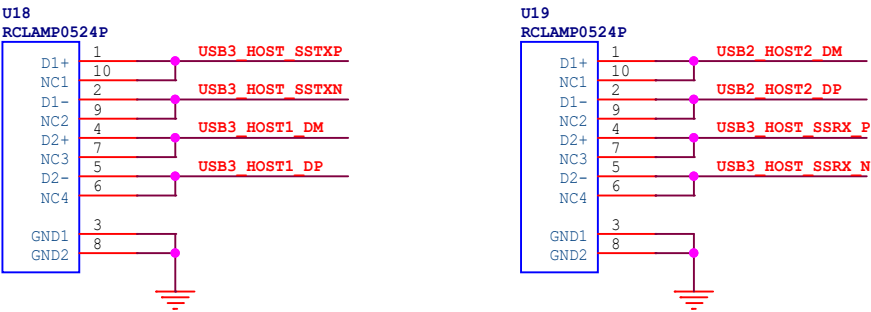


USB POWER



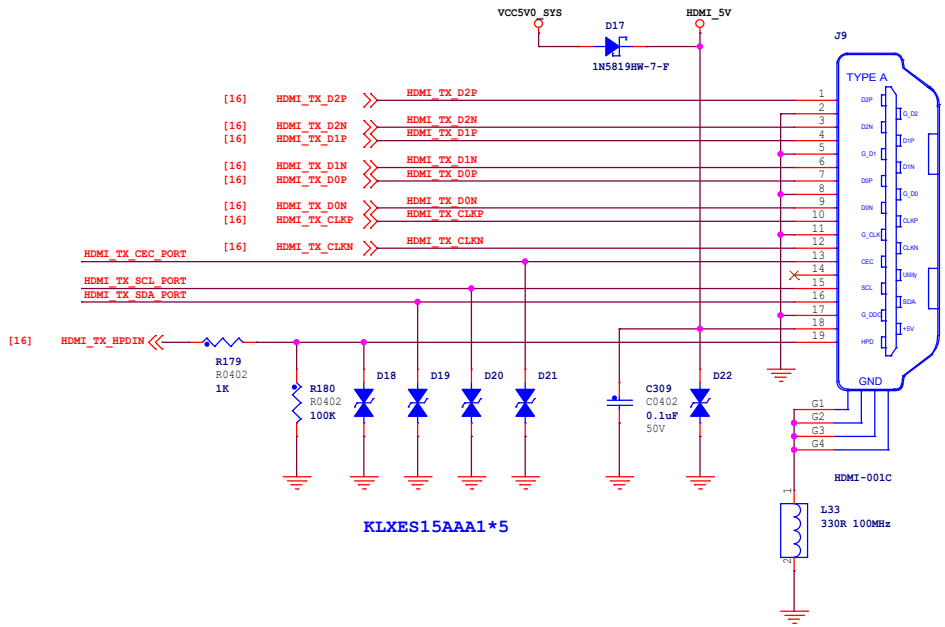
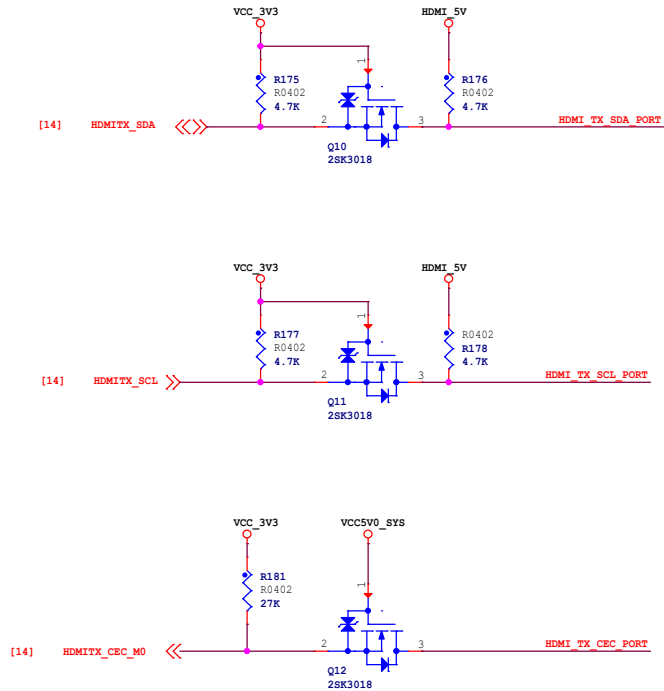
USB3_HOST1_DM	>>	USB3_HOST1_DM	[13]
USB3_HOST1_DP	>>	USB3_HOST1_DP	[13]
USB2_HOST2_DM	>>	USB2_HOST2_DM	[13]
USB2_HOST2_DP	>>	USB2_HOST2_DP	[13]
USB3_HOST_SSRX_N	>>	USB3_HOST_SSRX_N	[13]
USB3_HOST_SSRX_P	>>	USB3_HOST_SSRX_P	[13]
USB3_HOST_SSTX_N	>>	USB3_HOST_SSTX_N	[13]
USB3_HOST_SSTX_P	>>	USB3_HOST_SSTX_P	[13]

ESD

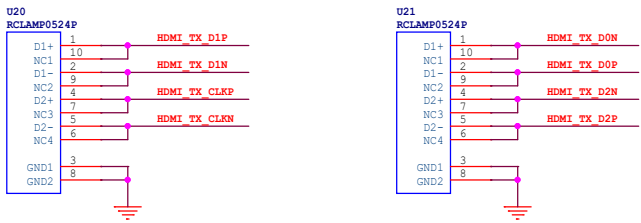


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Title 野火_RK3568 LubanCat 2 N_原理图_v1.3		
Size A4	Document Number USB_PORT	Rev V1.3
Date: Wednesday, August 23, 2023 Sheet 22 of 29		

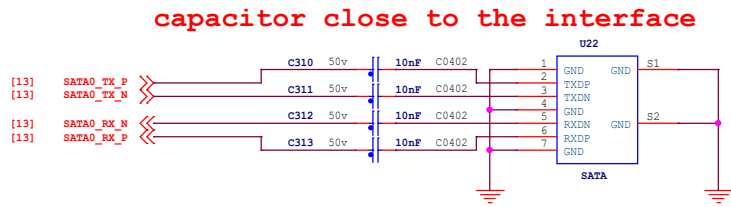
HDMI_PORT



HDMI_ESD

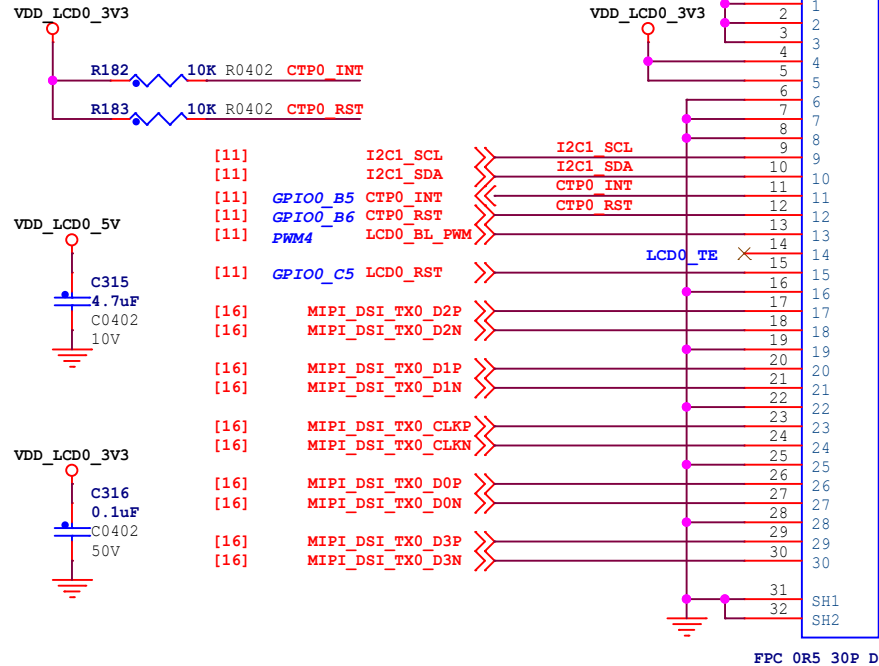


SATA_PORT

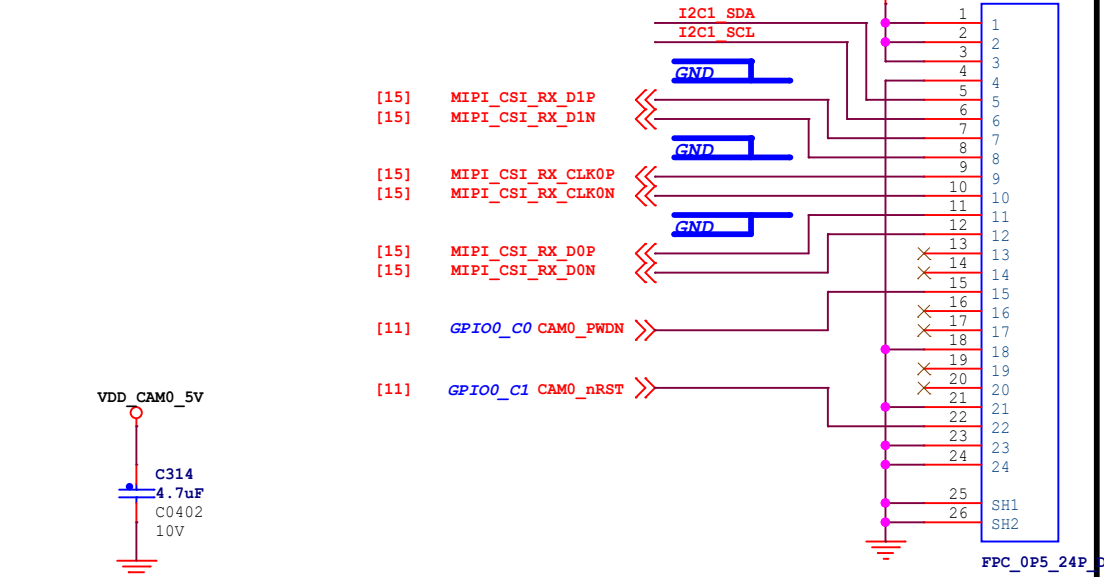


Title		
野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size	Document Number	Rev
A3	HDMI_PORT/SATA_PORT	V1.3
Date:	Wednesday, August 23, 2023	Sheet 23 of 29

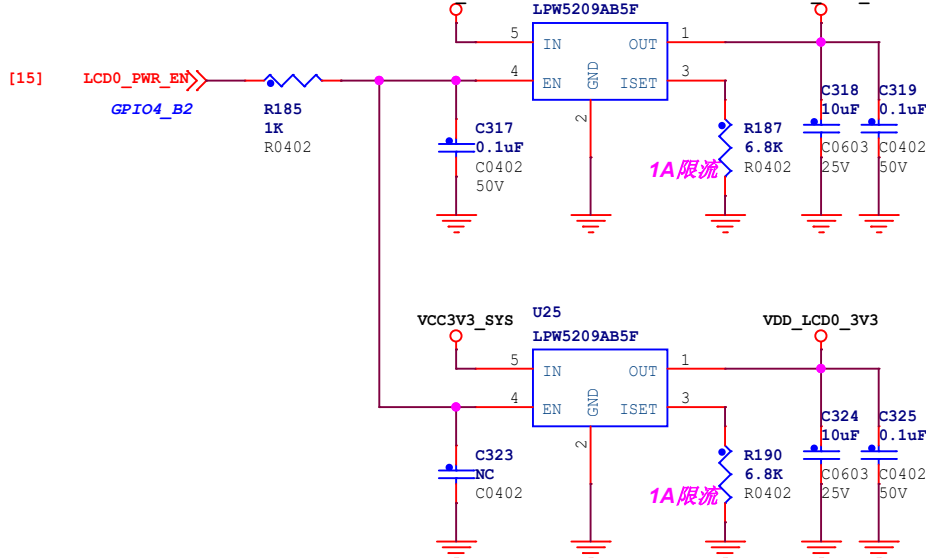
MIPI DSI LCD PORT 0



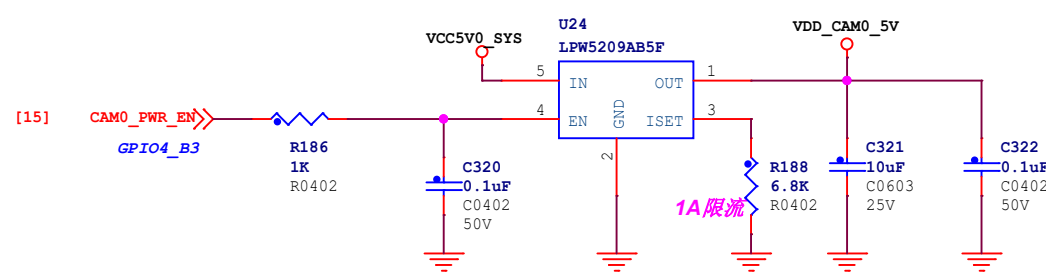
MIPI CSI PORT 0



LCD Power



MIPI CSI Power



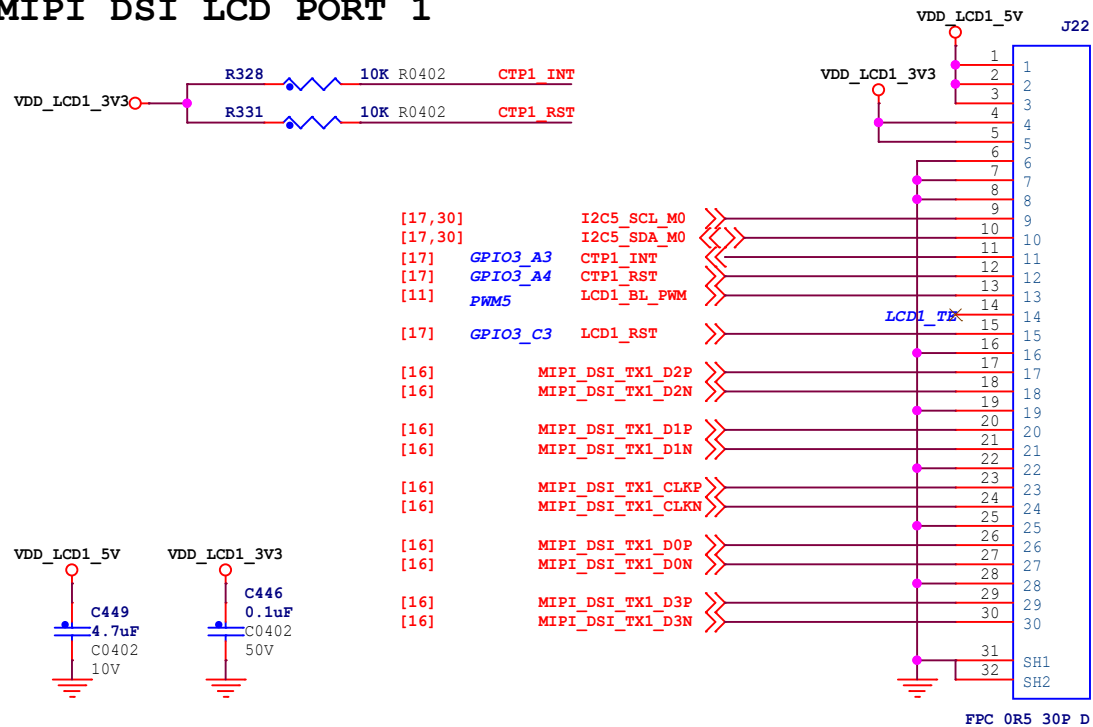
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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3

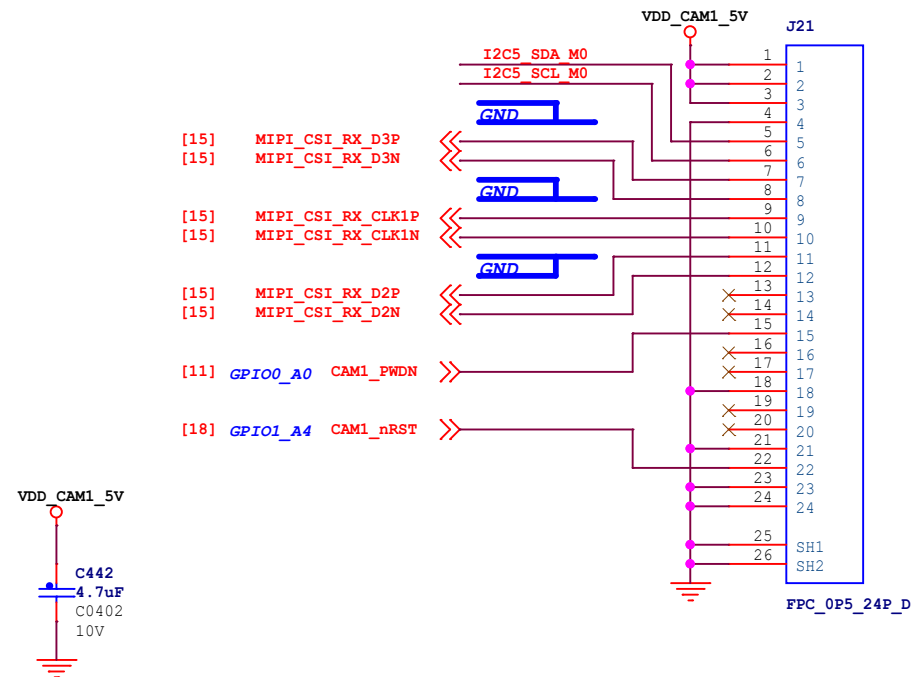
Size	Document Number	Rev
A4	MIPI DSI/MIPI CSI_PORT	V1.3

Date: Wednesday, August 23, 2023 Sheet 24 of 29

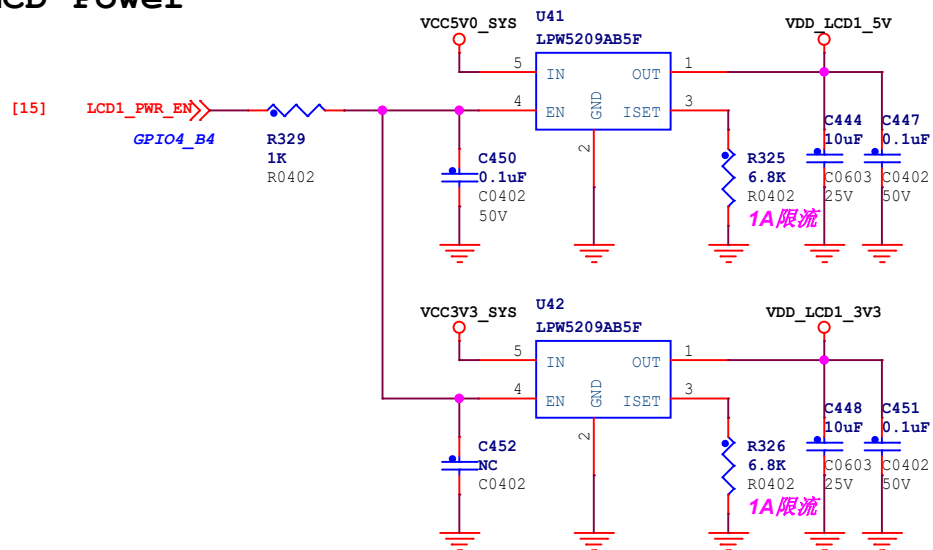
MIPI DSI LCD PORT 1



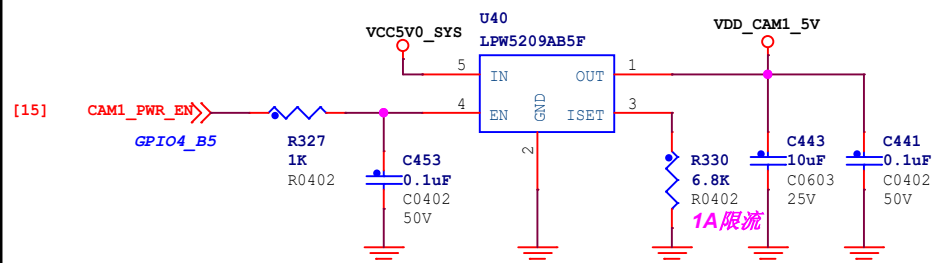
MIPI CSI PORT 1



LCD Power



MIPI CSI Power



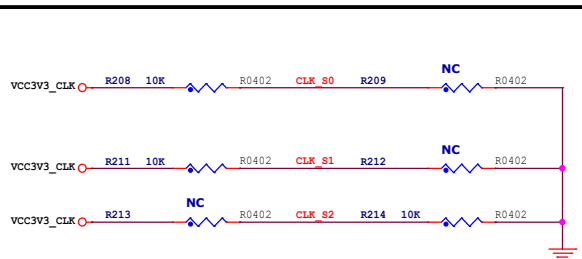
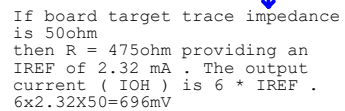
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Title: 野火_RK3568 LubanCat 2 N_原理图_v1.3

Size: A4 Document Number: MIPI DSI/MIPI CSI_PORT Rev: V1.3

Date: Wednesday, August 23, 2023 Sheet 25 of 30

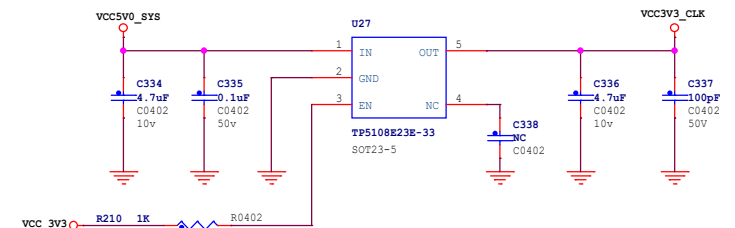
CLK*3 @100MHz



Default: No Spread

CLK_S0	CLK_S1	CLK_S2	Spread %	Out Freq
0	0	0	-0.5	100MHz
1	0	0	-1.0	100MHz
0	1	0	-1.5	100MHz
1	1	0	No Spread	100MHz

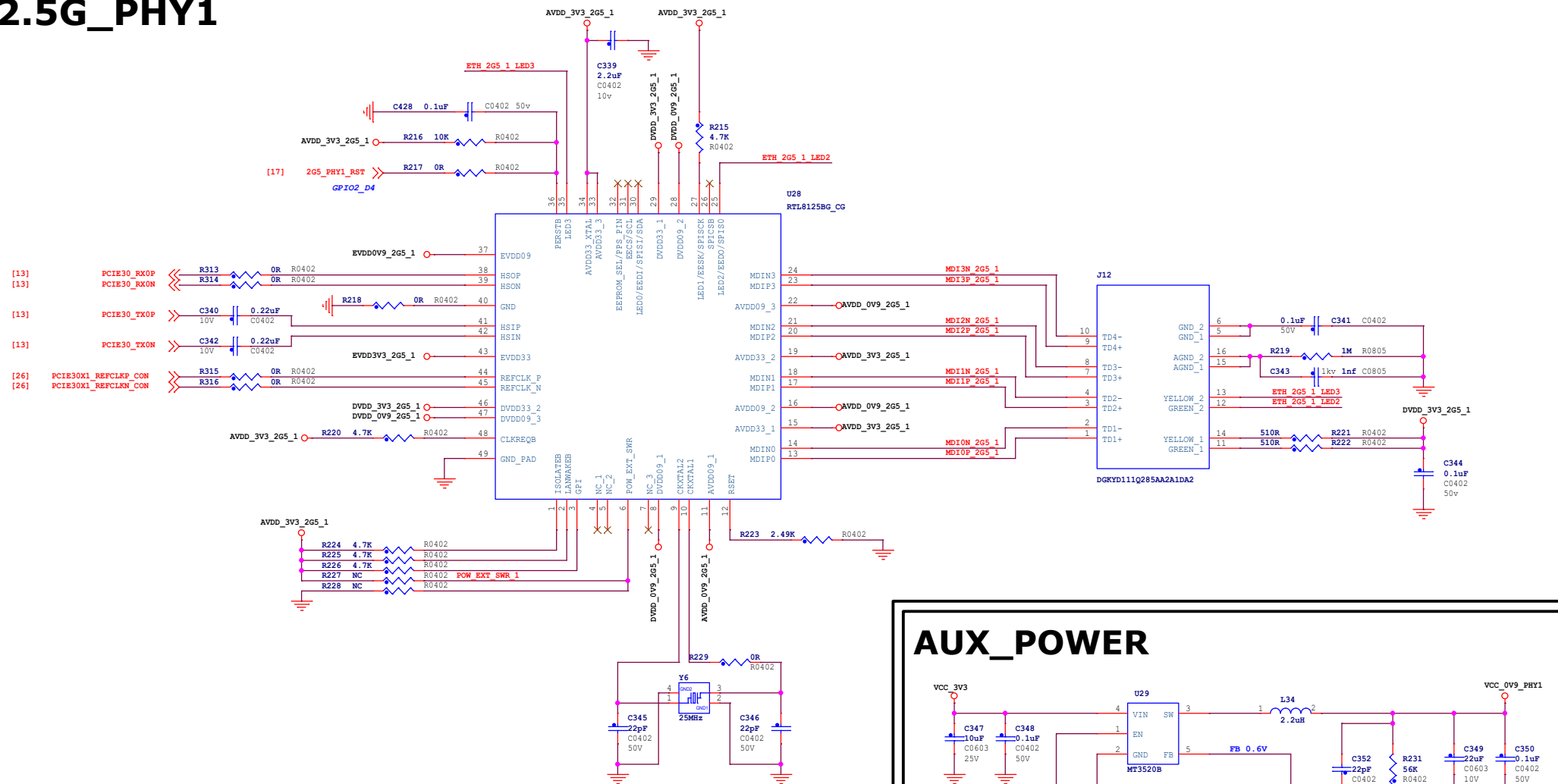
SPLIT_CLK_POWER



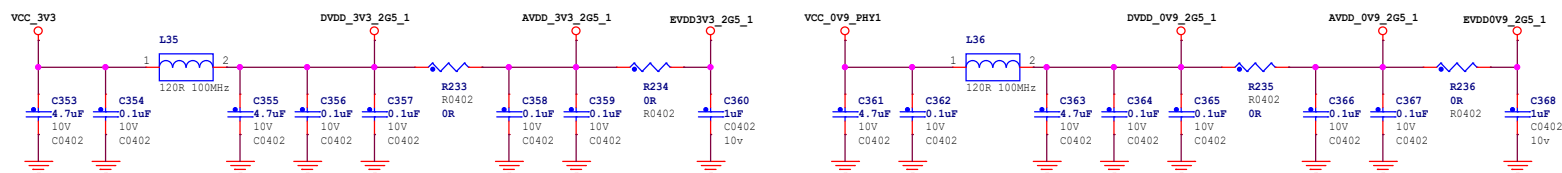
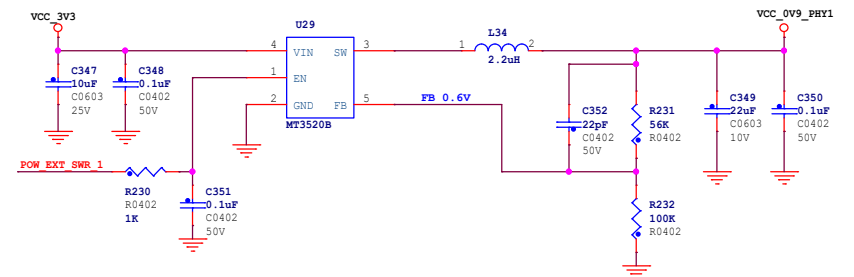
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Title		
野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size	Document Number	Rev
A3	PCIE3.0_REFCLK	V1.3
Date:	Wednesday, August 23, 2023	Sheet 26 of 30

2.5G_PHY1



AUX_POWER

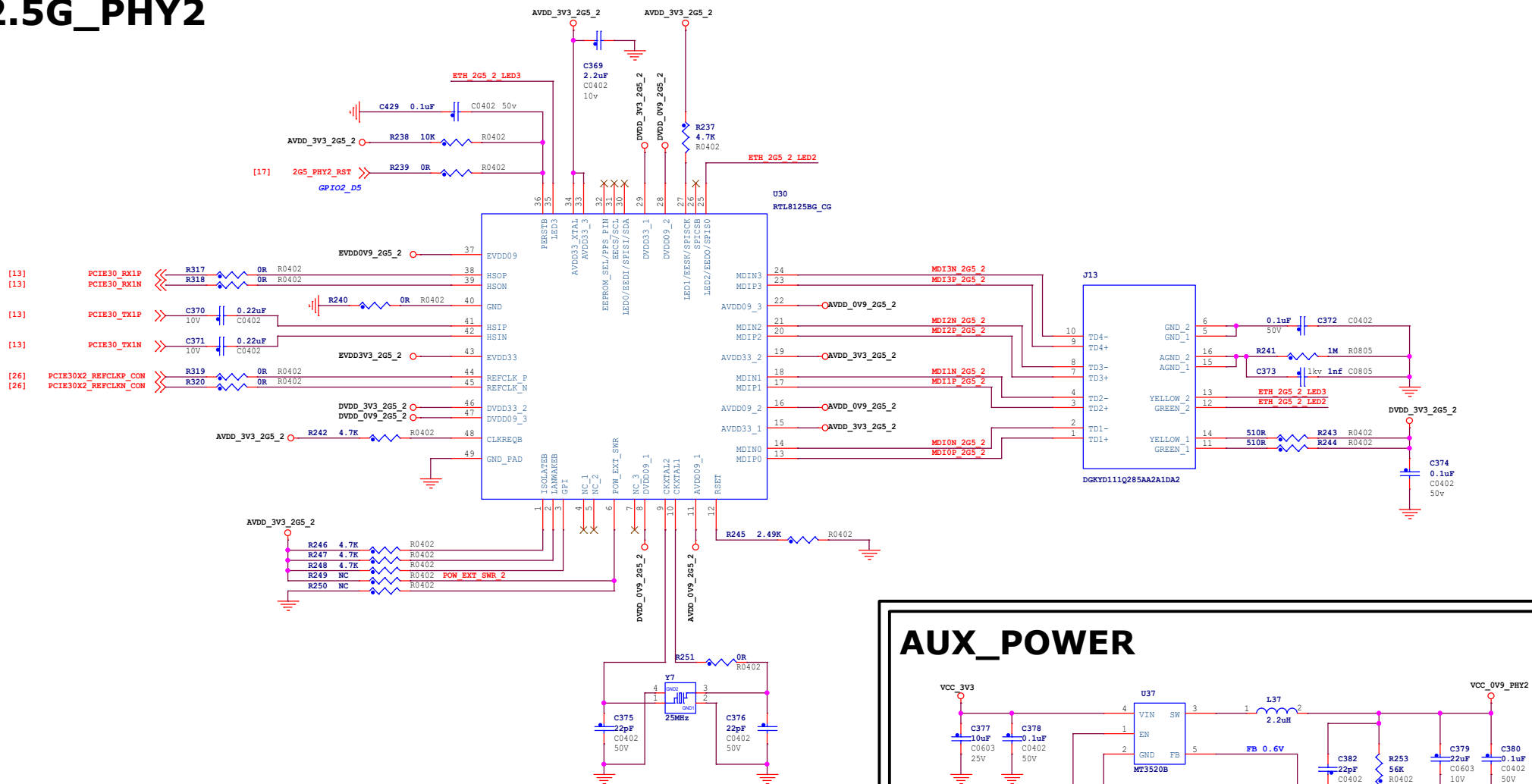


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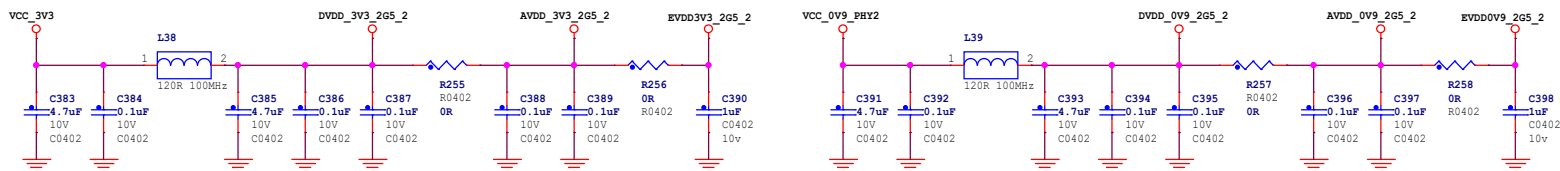
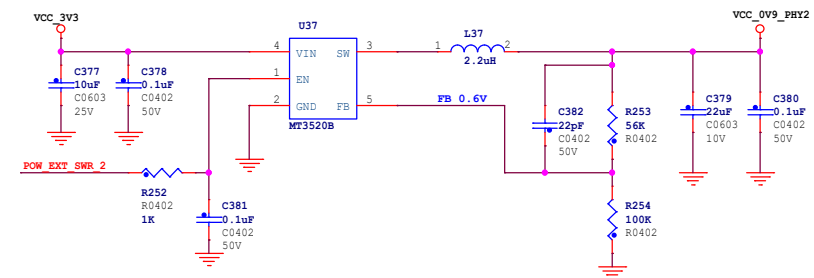
Title 野火_RK3568 LubanCat 2 N_原理图_V1.3

Size A3	Document Number 2.5G_PHY1	Rev V1.3
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2.5G_PHY2



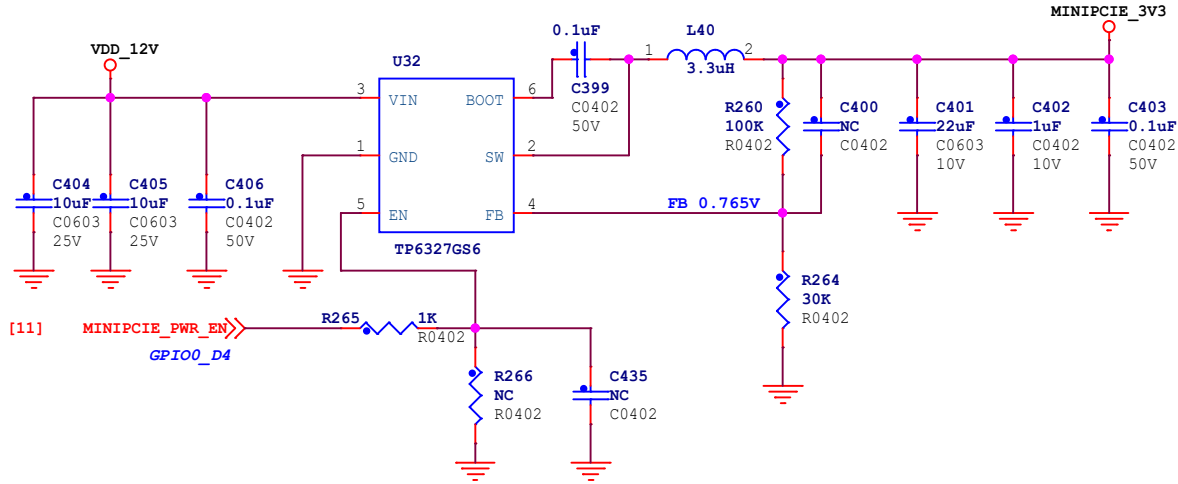
AUX_POWER



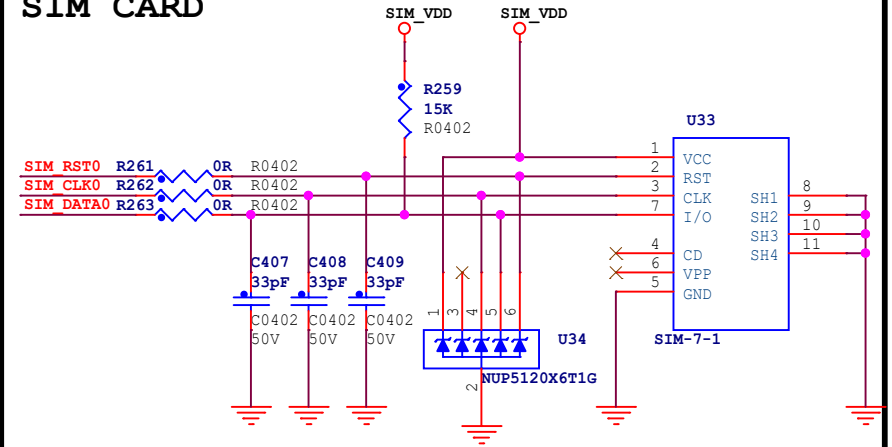
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Title		
野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A3	Document Number 2.5G_PHY2	Rev V1.3
Date: Wednesday, August 23, 2023	Sheet 28 of 30	

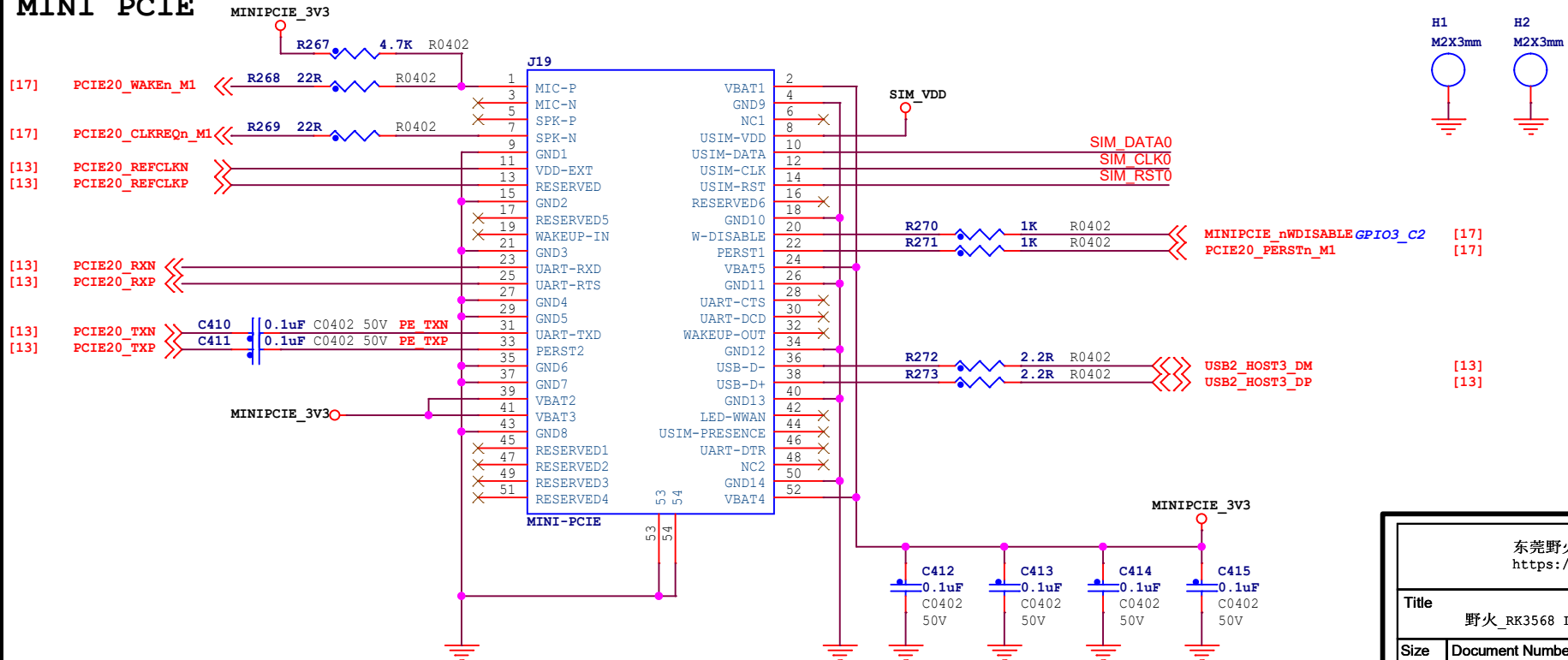
MINI PCIE POWER



SIM CARD



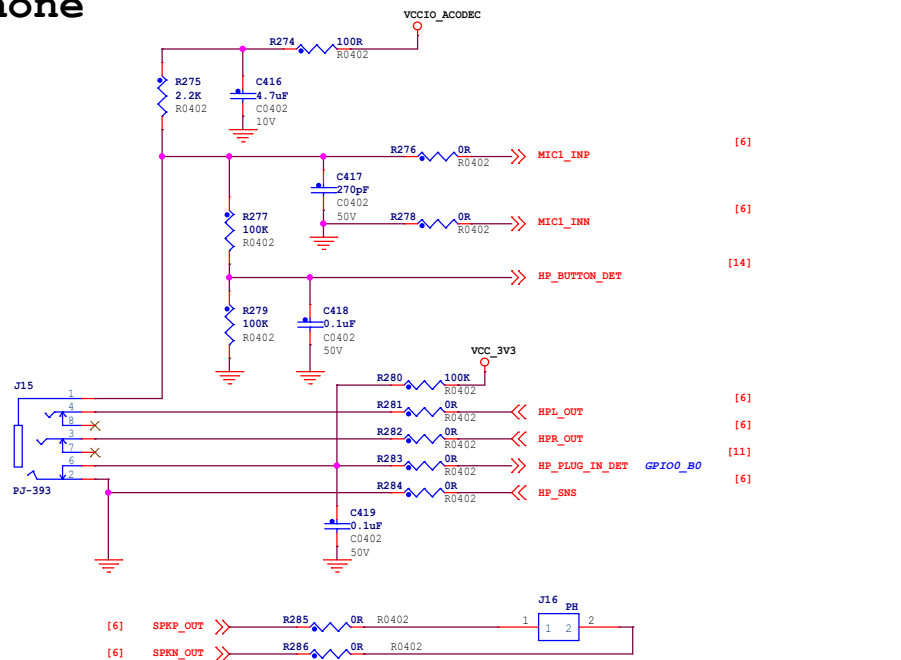
MINI PCIE



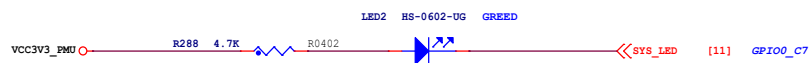
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Title 野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A4	Document Number MINI PCIE_PORT	Rev V1.3
Date: Friday, September 08, 2023 Sheet 29 of 30		

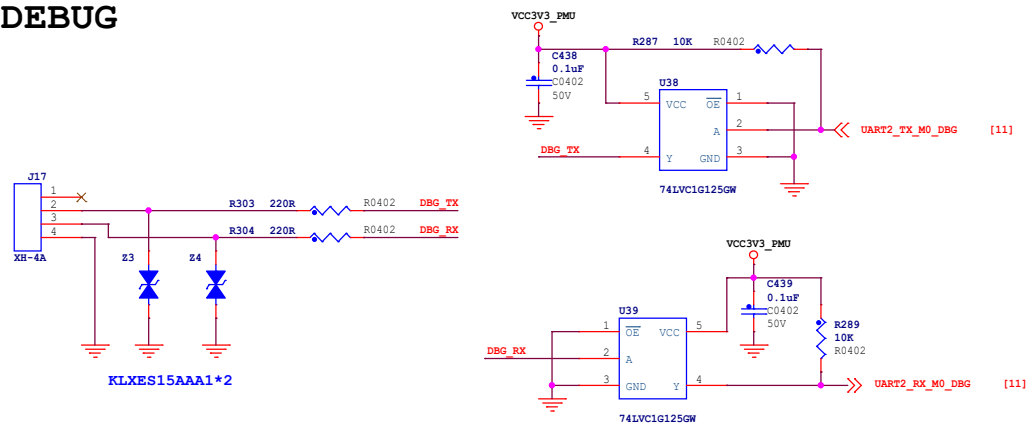
Earphone



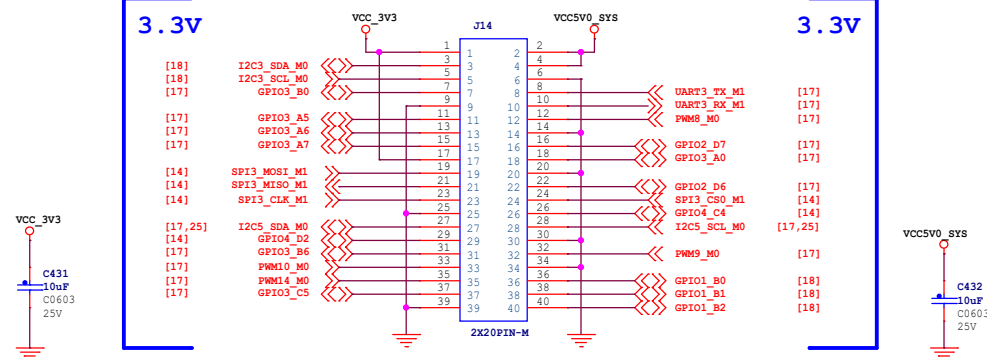
LED



DEBUG

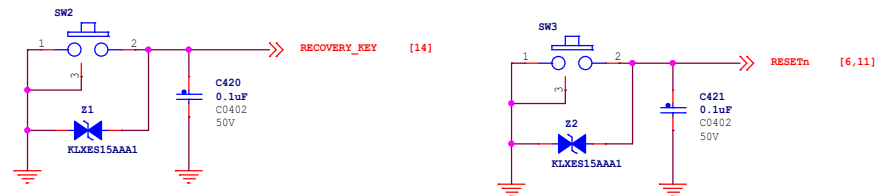


IO PORT

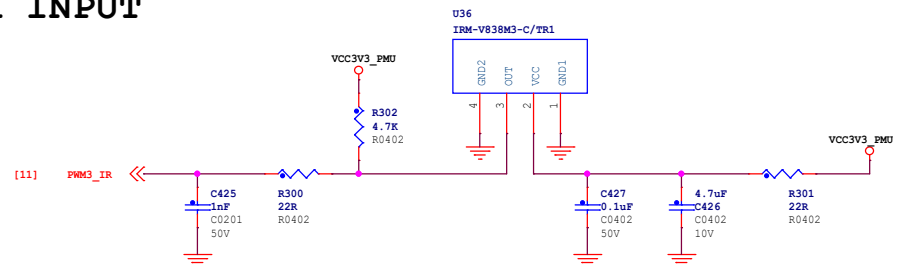


RECOVERY KEY

RESET KEY



IR INPUT



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Title		
野火_RK3568 LubanCat 2 N_原理图_V1.3		
Size A3	Document Number Earphone/DEBUG/IO_PORT/LED	Rev V1.3
Date: Wednesday, August 23, 2023	Sheet 30	of 30