

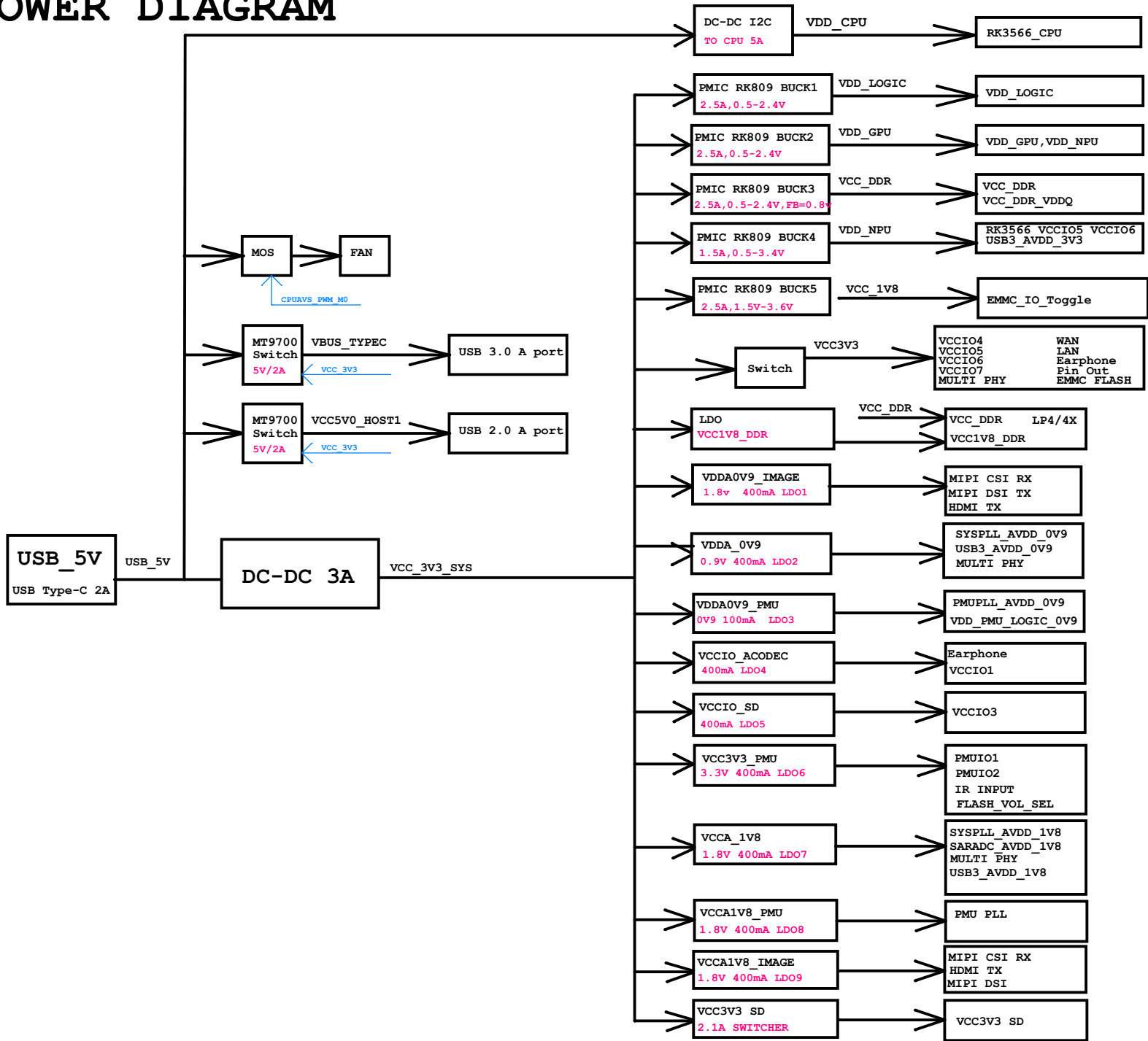
野火_RK3566 LubanCat 1 N 原理图_v0.2

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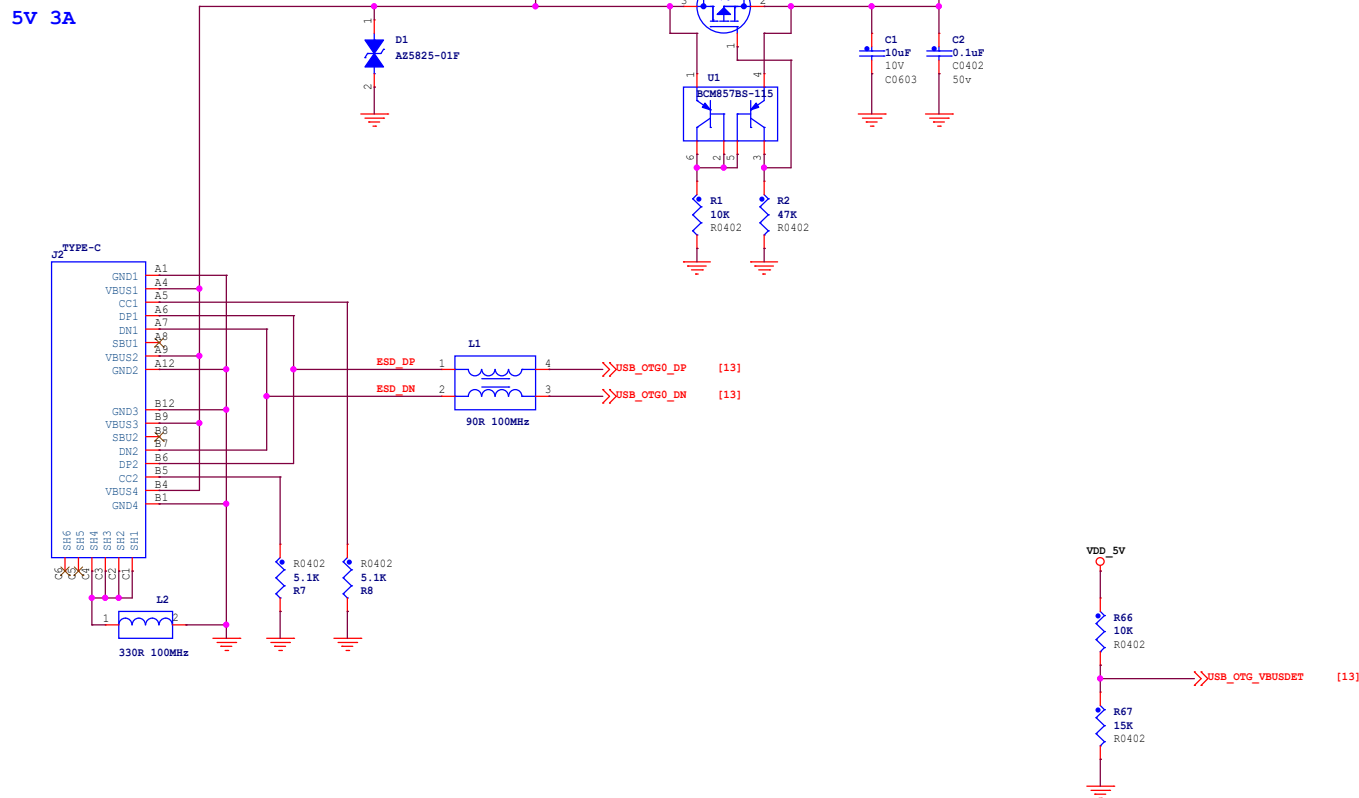
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历史版本			
版本号	日期	设计	描述
V0.1	2022-03-18	ghs	初始版本
V0.2	2022-06-24	ghs	修正版本，修正GMAC网口的电压域，同时更换WIFI网卡模块，优化主供电滤波

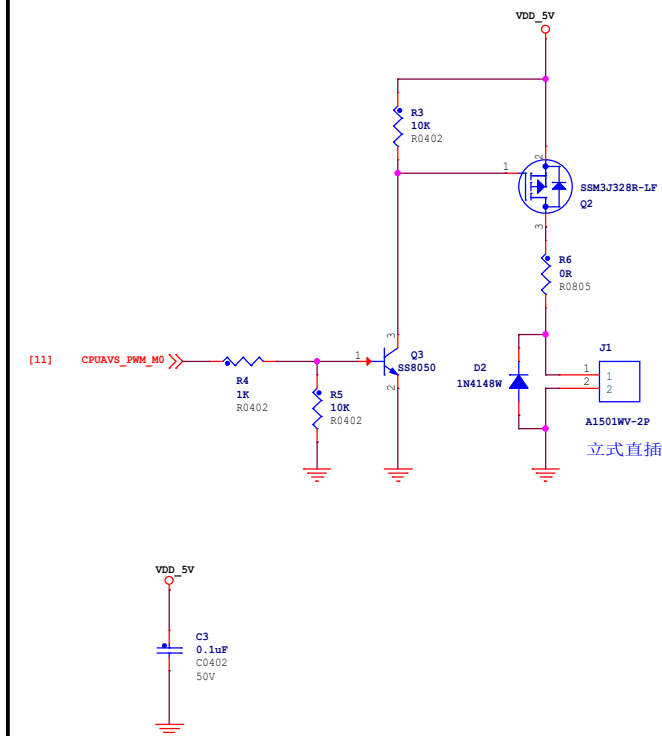
POWER DIAGRAM



POWER IN

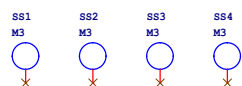


Active Cooling

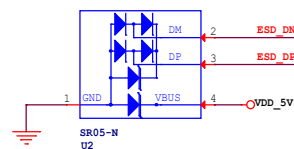


机械定位孔

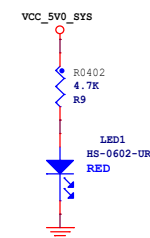
4*M3



USB ESD



PWR_LED



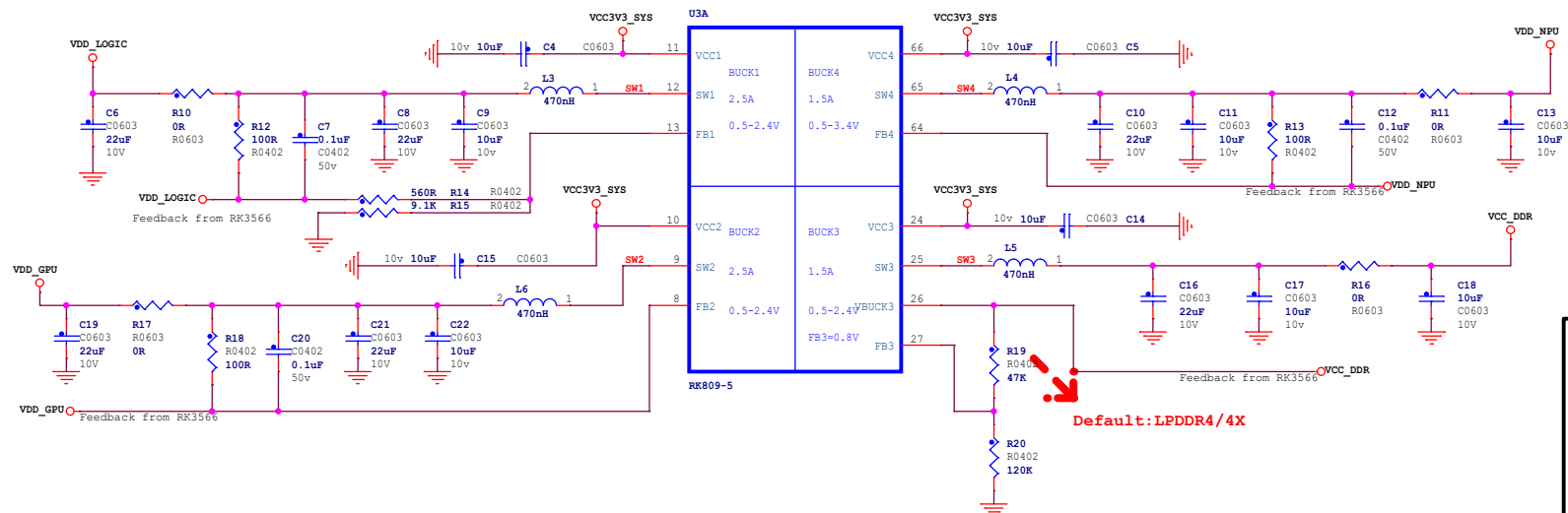
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Title 野火_RK3566 LubanCat 1 N_原理图

Size A3 Document Number TYPE_C_IN Rev V0.2

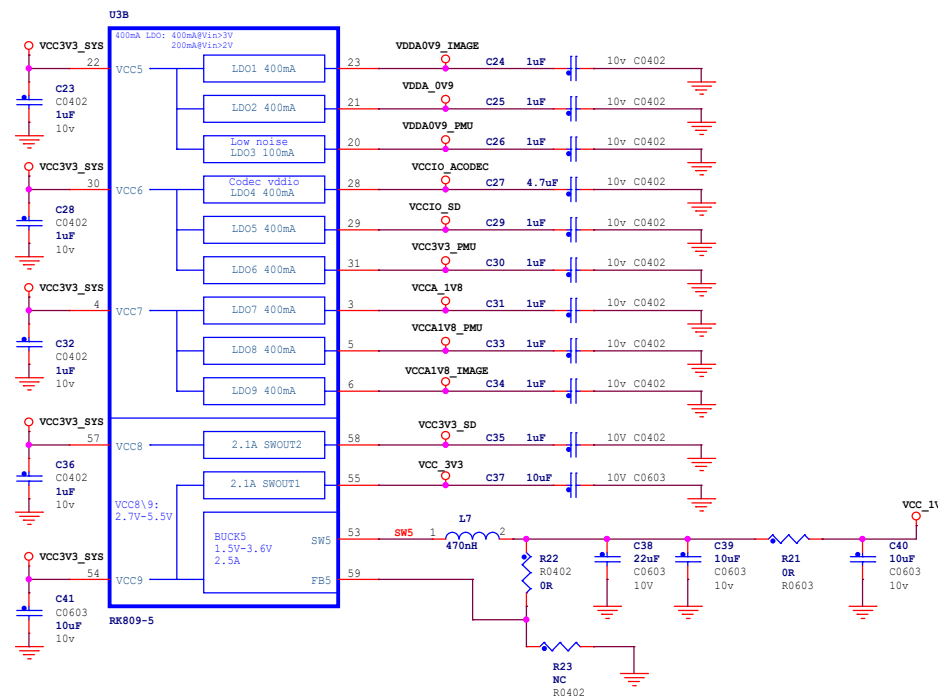
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PMIC RK809 DCDC



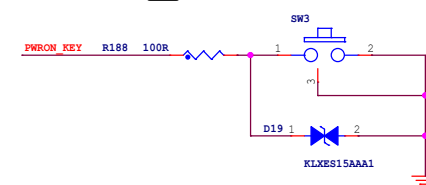
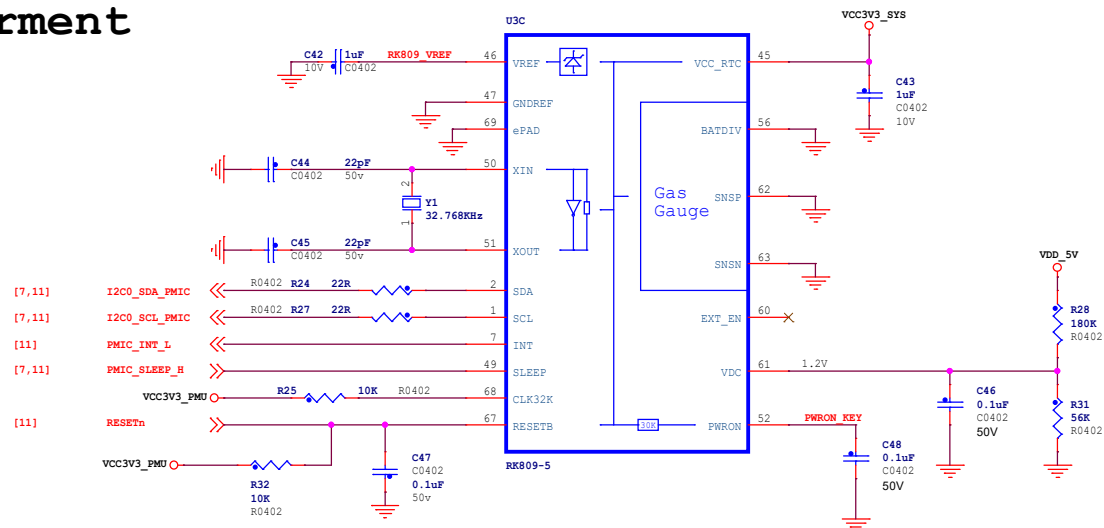
RK3566 BUCK FB

PMIC RK809 LDO

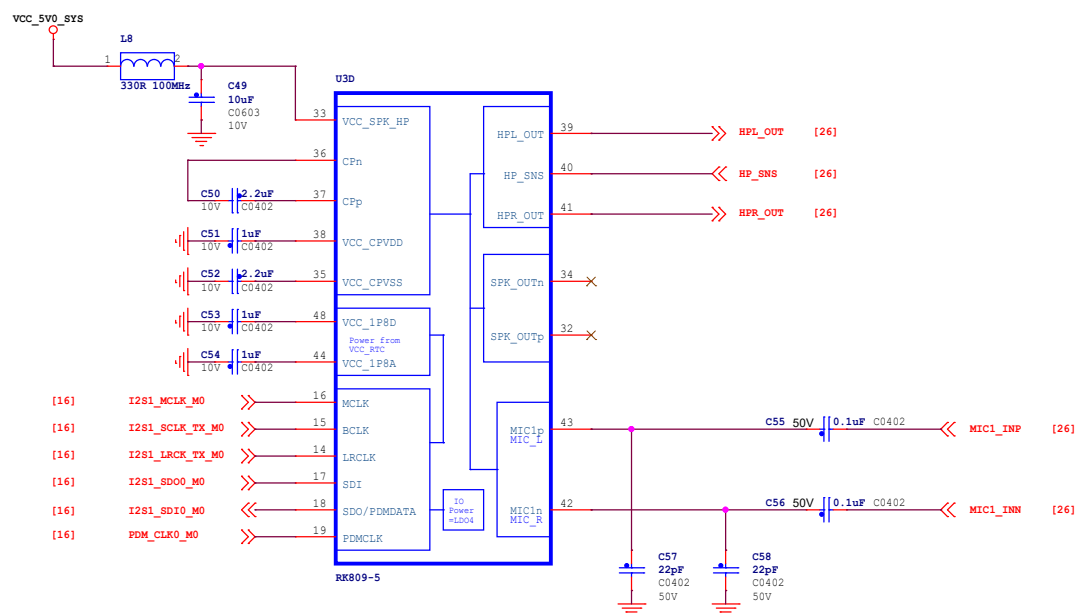


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Title	野火_RK3566 LubanCat 1 N_原理图	
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PMIC RK809 Managerment



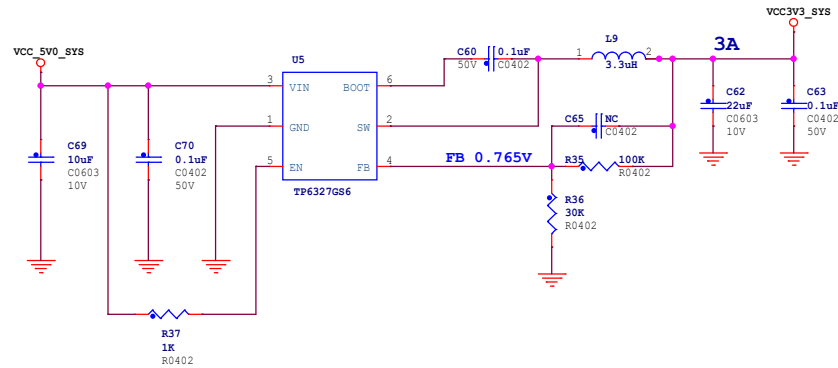
PMIC RK809 CODEC



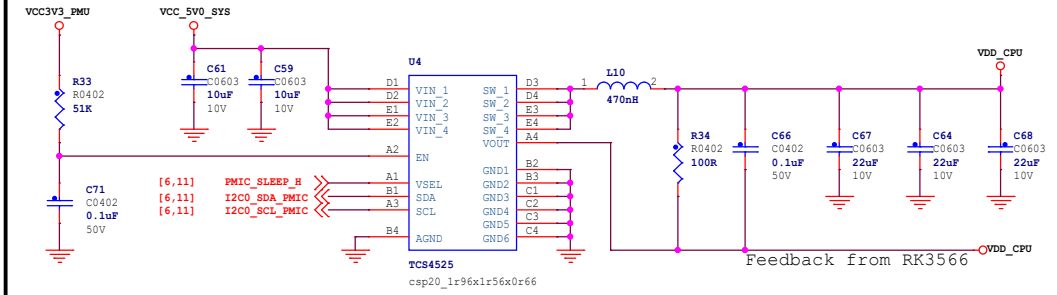
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A3	PMIC_Managerment/CODE	V0.
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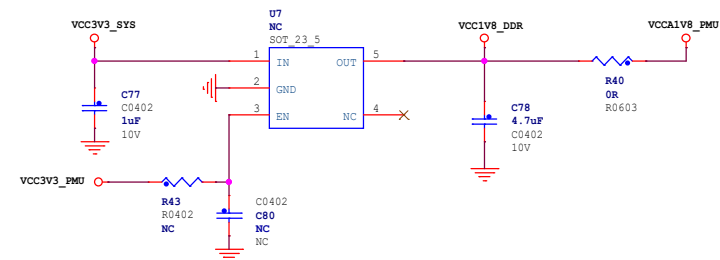
SYS_Power



RK3566 CPU Power VDD_CPU_EXT

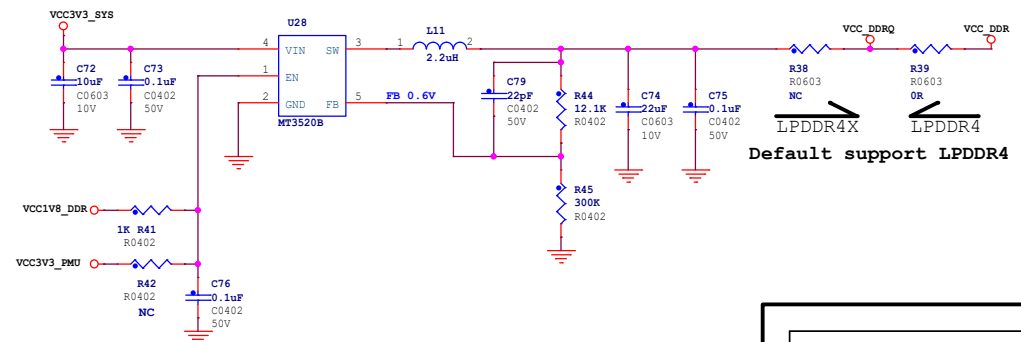


Auxiliary power supply LPDDR4_VCC1V8_DDR



LPDDR4X Power

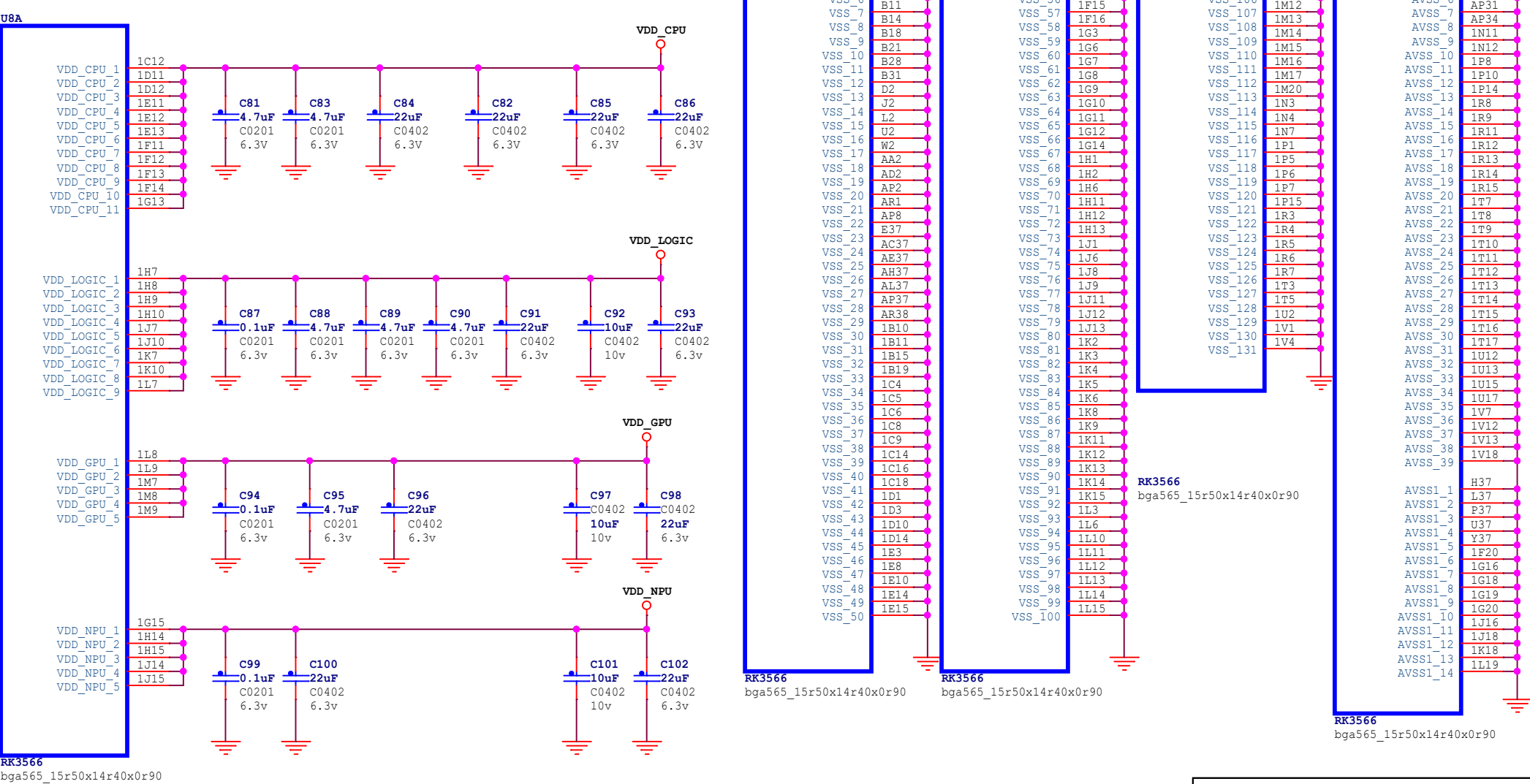
output: 0.6V



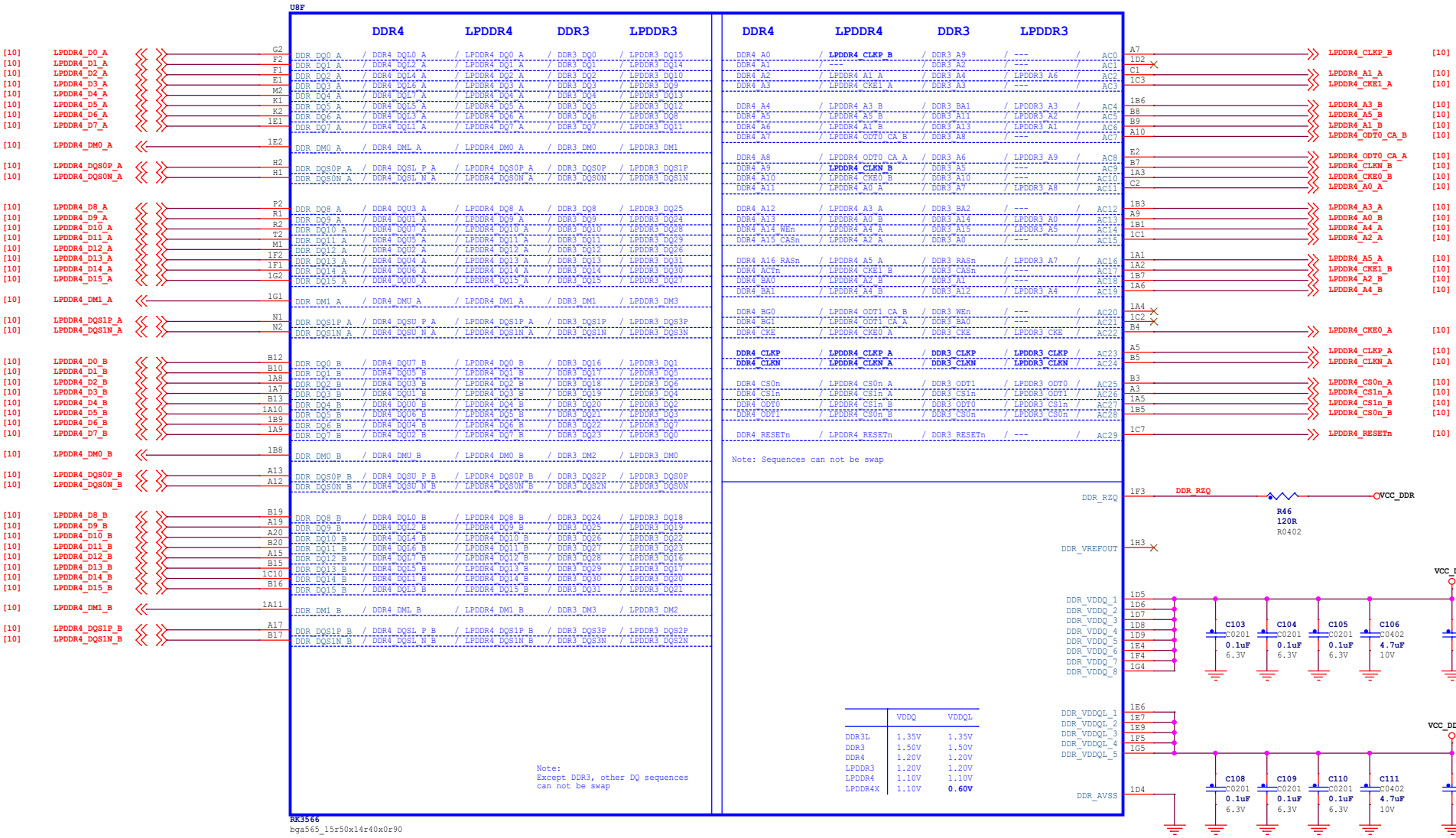
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RK3566_ABCDE

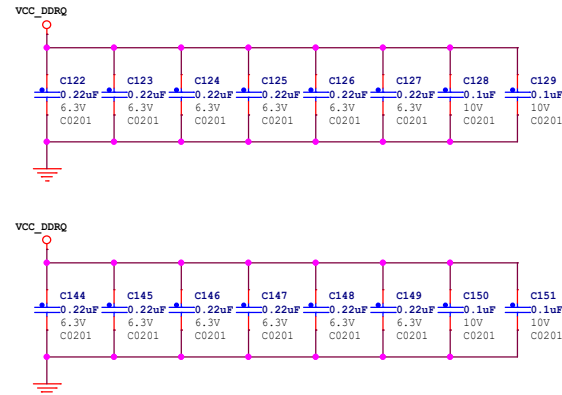
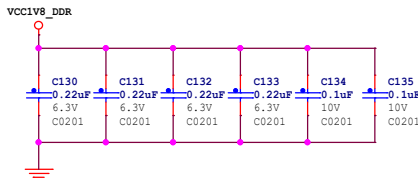
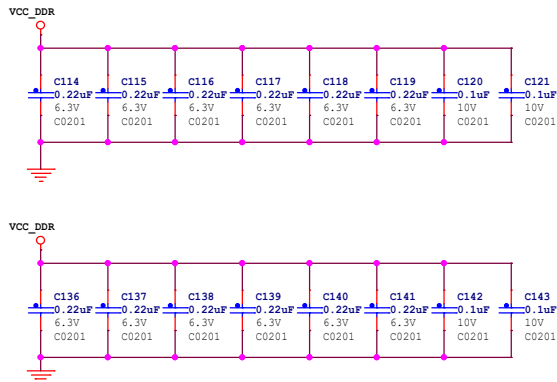
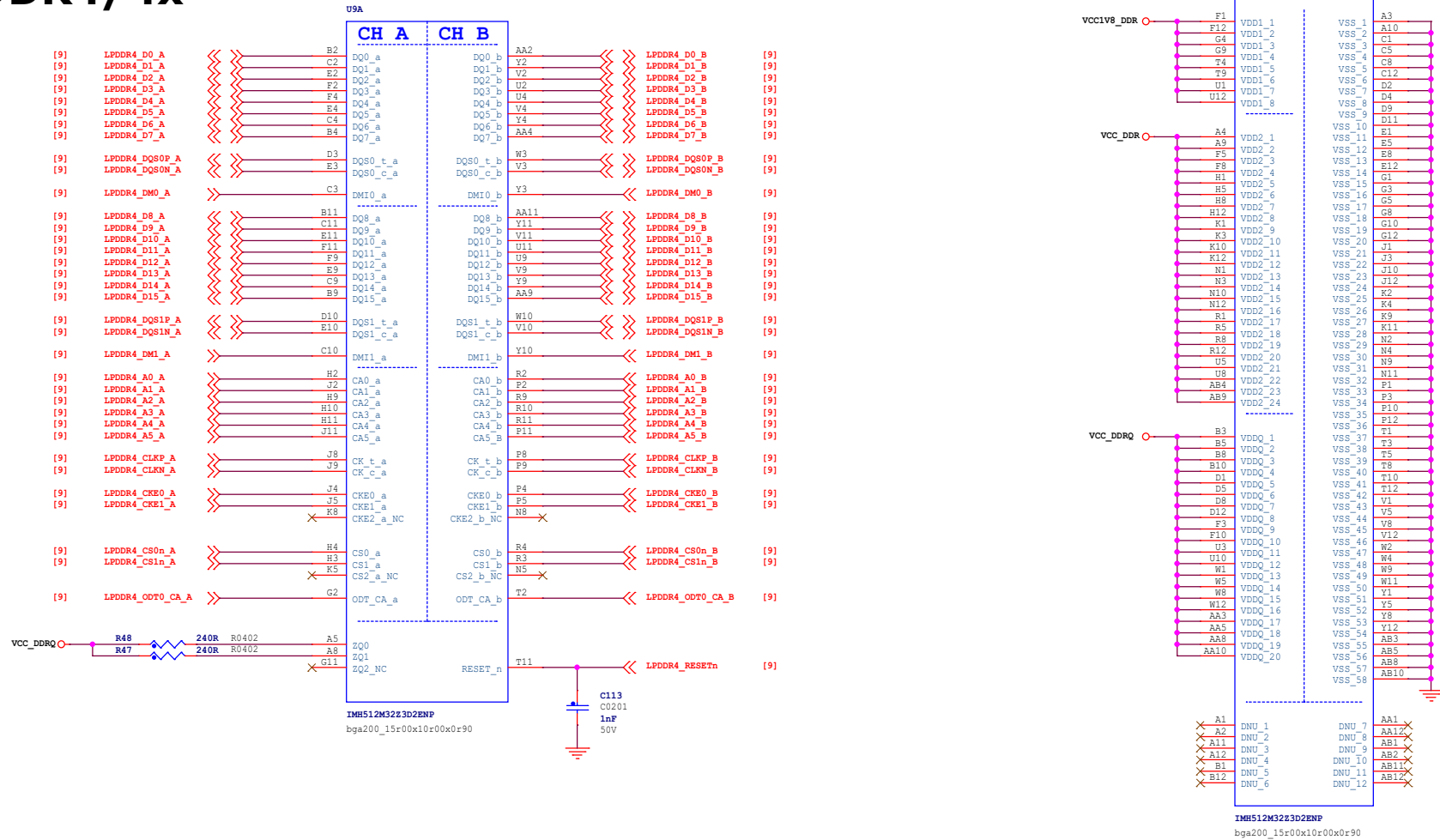
(Power&GND)



RK3566 (DDR PHY)

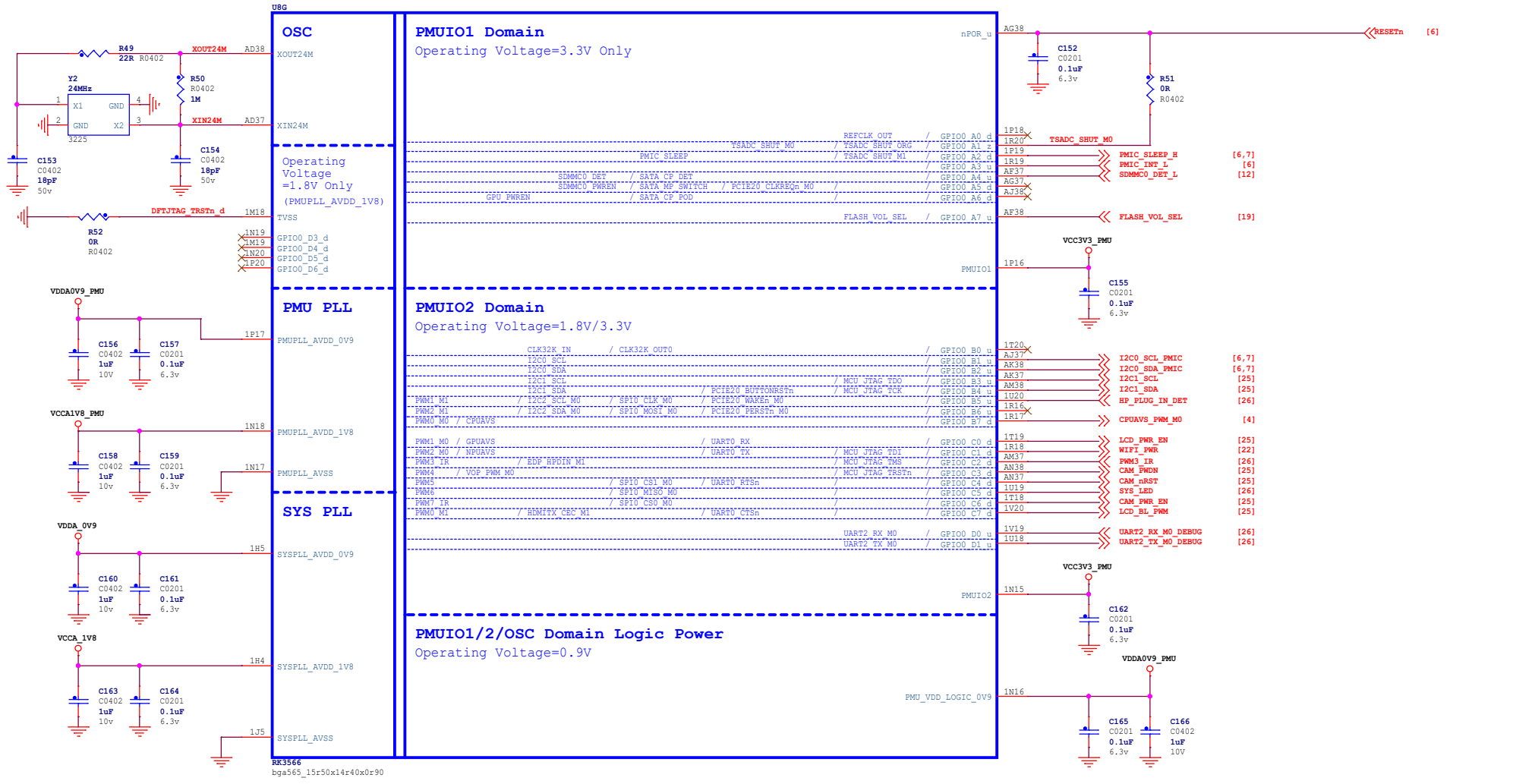


LPDDR4/4x

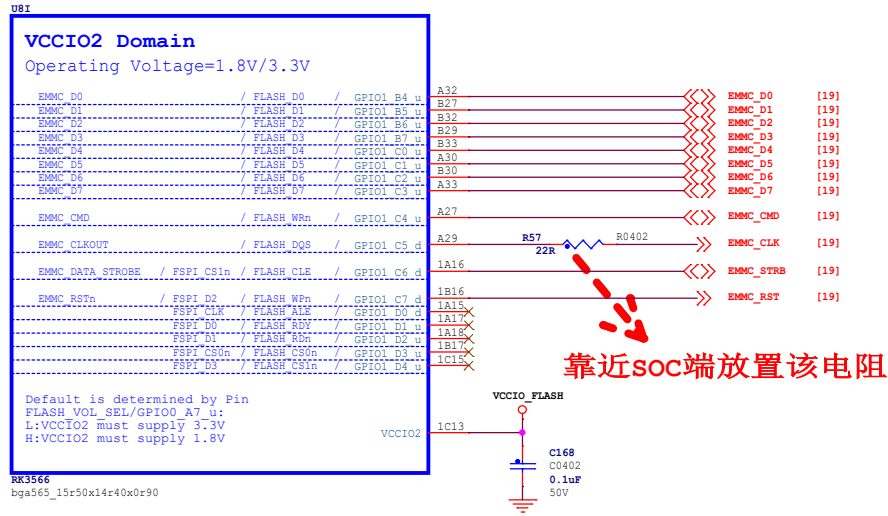


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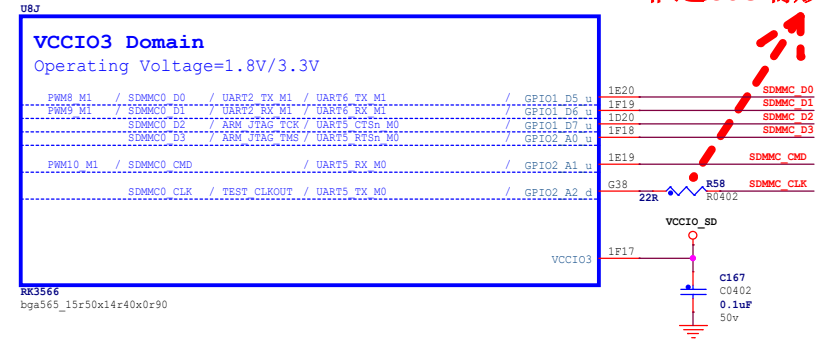
RK3566_G (OSC/PLL/PMUIO1/2)



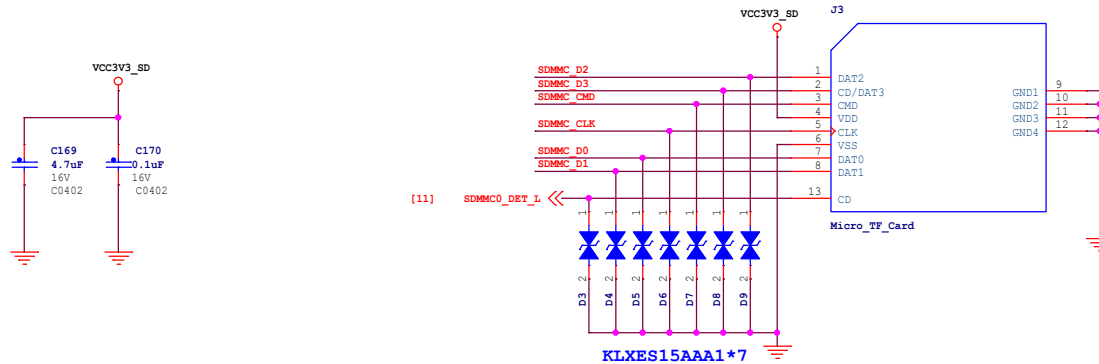
RK3566_I (VCCIO2 Domain) EMMC_IO



RK3566_J (VCCIO3 Domain) SDMMC_IO

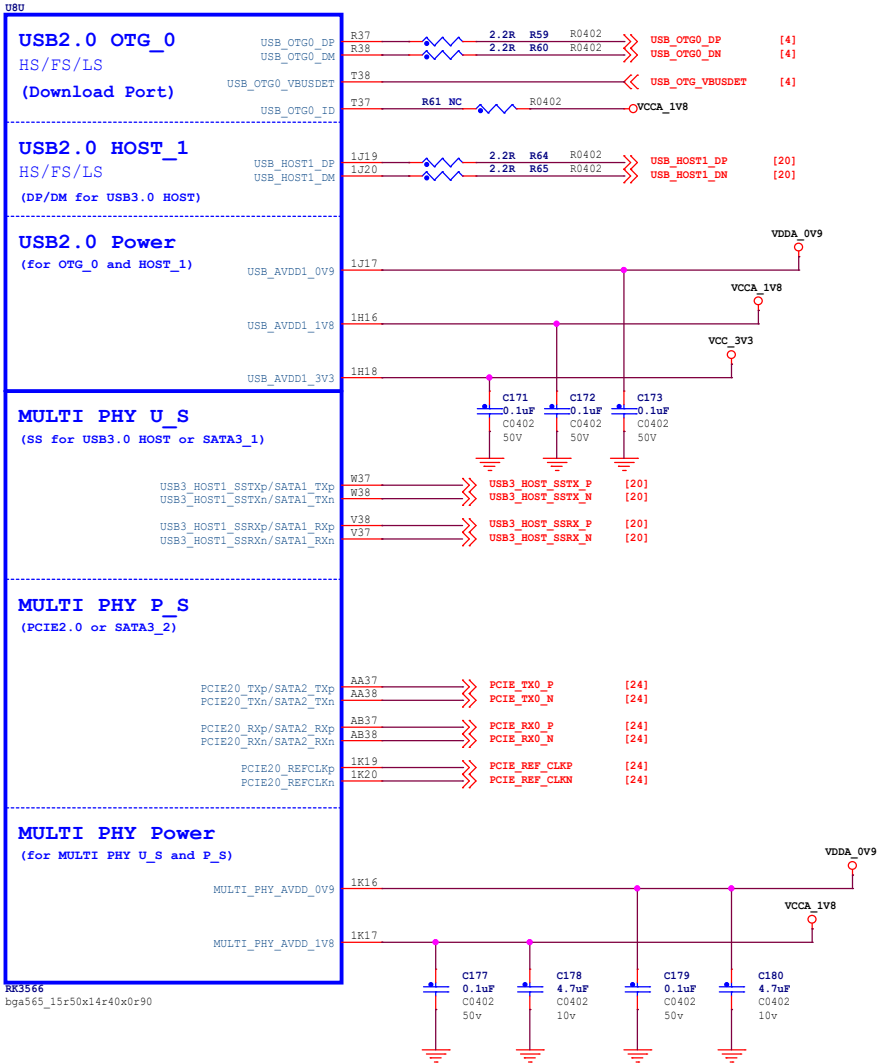


TF_CARD

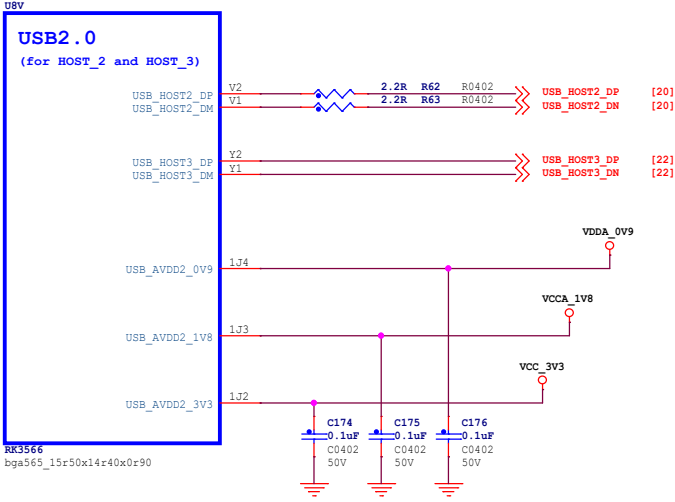


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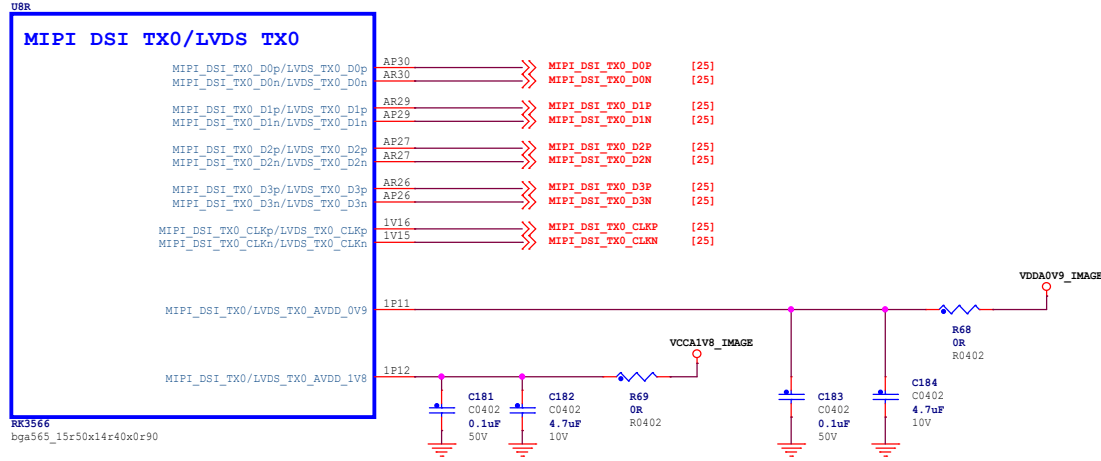
RK3566_U (USB3.0/SATA/PCIE2.0 x1)



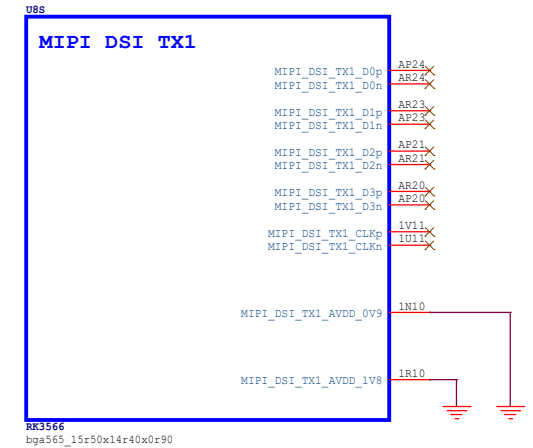
RK3566_V (USB2.0 HOST)



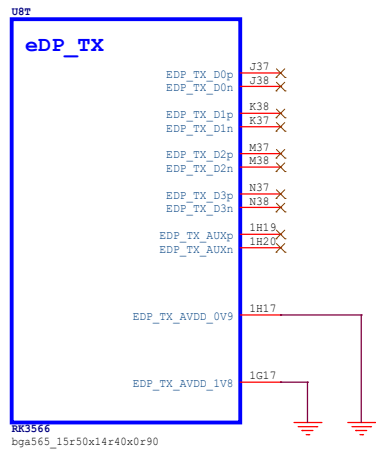
RK3566_R (MIPI_DSI_TX0/LVDS_TX0)



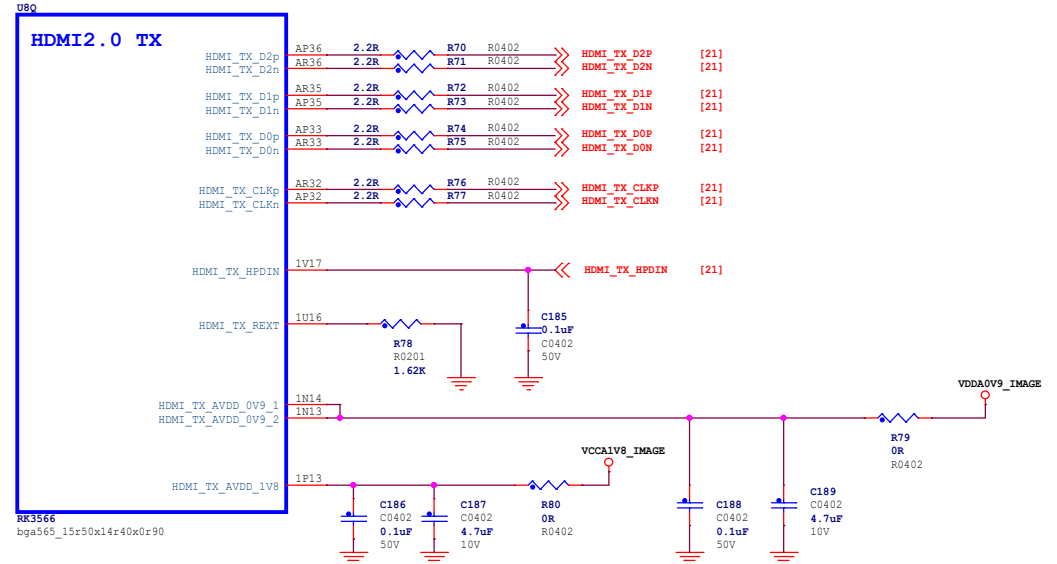
RK3566_S (MIPI_DSI_TX1)



RK3566_T (eDP/DP TX)



RK3566_Q (HDMI2.0 TX)



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Title		
野火_RK3566 LubanCat 1 N_原理图		
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A3	MIPI_DSI/EDP/HDMI_Controller	V0.2
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U3M

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

CIF D0	/ EBC SDD00	/ SDMMC2 D0 M0	/ I2S1 MCLK M1	/ VOP BT656 D0 M1	/ GPIO3 C6 d	I27			
CIF D1	/ EBC SDD01	/ SDMMC2 D1 M0	/ I2S1 MCLK TX M1	/ VOP BT656 D1 M1	/ GPIO3 C7 d	I01			
CIF D2	/ EBC SDD02	/ SDMMC2 D2 M0	/ I2S1 MCLK RX M1	/ VOP BT656 D2 M1	/ GPIO3 D0 d	AP1			
CIF D3	/ EBC SDD03	/ SDMMC2 D3 M0	/ I2S1 SDO0 M1	/ VOP BT656 D3 M1	/ GPIO3 D1 d	AN2			
CIF D4	/ EBC SDD04	/ SDMMC2 D4 M0	/ I2S1 SDO1 M1	/ VOP BT656 D4 M1	/ GPIO3 D2 d	AN2			
CIF D5	/ EBC SDD05	/ SDMMC2 D5 M0	/ I2S1 SDO1 M1	/ VOP BT656 D5 M1	/ GPIO3 D3 d	AN1			
CIF D6	/ EBC SDD06	/ SDMMC2 DET M0	/ I2S1 SDO2 M1	/ VOP BT656 D6 M1	/ GPIO3 D4 d	I22			
CIF D7	/ EBC SDD07	/ SDMMC2 PAREN M0	/ I2S1 SDO3 M1	/ VOP BT656 D7 M1	/ GPIO3 D5 d	I71			
CIF D8	/ EBC SDD08	/ GMAC1 TXD2 M1	/ UART1 TX M1	/ PDM CLK0 M1	/ GPIO3 D6 d	AL2	R194	22R	R0402
CIF D9	/ EBC SDD09	/ GMAC1 TXD3 M1	/ UART1 RX M1	/ PDM SDO1 M1	/ GPIO3 D7 d	AL1	R195	22R	R0402
CIF D10	/ EBC SDD010	/ GMAC1 RXD2 M1	/ PDM CLK1 M1	/ PDM CLK1 M1	/ GPIO4 A0 d	AK2	R196	22R	R0402
CIF D11	/ EBC SDD011	/ GMAC1 RXD3 M1	/ PDM SDO1 M1	/ PDM SDO1 M1	/ GPIO4 A1 d	IP2			
CIF D12	/ EBC SDD012	/ GMAC1 RXD3 M1	/ UART7 TX M2	/ PDM SDO2 M1	/ GPIO4 A2 d	I11			
CIF D13	/ EBC SDD013	/ GMAC1 RXD3 M1	/ UART7 RX M2	/ PDM SDO3 M1	/ GPIO4 A3 d	AJ2			
CIF D14	/ EBC SDD014	/ GMAC1 TXD3 M1	/ UART7 TX M2	/ I2S2 TXD3 M1	/ GPIO4 A4 d	I12	R197	22R	R0402
CIF D15	/ EBC SDD015	/ GMAC1 TXD3 M1	/ UART7 RX M2	/ I2S2 RXD3 M1	/ GPIO4 A5 d	AJ1	R198	22R	R0402
ISP FLASHTRIGOUT	/ EBC SDCE0	/ GMAC1 TXEN M1	/ SPI3 CS0 M0	/ I2S1 SCLK RX M1	/ GPIO4 A6 d	AH2	R199	22R	R0402
CAM CLKOUT0	/ EBC SDCE1	/ GMAC1 RXD0 M1	/ SPI3 CS1 M0	/ I2S1 LACK RX M1	/ GPIO4 A7 d	I11			
CAM CLKOUT1	/ EBC SDCE2	/ GMAC1 RXD1 M1	/ SPI3 MISO M0	/ I2S1 SDO1 M1	/ GPIO4 B0 d	I12			
ISP PRELIGHT TRIG	/ EBC SDCE3	/ GMAC1 RXDV CRS M1	/ I2S1 SDO2 M1	/ I2S1 SDO2 M1	/ GPIO4 B1 d	AG2			
I2C4 SDA M0	/ EBC VCOM	/ GMAC1 RXER M1	/ SPI3 MOSI M0	/ I2S2 SDI M1	/ GPIO4 B2 d	AF2			
I2C4 SCL M0	/ EBC GDCE	/ ETH1 REFCLK0 75M M1	/ SPI3 CLK M0	/ I2S2 SDO M1	/ GPIO4 B3 d	AE2			
ISP FLASH TRIGIN	/ I2C2 SDA M1	/ EBC GDSP	/ I2C2 SCL M1	/ VOP BT656 CLK M1	/ GPIO4 B4 d	AF1			
CIF HREF	/ EBC SDLE	/ GMAC1 MDC M1	/ UART1 RTSn M1	/ I2S2 MCLK M1	/ GPIO4 B6 d	AD1			
CIF VSYNC	/ EBC SDCE	/ GMAC1 MDIO M1	/ I2S2 SCLK TX M1	/ I2S2 SCLK TX M1	/ GPIO4 B7 d	AC2			
PWM11 IR M1	/ CIF CLKOUT	/ EBC GDCLK			/ GPIO4 C0 d	AB2			
CIF CLKIN	/ EBC SDCLK	/ GMAC1 MCLKINOUT M1	/ UART1 CTSn M1	/ I2S2 SCLK RX M1	/ GPIO4 C1 d	AB1			
VCCIO6_1						I14			
VCCIO6_2						I15			

U3M
 RK3566
 bga565_15r50x14r40x0r90

[illegible]

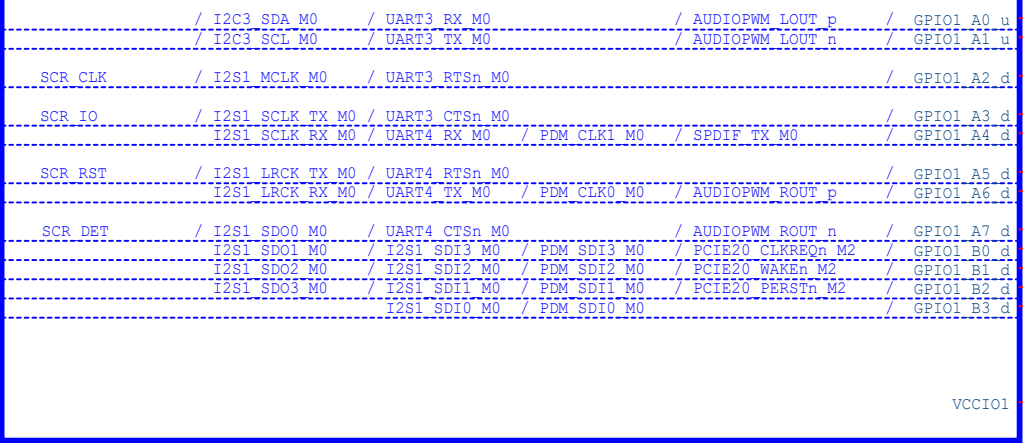
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Title 野火_RK3566 LubanCat 1 N_原理图			
Size A3	Document Number MIPIT_CSI/GMAC_Controller		Rev V0.2
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RK3566_H (VCCIO1 Domain)

U8H

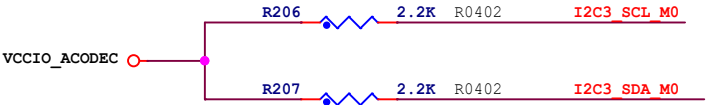
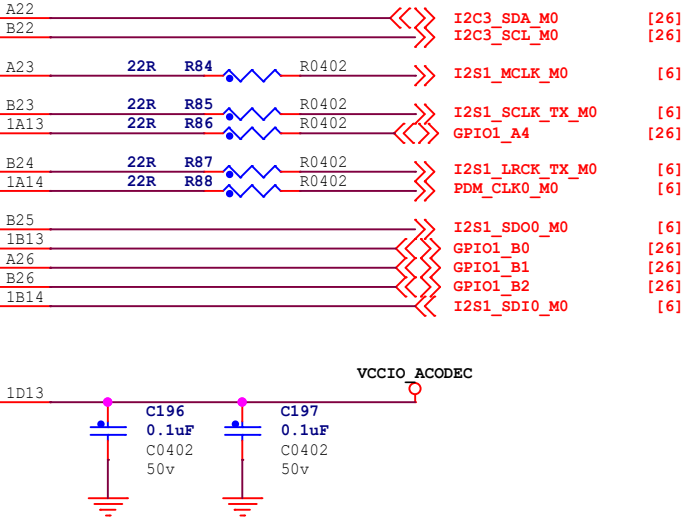
VCCIO1 Domain

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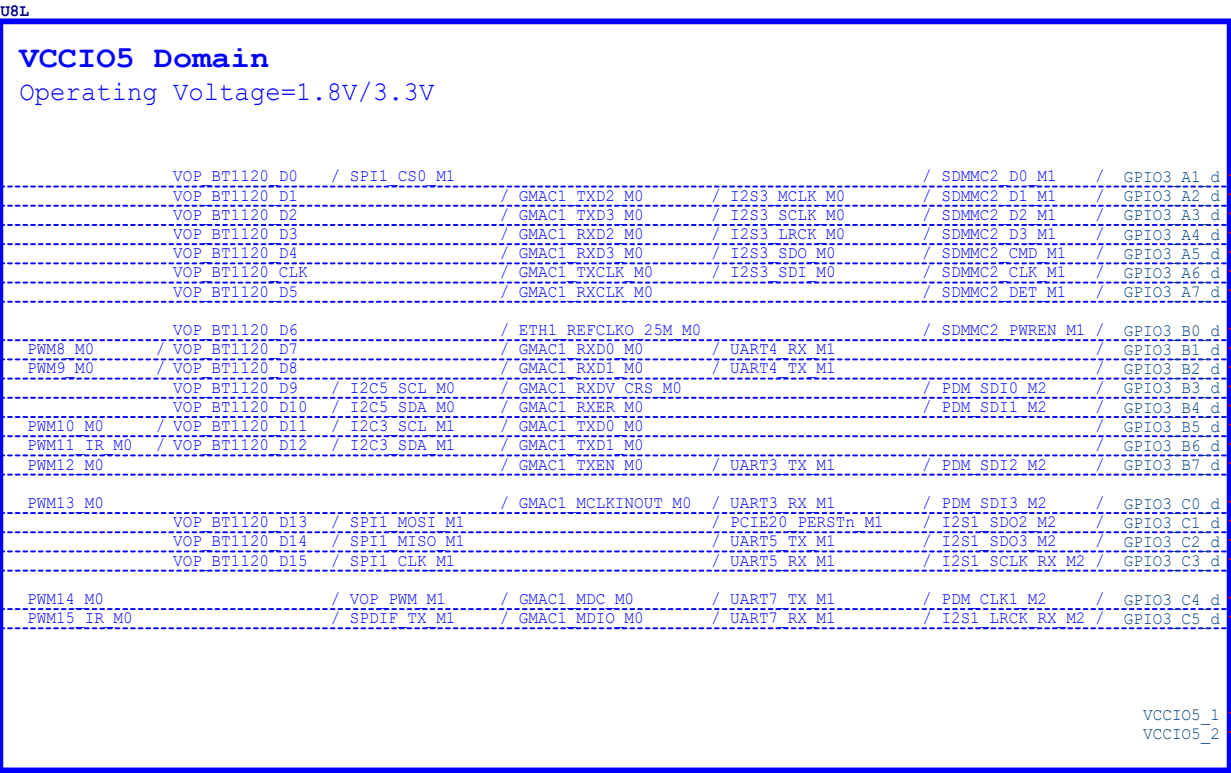
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VCCIO1



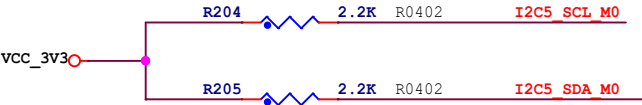
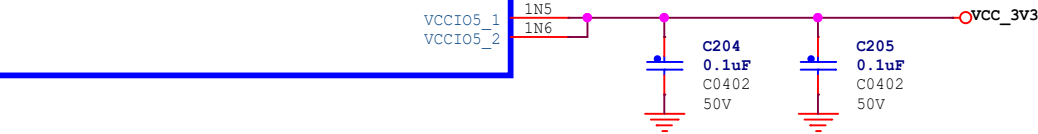
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RK3566_L(VCCIO5 Domain)



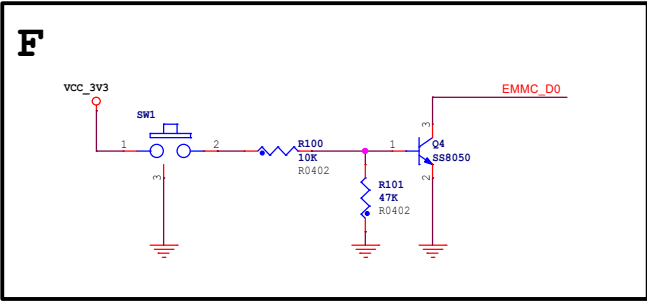
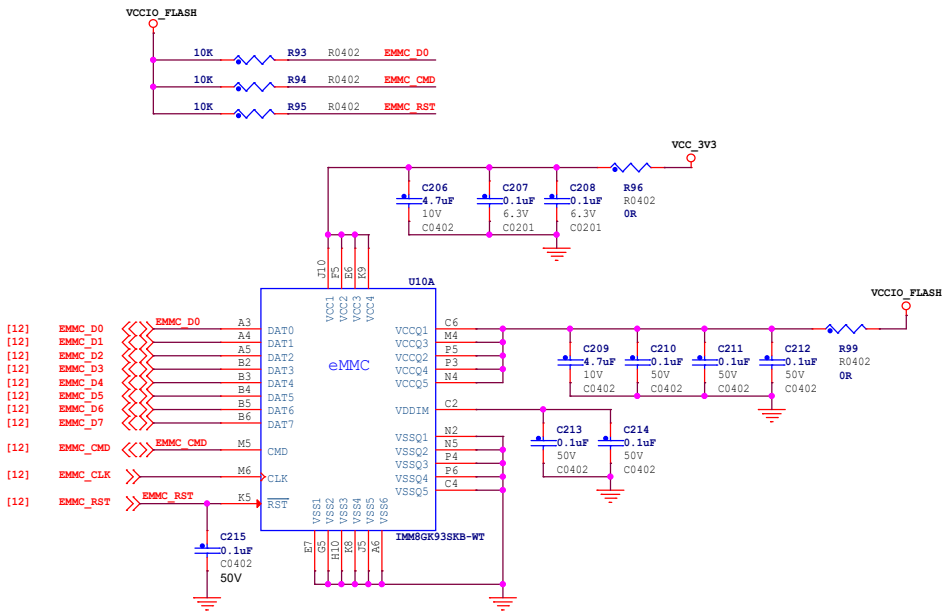
RK3566

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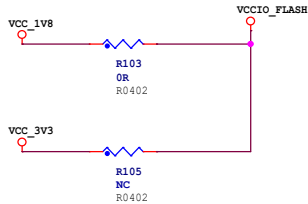


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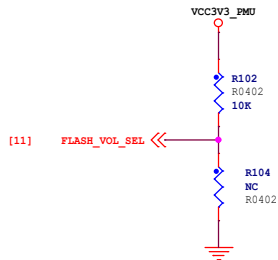
EMMC FLASH



EMMC_IO_Toggle



FLASH_VOL_SEL



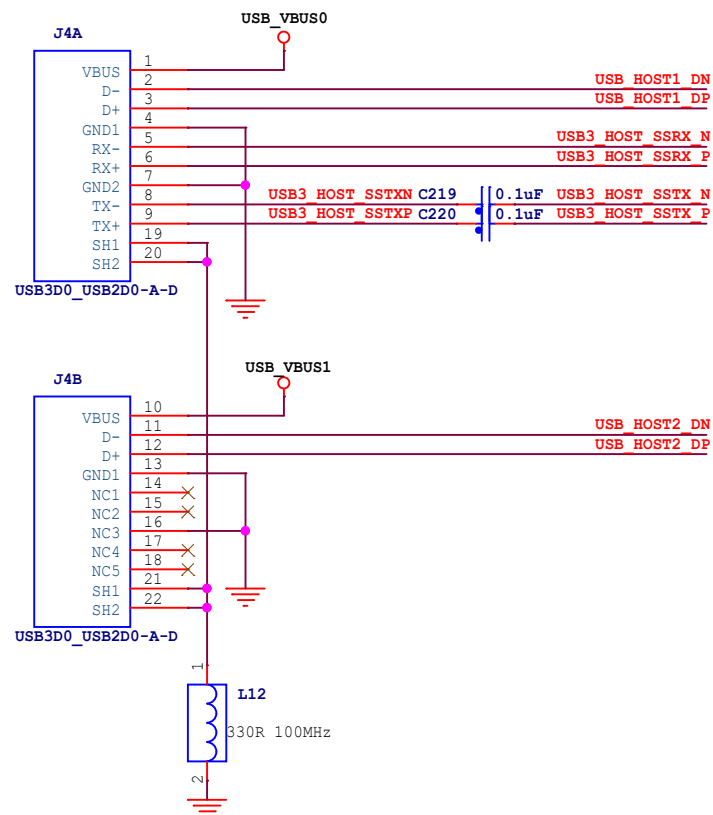
Note:

FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

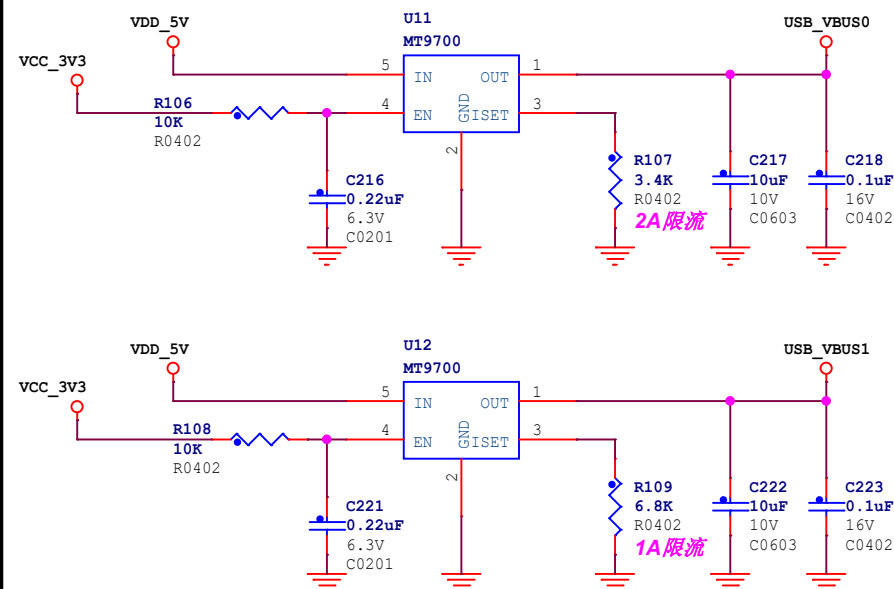
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A3	EMMC_FLASH	V0.2
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USB 3.0 HOST x1

USB 2.0 HOST x1



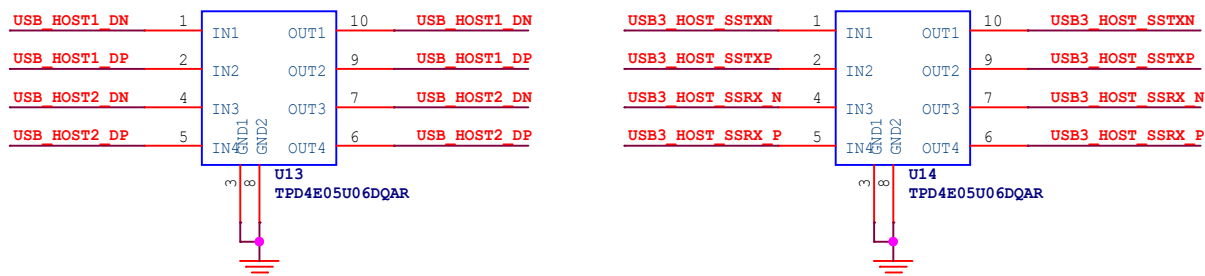
USB POWER



USB_HOST1_DN >> USB_HOST1_DN [13]
 USB_HOST1_DP >> USB_HOST1_DP [13]
 USB_HOST2_DN >> USB_HOST2_DN [13]
 USB_HOST2_DP >> USB_HOST2_DP [13]

USB3_HOST_SSRX_N >> USB3_HOST_SSRX_N [13]
 USB3_HOST_SSRX_P >> USB3_HOST_SSRX_P [13]
 USB3_HOST_SSTX_N >> USB3_HOST_SSTX_N [13]
 USB3_HOST_SSTX_P >> USB3_HOST_SSTX_P [13]

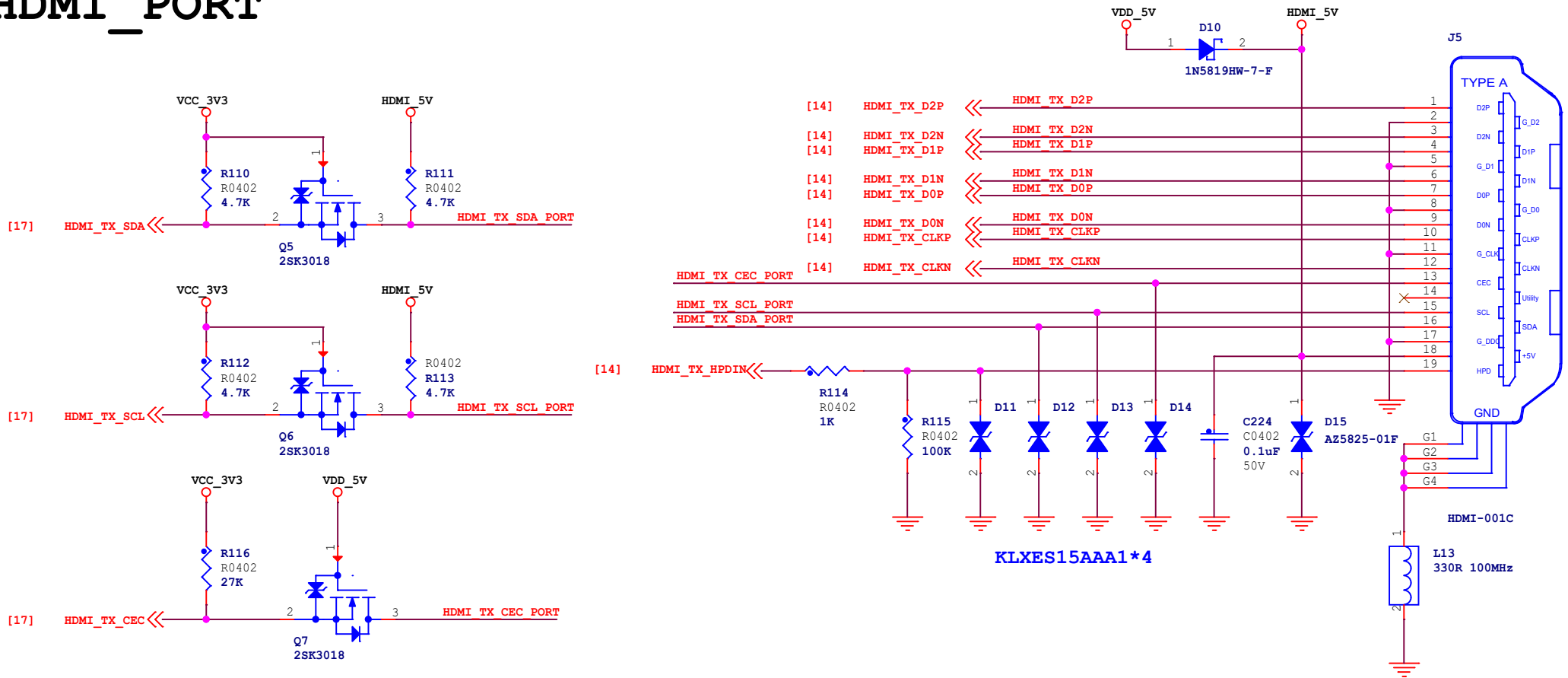
ESD



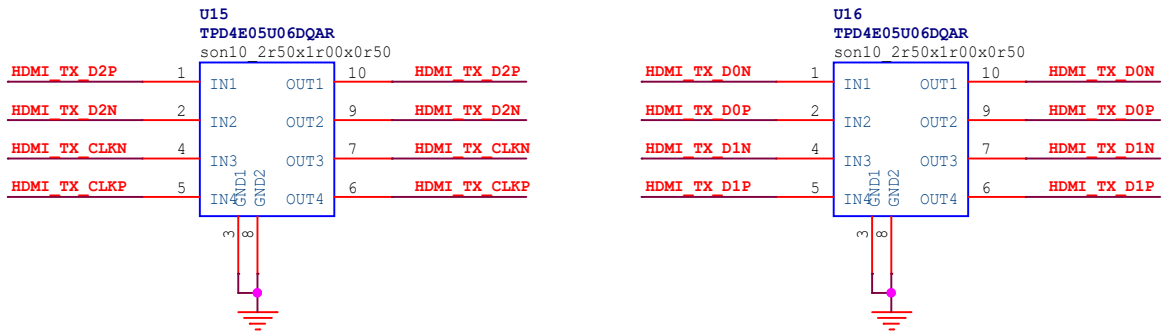
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Title 野火_RK3566 LubanCat 1 N_原理图		
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HDMI PORT



ESD



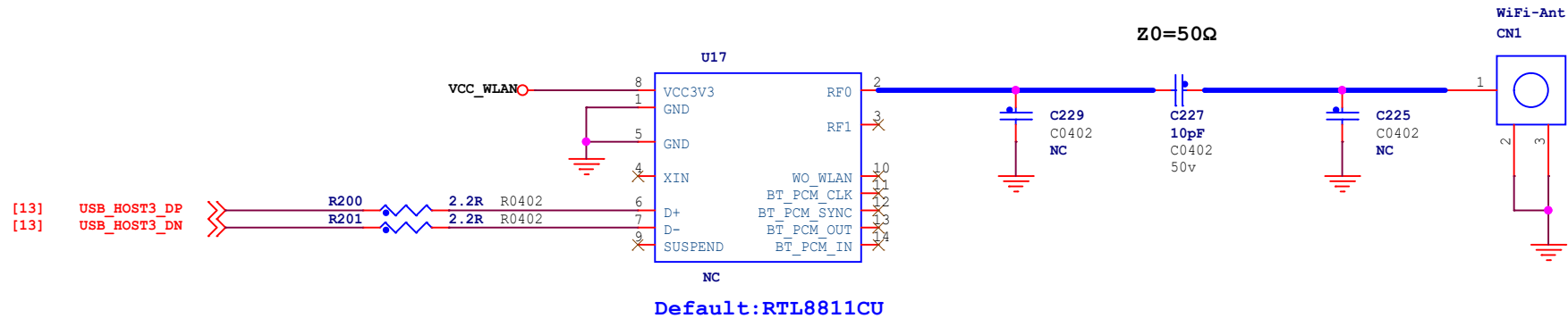
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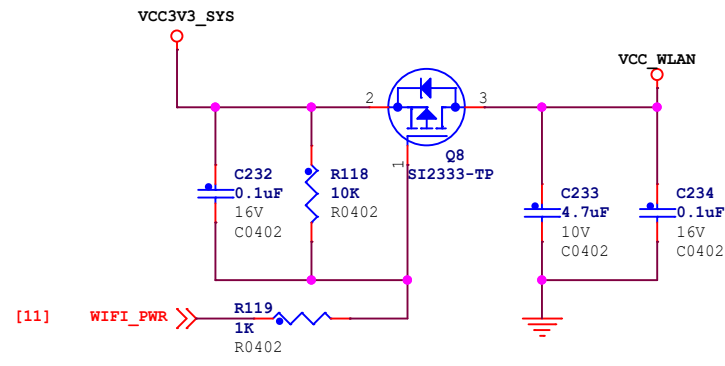
Size A4	Document Number HDMI_PORT	Rev V0.2
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WLAN



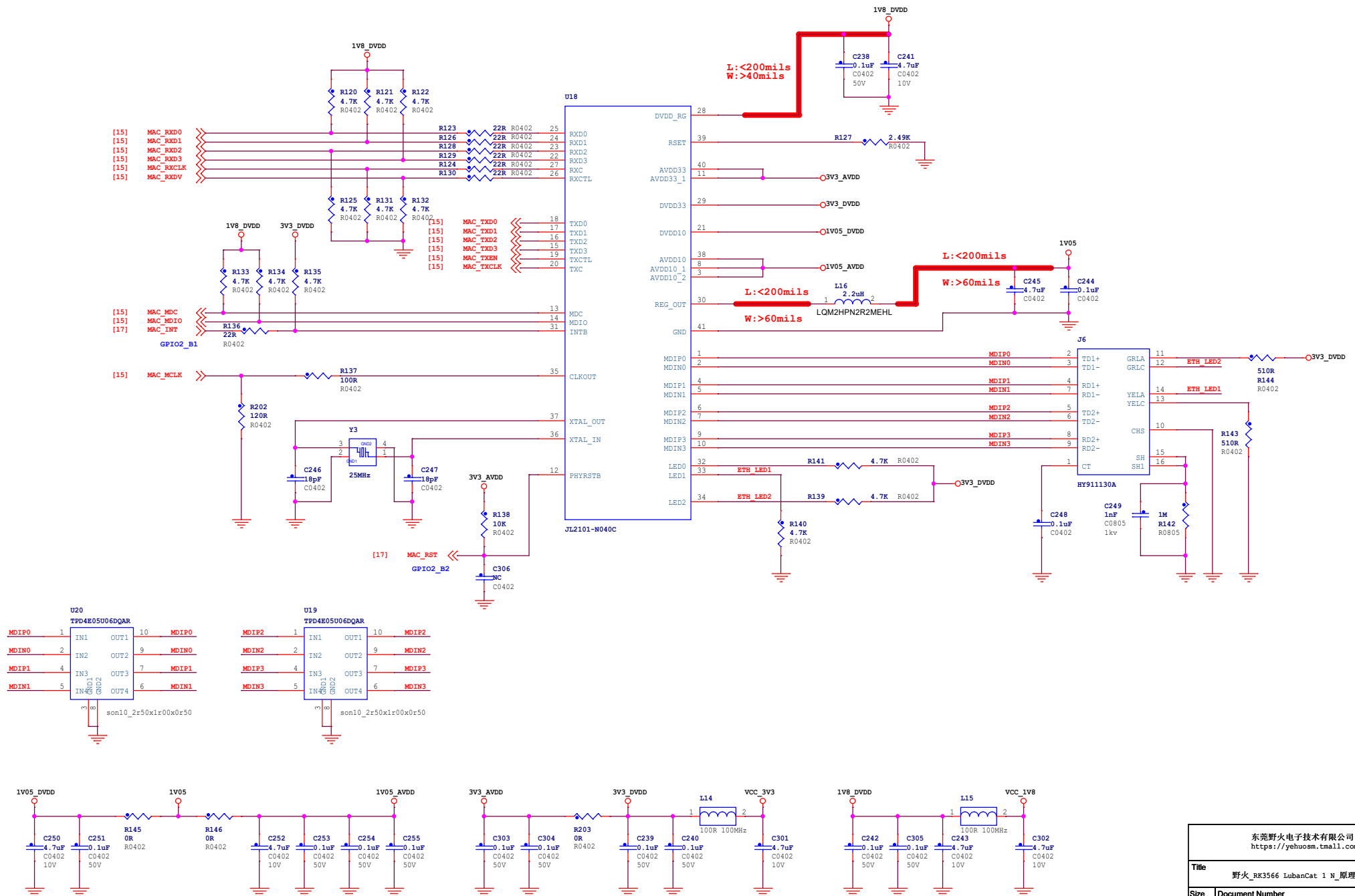
WLAN_Power



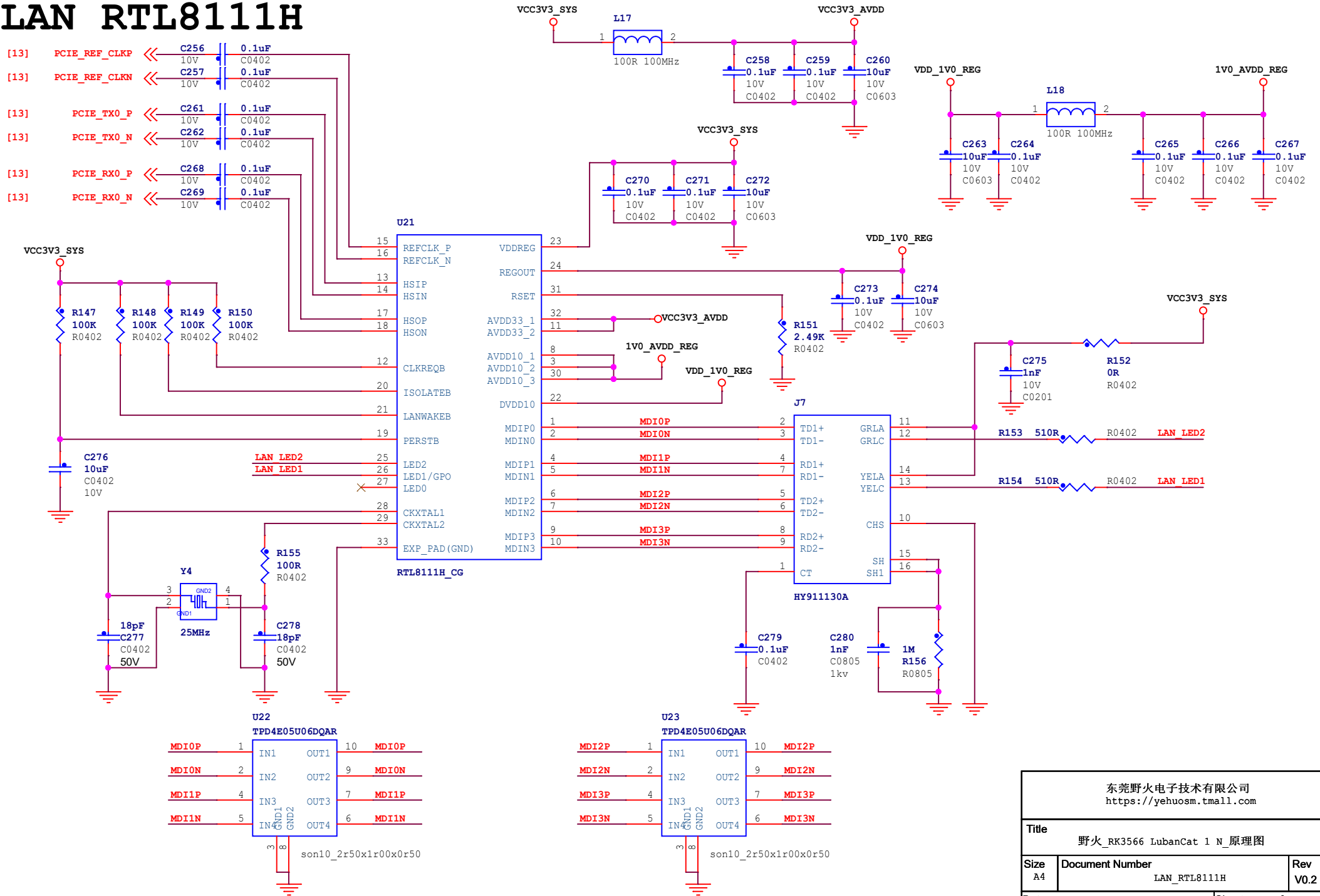
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Title 野火_RK3566 LubanCat 1 N_原理图		
Size A4	Document Number WLAN	Rev V0.2
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```
TXC / RXC : delays 2ns
PHY Address : 001
```

```
TXC / RXC : delays 2ns
PHY Address : 001
```



LAN RTL8111H



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Title	野火_RK3566 LubanCat 1 N_原理图
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Size
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Document Number

LAN_RTL8111H

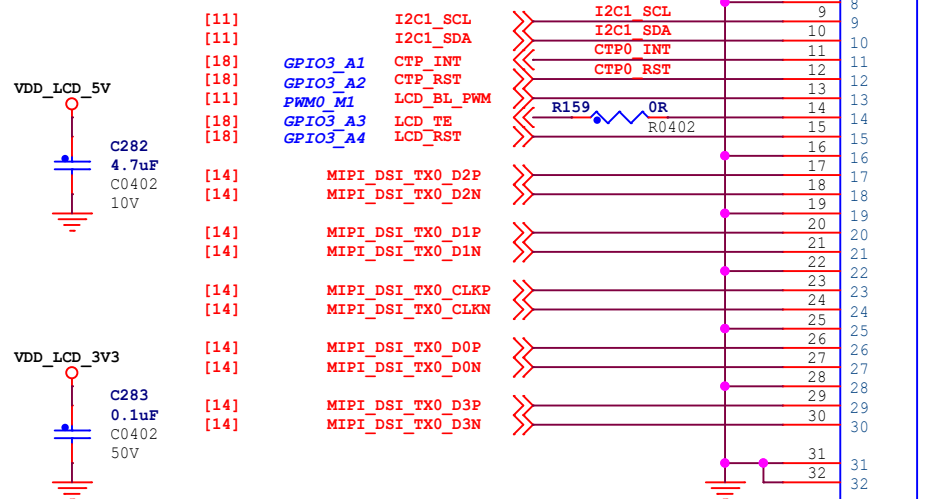
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VDD_LCD_3V3

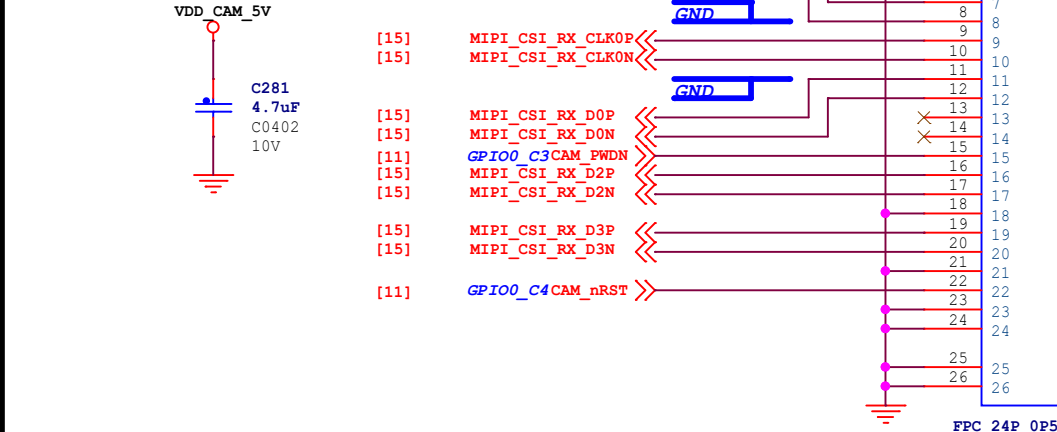
R157 10K R0402 CTP0 INT

R158 10K R0402 CTP0 RST



FPC-30P-0P5

100



[11] **LCD_PWR_EN** $\gg$ **GPIO0_C0**

U25 MT9700

- IN: 5
- OUT: 1
- EN: 4
- GND: 3

U26 MT9700

- IN: 5
- OUT: 1
- EN: 4
- GND: 3

Components:

- R160: 1K, R0402
- C284: 0.1uF, C0402, 50V
- R161: 3.4K, R0402
- C285: 10uF, C0603, 10V
- C286: 0.1uF, C0402, 50V
- C290: NC, C0402, NC
- R164: 3.4K, R0402
- C291: 10uF, C0603, 10V
- C292: 0.1uF, C0402, 50V

Labels:

- VCC3V3_SYS
- VDD_LCD_3V3
- 2A 限流

The diagram shows the PCB layout for the RK3566 camera module. The central component is the MT9700 camera chip (U25). Its power and control pins are connected as follows:

- VCC5V0_SYS** is connected to the **IN** pin (pin 5) of the MT9700.
- VDD_CAM_5V** is connected to the **OUT** pin (pin 1) of the MT9700.
- GPIO0_C6** is connected to the **EN** pin (pin 4) of the MT9700 via a 1K resistor (R162).
- The **GND** pin (pin 2) of the MT9700 is connected to ground.
- The **CISET** pin (pin 3) of the MT9700 is connected to ground via a 6.8K resistor (R163) and a 0.1uF capacitor (C287).
- The **OUT** pin (pin 1) is connected to a 10uF capacitor (C288) and a 0.1uF capacitor (C289), both connected to ground.
- The **OUT** pin (pin 1) is also connected to a 10V capacitor (C0603) and a 50V capacitor (C0402), both connected to ground.

Other components shown include:

- R165** (R0603, 0R) connected between **VCC_5V0_SYS** and **VCC5V0_SYS**.
- C293** (C0402, 4.7uF, 10V) connected between **VCC5V0_SYS** and ground.

A note "1A 限流" (1A current limiting) is present near the 6.8K resistor (R163).

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Title 野火_RK3566 LubanCat 1 N_原理图

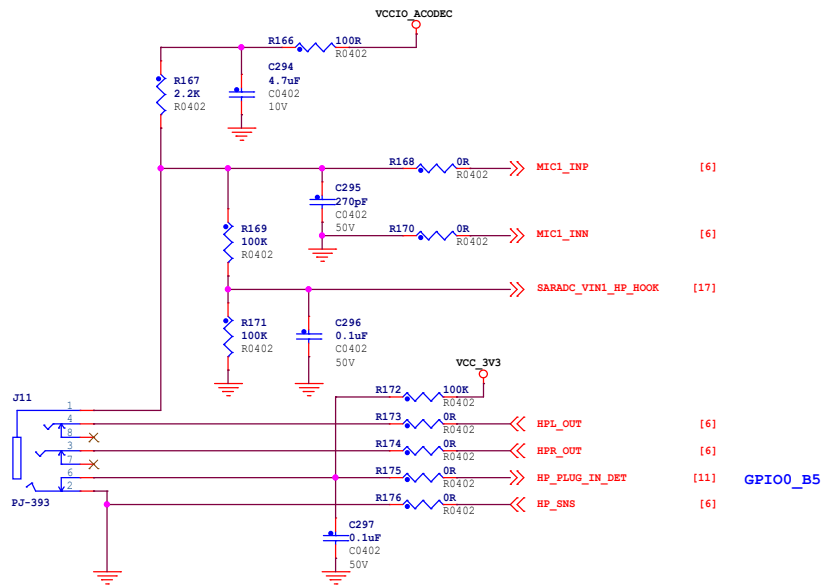
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Title	野火 RK3566 LubanCat 1 N 原理图
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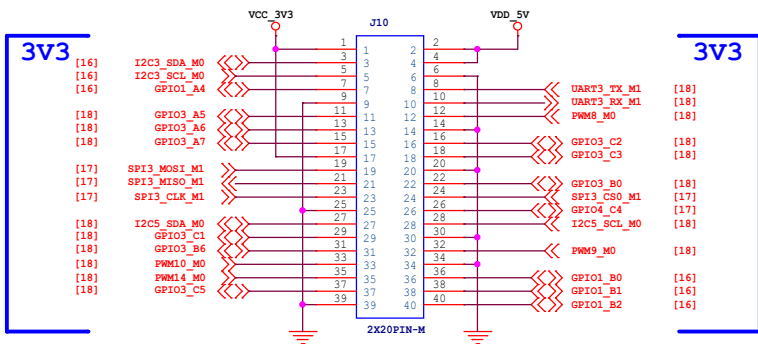
Size A4	Document Number MIPI DSI/MIPI CSI PORT	Rev V0.2
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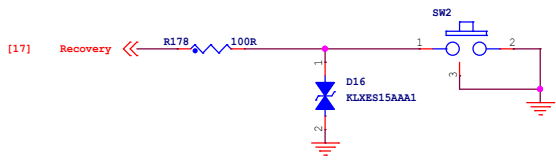
Earphone



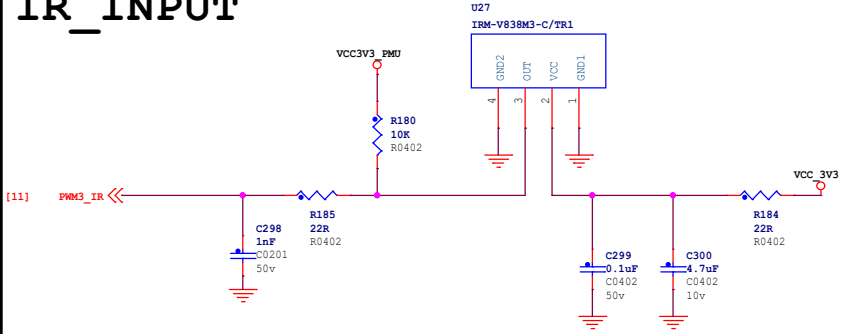
Pin Out



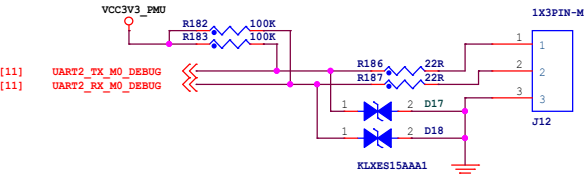
REC KEY



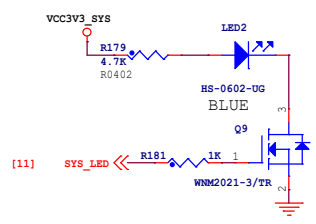
IR_INPUT



Debug UART2



SYS_LED



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Title 野火_RK3566 LubanCat 1 N 原理图		
Size A3	Document Number DEBUC/KEY/LED/IR_IN/PIN_OUT	Rev V0.2
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